



# LA5692D, 5692S, 5692M

## Voltage Regulator Driver with Watchdog Timer

### Overview

The LA5692 is a single-chip voltage regulator for microcomputer system monitor use that performs the functions of 5V output voltage control, watchdog timer, and voltage detector. Since the LA5692 can hold the reset output, it is especially suited for use in peripheral control and monitor output applications (example : valves used in refrigeration equipment, hot water supply system).

### Applications

- Microcomputer system for car equipment, refrigeration/heating equipment, office automation equipment.

### Functions

- Output voltage 5V control.
- Watchdog timer.
- Reset generation at power-ON mode.
- Reset hold output [RES (2)] (Cleared with CK reinput).

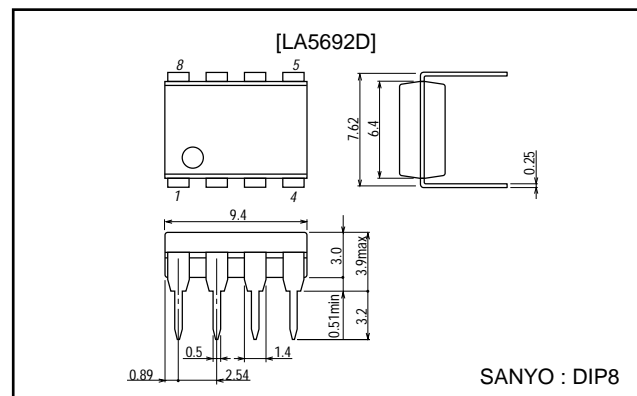
### Features

- An external PNP transistor can be used to provide a low-saturation voltage regulator.
- CK input with edge detector.
- Variable detection voltage.
- The watchdog time can be made longer.

### Package Dimensions

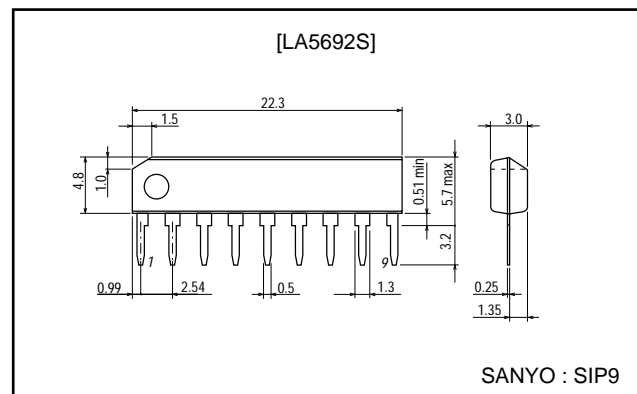
unit: mm

#### 3001B-DIP8



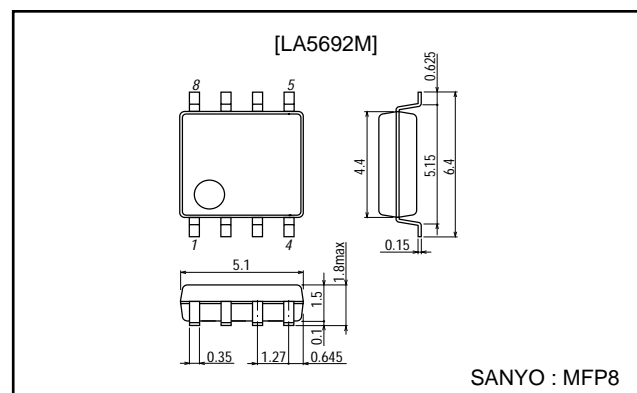
unit: mm

#### 3017B-SIP9



unit: mm

#### 3032B-MFP8



## LA5692D, 5692S, 5692M

### Specifications

#### Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Control pin voltage	V <sub>CONTmax</sub>	1s	60	V
Control pin voltage	V <sub>CONTmax</sub>		41	V
Control pin current	I <sub>CONTmax</sub>	*V <sub>CC</sub> ≥6V	11	mA
CK input voltage	V <sub>CKmax</sub>		25	V
Reset pin voltage	V <sub>RES(1)max</sub> , V <sub>RES(2)max</sub>		41	V
Allowable power dissipation	Pd max	LA5692D, 5692S	500	mW
		LA5692M	370	mW
Operating temperature	T <sub>opr</sub>		-40 to +85	°C
Storage temperature	T <sub>stg</sub>		-55 to +150	°C

\* : A PNP transistor is connected to the LA5692D, 5692S externally to provide a low-saturation voltage regulator.  
Therefore, I<sub>CONT</sub>≈100mA will flow, as starting current, in the V<sub>CC</sub> range where the output cannot be regulated.

#### Operating Conditions at Ta=25°C

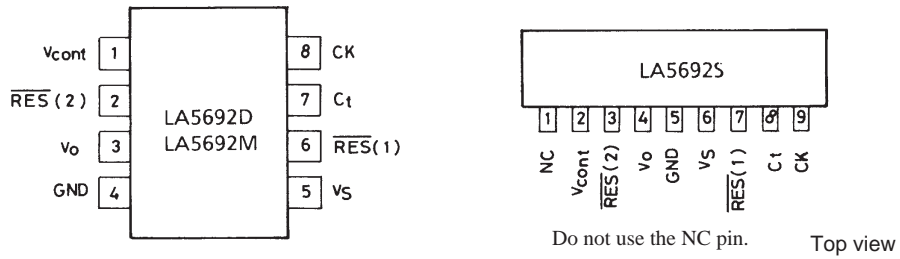
Parameter	Symbol	Conditions	Ratings	Unit
Control pin voltage	V <sub>CONT</sub>		6 to 40	V
Control pin current	I <sub>CONTmax</sub>		10	mA
Reset output current	I <sub>RES(1)max</sub> , I <sub>RES(2)max</sub>	External R pull-up	8	mA
Reset detection voltage	V <sub>S</sub> min		4	V

#### Operating Characteristics at Ta=25°C, V<sub>CC</sub>=14V, I<sub>O</sub>=50mA, unless otherwise specified.

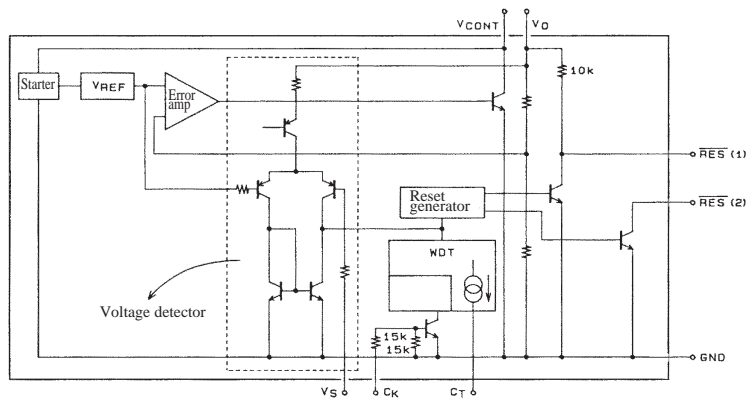
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output voltage	V <sub>O</sub>		4.8	5.0	5.2	V
Line regulation1	ΔV <sub>OLN1</sub>	9V≤V <sub>CC</sub> ≤16V		2	10	mV
Line regulation2	ΔV <sub>OLN2</sub>	6V≤V <sub>CC</sub> ≤40V		4	30	mV
Load regulation	ΔV <sub>OLD</sub>	1mA≤I <sub>O</sub> ≤50mA		4	30	mV
Current dissipation	I <sub>CC</sub>	I <sub>O</sub> =0		4.4	6.5	mA
Output noise voltage	V <sub>NO</sub>	10Hz≤f≤100kHz, V <sub>CK</sub> =0		150		μV
Temperature coefficient of output voltage	ΔV <sub>O</sub> / ΔTa	I <sub>O</sub> =5mA, -40°C≤Ta≤+85°C		±0.2		mV/°C
Reference voltage	V <sub>REF</sub>		1.13	1.18	1.23	V
'H'-level CK input voltage	V <sub>IH</sub>		2			V
'L'-level CK input voltage	V <sub>IL</sub>				0.8	V
'H'-level CK input current	I <sub>IH</sub>	V <sub>CK</sub> =5V		0.3	0.7	mA
'L'-level CK input current	I <sub>IL</sub>	V <sub>CK</sub> =0V	-1.0	-0.1		μA
'H'-level reset output voltage	V <sub>ORH(1)</sub> / V <sub>ORH(2)</sub>	RES(2) : 10kΩ pull-up	4.8	5.0	5.2	V
'L'-level reset output voltage1	V <sub>ORL(1)1</sub> / V <sub>ORL(2)1</sub>	RES(2) : 10kΩ pull-up		40	200	mV
'L'-level reset output voltage2	V <sub>ORL(1)2</sub> / V <sub>ORL(2)2</sub>	I <sub>RES(1)</sub> =I <sub>RES(2)</sub> =8mA		0.16	0.8	V
CK input pulse width	t <sub>CKW</sub>	V <sub>CK</sub> =5V	3			μs
Reset output delay time	t <sub>d</sub>	C <sub>t</sub> =1μF	7.5	10	12.5	ms
Watchdog time	t <sub>WD</sub>	C <sub>t</sub> =1μF	30	40	50	ms
Watchdog reset time	t <sub>WR</sub>	C <sub>t</sub> =1μF	0.1	0.25	0.4	ms
Reset hysteresis voltage	V <sub>hys</sub>	V <sub>S</sub> =4.5V	100	200	300	mV

# LA5692D, 5692S, 5692M

## Pin Assignment

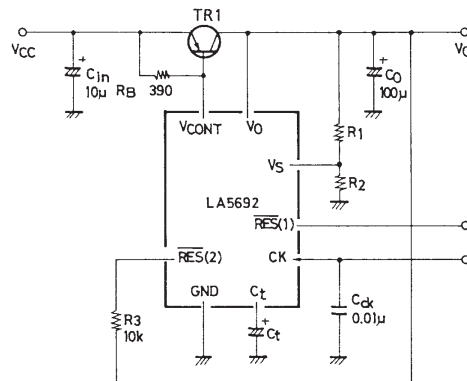


## Equivalent Circuit Block Diagram



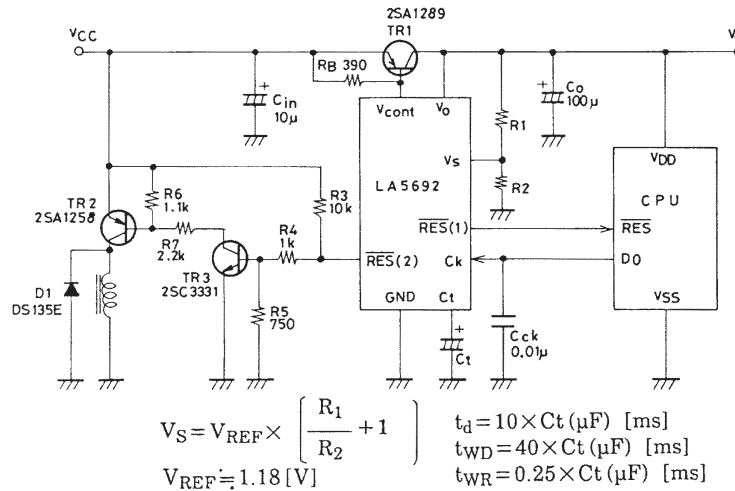
RES(1) : Contains a pull-up resistor of 10kΩ.  
 RES(2) : Open collector

## Test Circuit



Unit (resistance : Ω, capacitance : F)

Sample Application Circuit

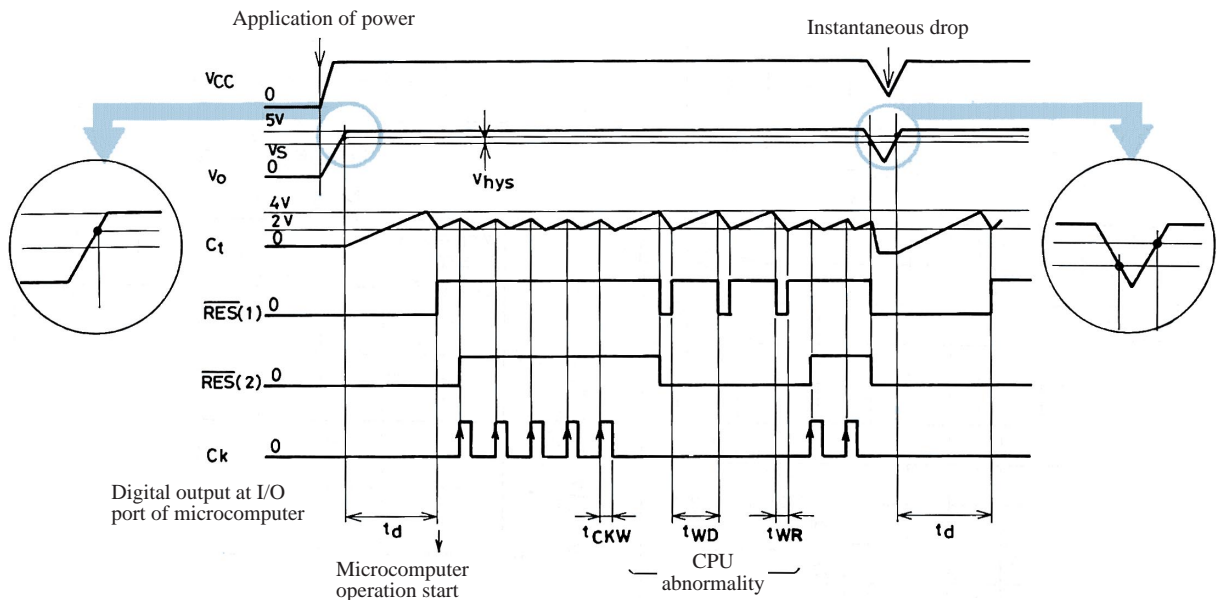


Unit (resistance : Ω, capacitance : F)

Note on application

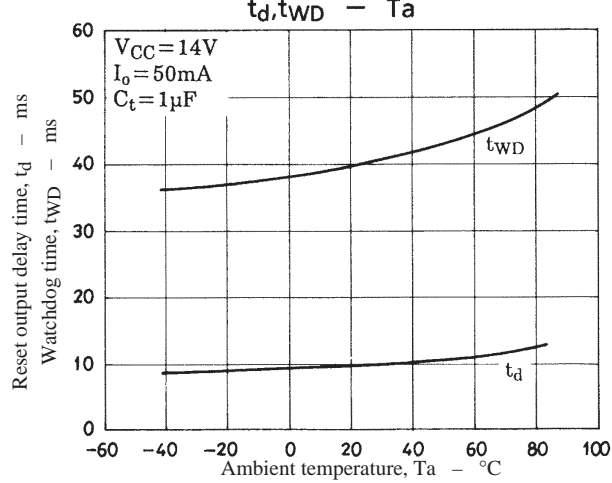
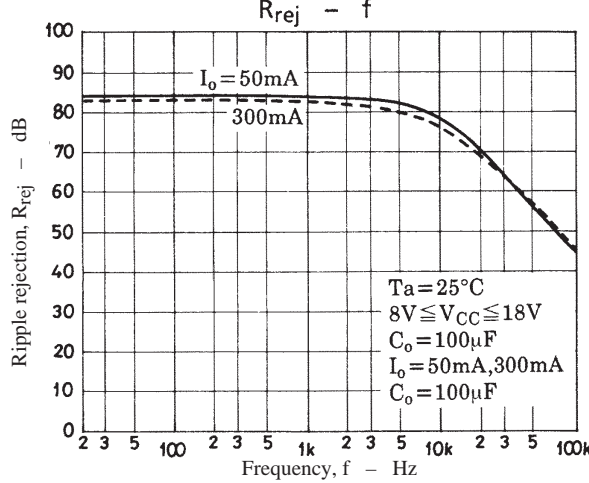
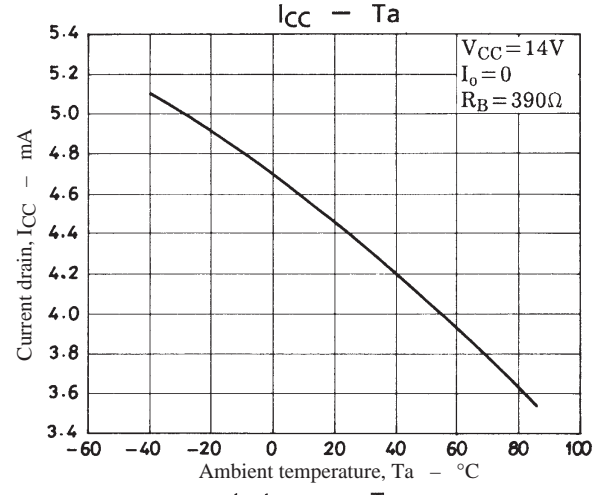
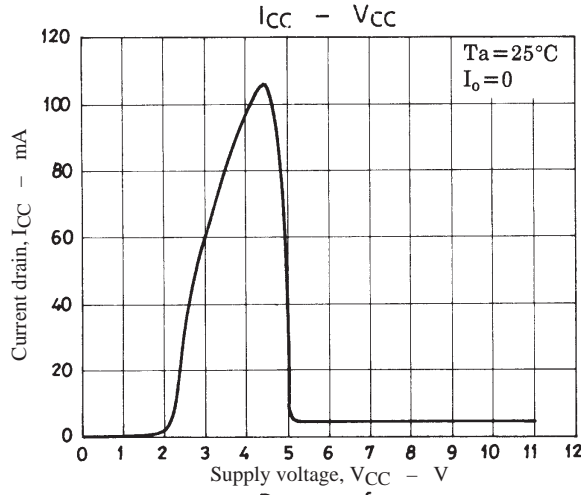
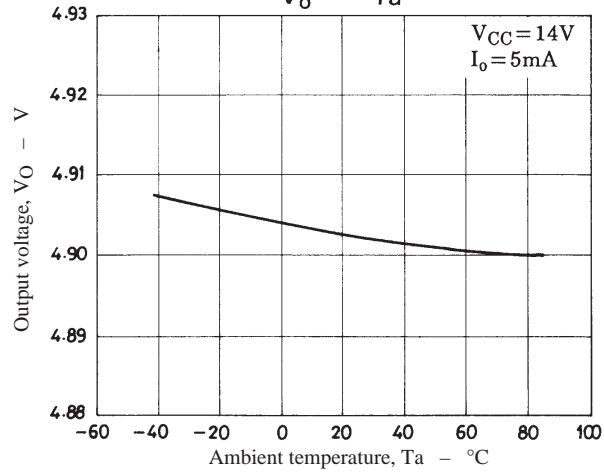
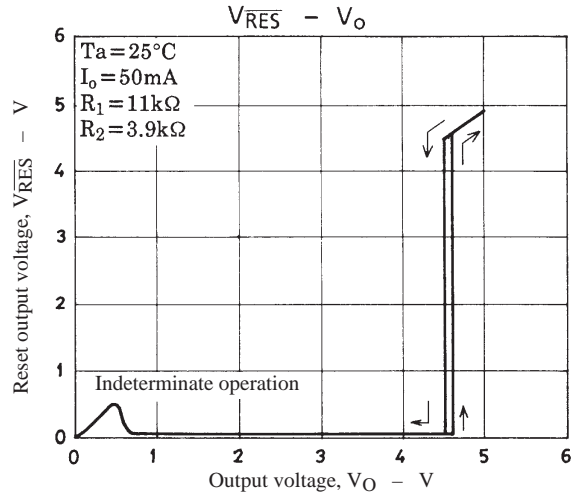
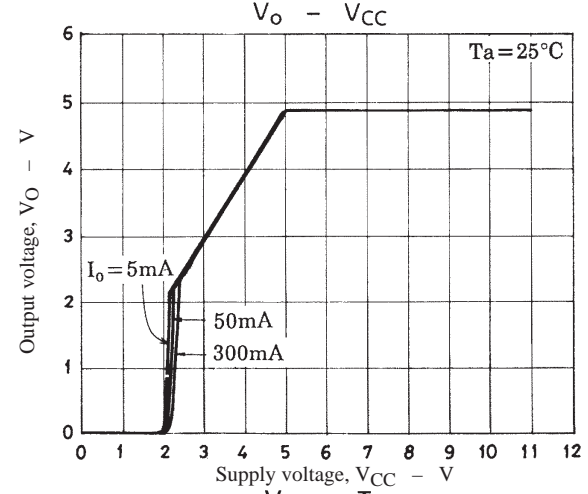
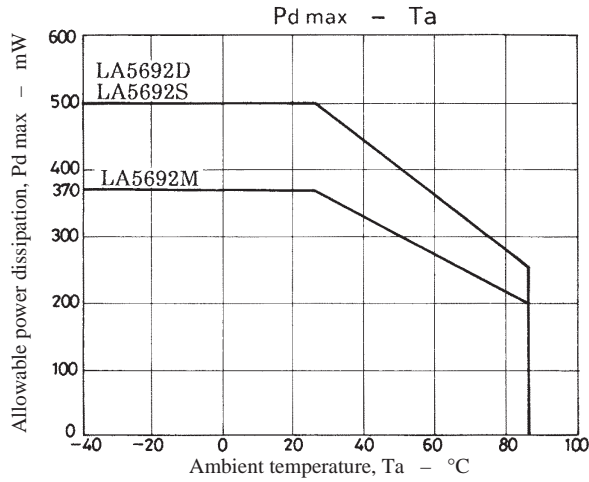
1. For stable operation, place  $C_{in}$ ,  $C_o$ , and TR1 as near to the IC as possible.
2. When used in 0°C or below it, a capacitor of which impedance at high-frequency operation is low and has a good temperature characteristic (such as SANYO OS-CON capacitor or others) should be used to prevent oscillation.
3. Set  $V_S$  to the output voltage level where the circuit will be reset using external resistors R1 and R2.  $V_S$  should be set to 4V or greater due to internal circuit operation.
4.  $C_{CK}$  must be inserted to cut the high range element of clock noise to prevent it from becoming a reset output noise.
5. For  $C_t$ , a capacitor which less varies the capacitance according to the temperature should be used.

Timing Chart

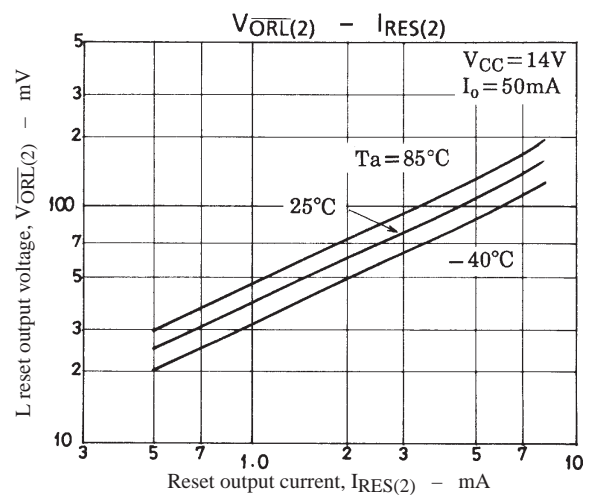
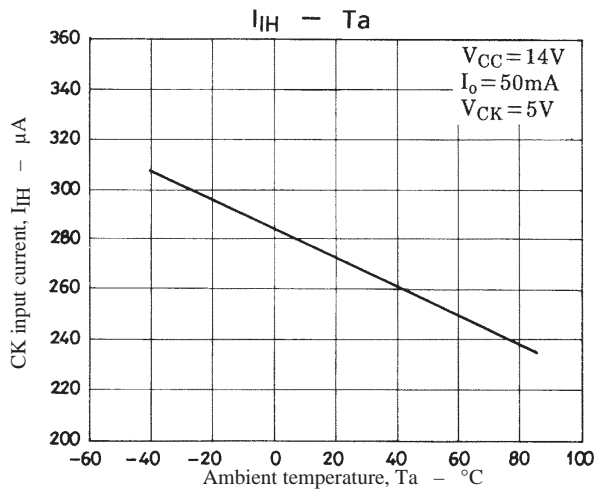
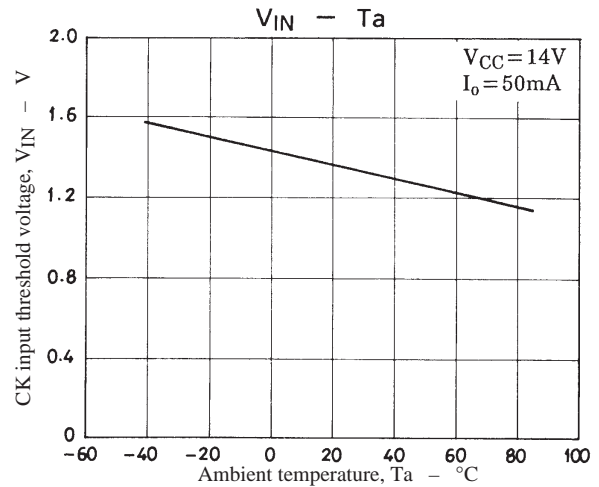
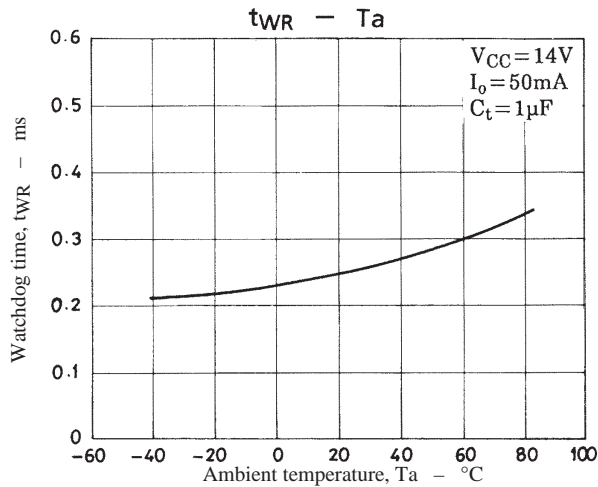


Note : Edge-triggered at the point indicated by the arrow of  $C_K$  signal.

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