Ordering number: EN 3244

Monolithic Linear IC

SANYO No.3244

LA5691D, 5691S

Voltage Regulator Driver with Watchdog Timer (with Output ON/OFF Function)

The LA5691 is a single-chip voltage regulator for microcomputer system monitor use that performs the functions of 5V output voltage control, watchdog timer, and voltage detector. Since the LA5691 is capable of exercising output ON/OFF controls it is especially suited for use in battery-powered equipment.

Applications

- Microcomputer system for car equipment, refrigeration/heating equipment, office automation equipment.

Functions

- Output voltage 5Vcontrol
- Watchdog timer
- Reset generation at power-ON mode
- The enable pin can be used to exercise output ON/OFF control. (Active-low)

Features

- An external PNP transistor can be used to provide a low-saturation voltage regulator.
- Capable of reducing of power dissipation at standby mode ($I_{Q\,OFF}$=300mA typ)
- CK input with edge detector
- Variable detection voltage

Maximum Ratings at Ta=25°C

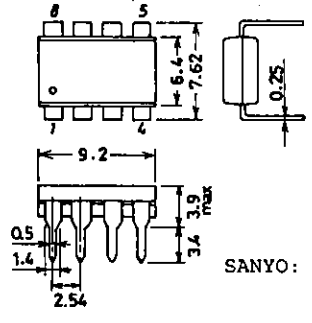
				unit
Control Pin Voltage	V_{CONT} max	1sec	60	V
Control Pin Voltage	V_{CONT} max		41	V
Control Pin Current	I_{CONT} max	*V_{CC}≧6V	11	mA
Enable Pin Voltage	$V_{\overline{EN}}$ max		41	V
CK Input Voltage	V_{CK} max		25	V
Reset Pin Voltage	$V_{\overline{RES}}$ max,		41	V
Allowable Power Dissipation	Pd max		500	mW
Operating Temperature	Topr		−40 to +85	°C
Storage Temperature	Tstg		−55 to +150	°C

*: A PNP transistor is connected to the LA5691D, 5691S externally to provide a low-saturation voltage regulator. Therefore, I_{CONT}≒100mA will flow, as starting current, in the V_{CC} range where the output cannot be regulated.

Operating Conditions at Ta=25°C

			unit
Control Pin Voltage	V_{CONT}	6 to 40	V
Control Pin Current	I_{CONT} max	10	mA
Reset Output Current	$I_{\overline{RES}}$ max,	External R pull-up (with pull-up R 10kΩ) 8	mA
Reset Detection Voltage	V_S min	4	V

Package Dimensions (unit: mm) **3001B** [LA5691D]



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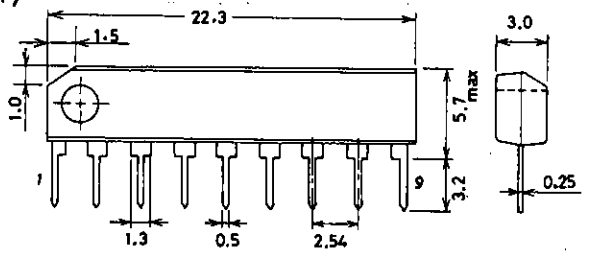
Package Dimensions (unit: mm) **3017B** [LA5691S]



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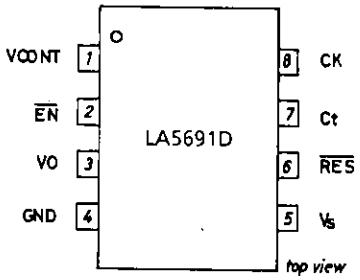
Operating Characteristics at Ta = 25°C, V_{CC} = 14V, I_O = 50mA, unless otherwise specified, See specified Test Circuit.

			min	typ	max	unit
Output Voltage	V_O		4.8	5.0	5.2	V
Line Regulation	ΔV_{OLN1}	9V ≦ V_{CC} ≦ 16V		2	10	mV
	ΔV_{OLN2}	6V ≦ V_{CC} ≦ 40V		4	30	mV
Load Regulation	ΔV_{OLD}	1mA ≦ I_O ≦ 50mA		4	30	mV
Current Dissipation	I_{CC}	I_O = 0		4.1	6.5	mA
Output Noise Voltage	V_{NO}	10Hz ≦ f ≦ 100kHz, V_{CK} = 0		200		μV
Temperature Coefficient of Output Voltage	$\Delta V_O / \Delta Ta$	I_O = 5mA, −40°C ≦ Ta ≦ +85°C		±0.2		mV/°C
Reference Voltage	V_{REF}		1.13	1.18	1.23	V
"H"-Level CK Input Voltage	V_{IH}		2			V
"L"-Level CK Input Voltage	V_{IL}				0.8	V
"H"-Level CK Input Current	I_{IH}	V_{CK} = 5V		0.3	0.7	mA
"L"-Level CK Input Current	I_{IL}	V_{CK} = 0	−1.0	−0.1		μA
"H"-Level Reset Output Voltage	$V_{\overline{ORH}}$		4.8	5.0	5.2	V
"L"-Level Reset Output Voltage 1	$V_{\overline{ORL1}}$			40	200	mV
"L"-Level Reset Output Voltage 2	$V_{\overline{ORL2}}$	$I_{\overline{RES}}$ = 8mA		0.16	0.8	V
CK Input Pulse Width	t_{CKW}	V_{CK} = 5V	3			μs
Reset Output Delay Time	t_d	C_t = 1μF	7.5	10	12.5	ms
Watchdog Time	t_{WD}	C_t = 1μF	3.8	5.0	6.2	ms
Watchdog Reset Time	t_{WR}	C_t = 1μF	0.1	0.25	0.4	ms
Reset Hysteresis Voltage	Vhys	V_S = 4.5V	100	200	300	mV
"L"-Level Output Voltage	$V_{O\,OFF}$	$V_{\overline{EN}}$ = 5V		150	300	mV
Quiescent Current	$I_{Q\,OFF}$	$V_{\overline{EN}}$ = 5V		300	600	μA
Output OFF Control Voltage	$V_{\overline{EN}H}$	Output OFF	2			V
Output ON Control Voltage	$V_{\overline{EN}L}$	Output ON			0.8	V

Pin Assignment



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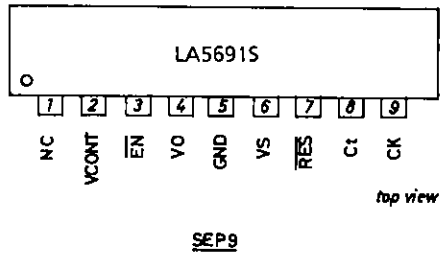

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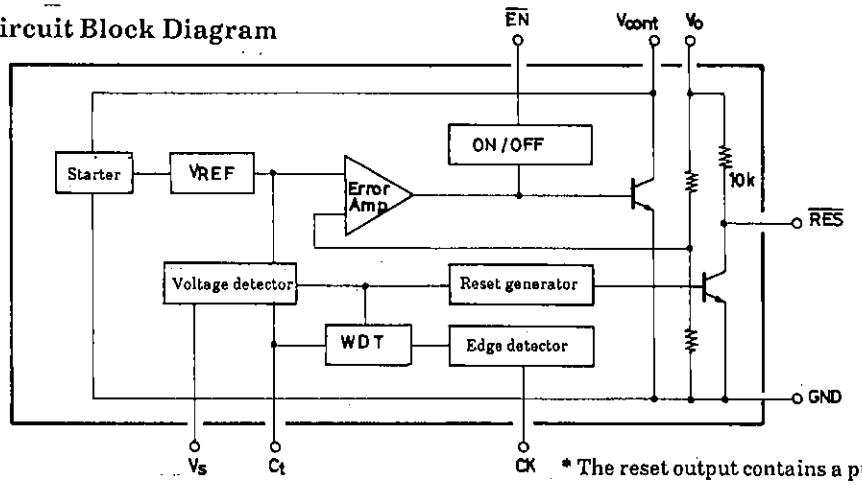
* The NC pin, which is left open, must not be used for wiring.

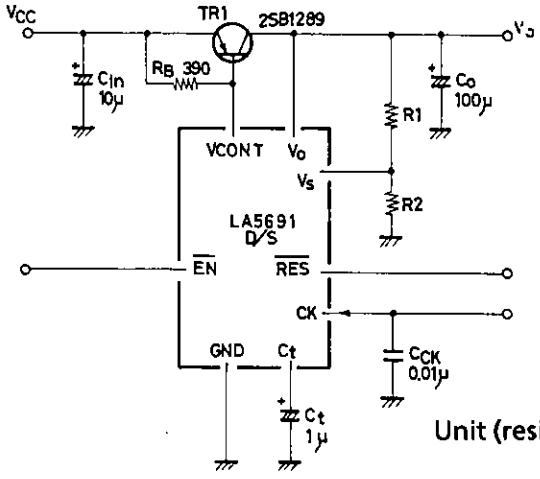
Equivalent Circuit Block Diagram



* The reset output contains a pull-up resistor of 10kΩ.

Unit (resistance: Ω)

Test Circuit

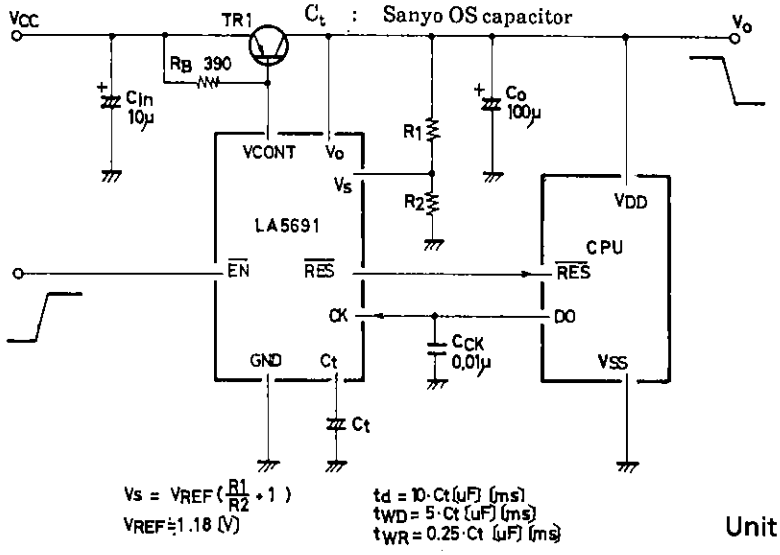


Unit (resistance: Ω, capacitance: F)

Sample Application Circuit

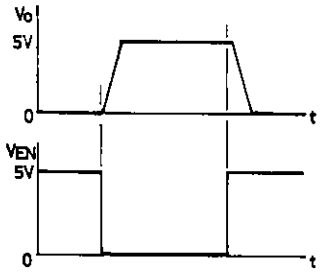
Q1 : 2SA1289 (60V/5A, TO-220)

C_t : Sanyo OS capacitor



Function Table

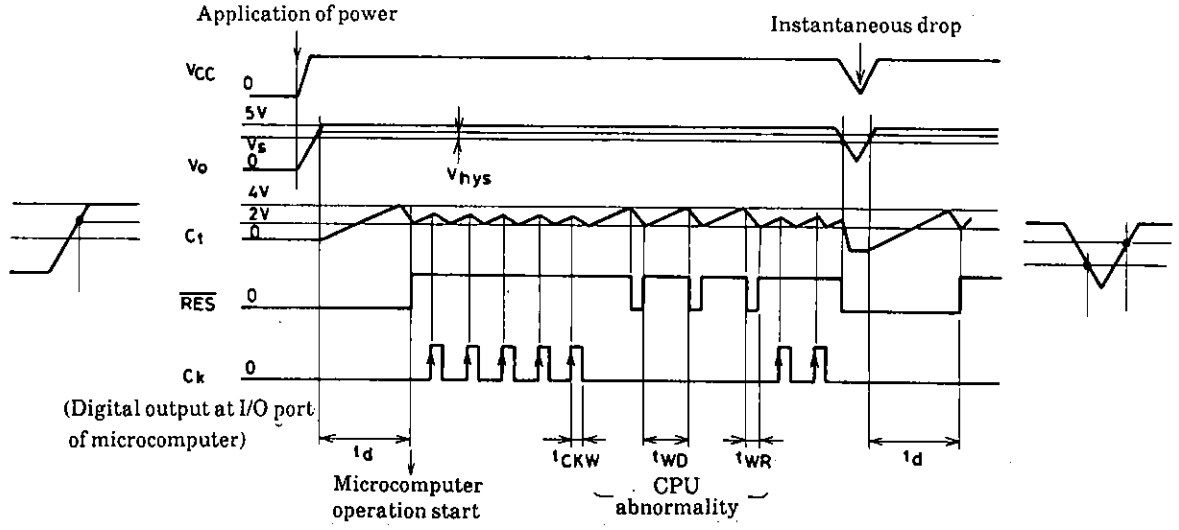
VEN	Vo
L	H
H	L



Unit (resistance: Ω, capacitance: F)

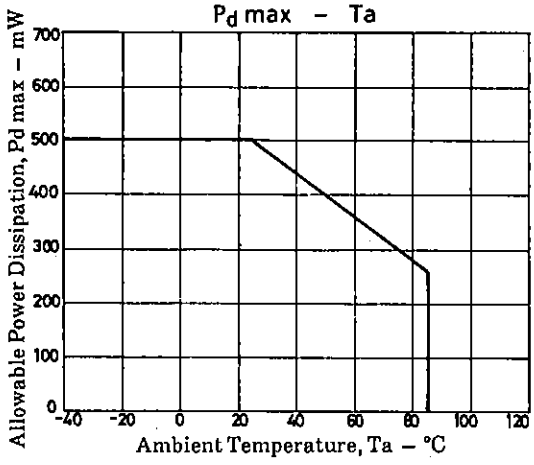
- C_t, C_O : Capacitors whose value does not vary with temperature very much.
- C_{CK} : Must be used to eliminate noise in the reset output.

Timing Chart

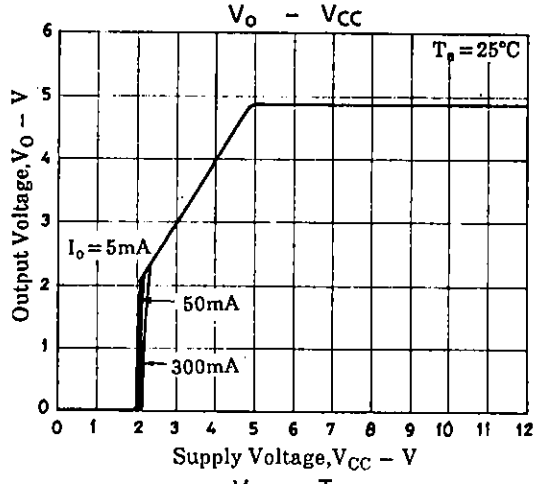


Note : Edge-triggered at the point indicated by the arrow of C_K signal.

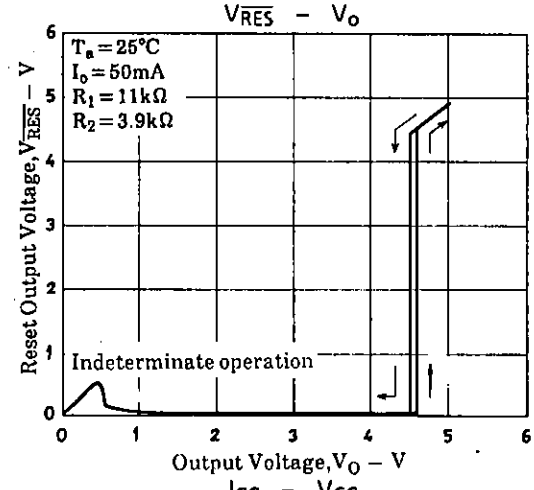
P_d max – Ta



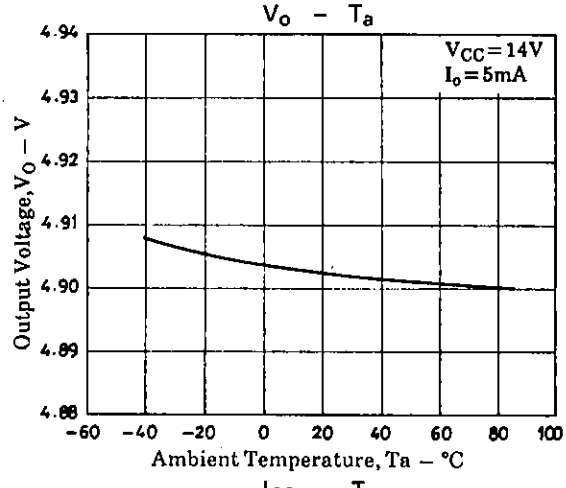
V_O – V_{CC}



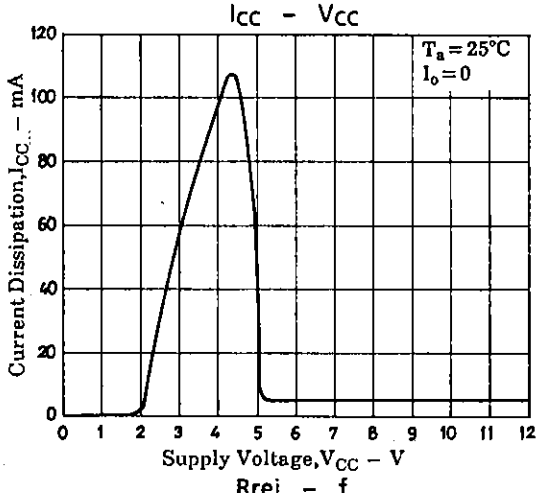
$V_{\overline{RES}}$ – V_O



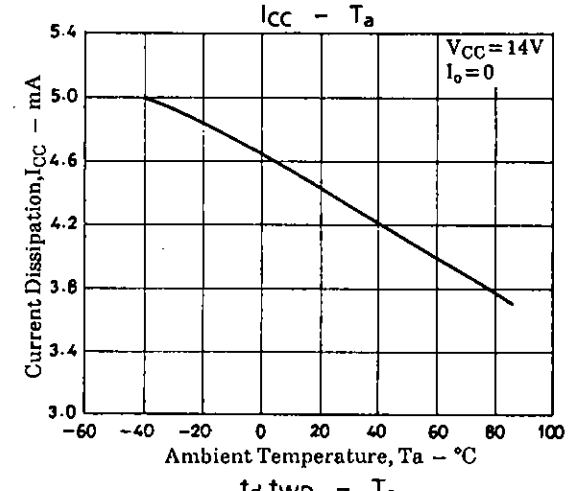
V_O – Ta



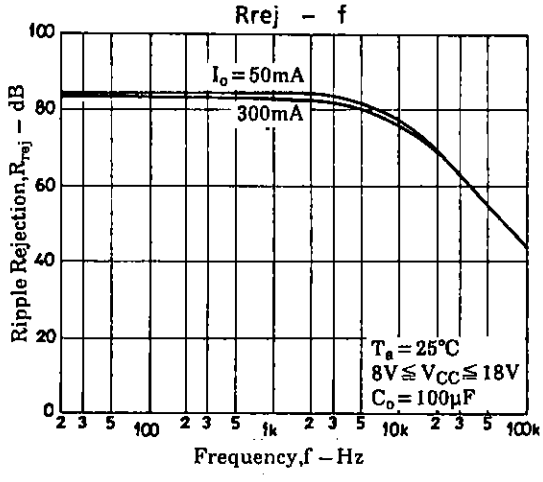
I_{CC} – V_{CC}



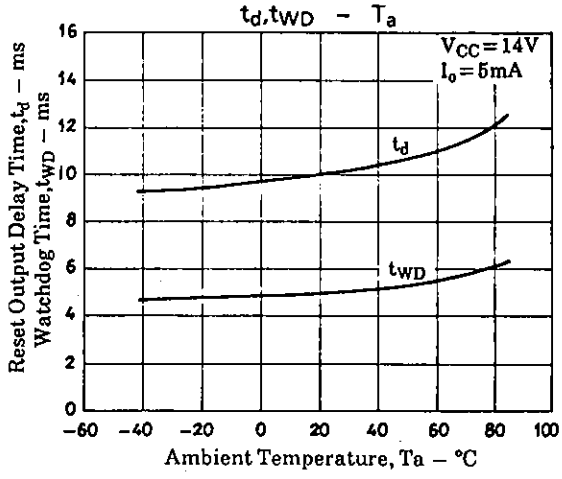
I_{CC} – Ta



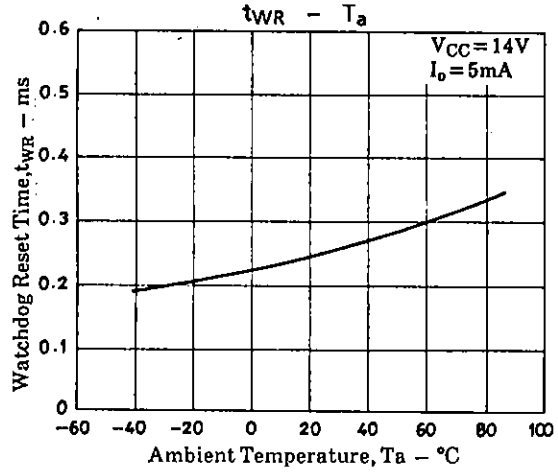
Rrej – f



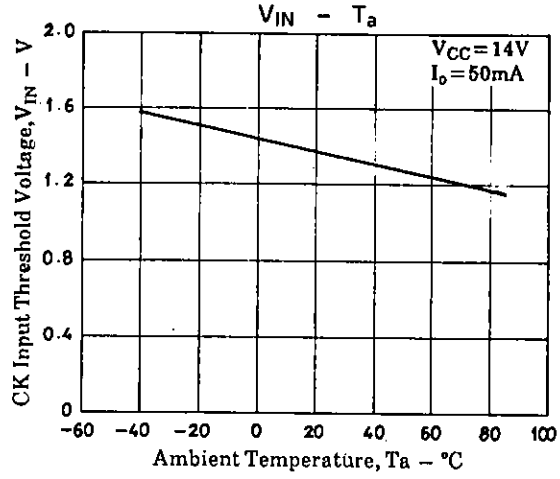
t_d, t_{WD} – Ta



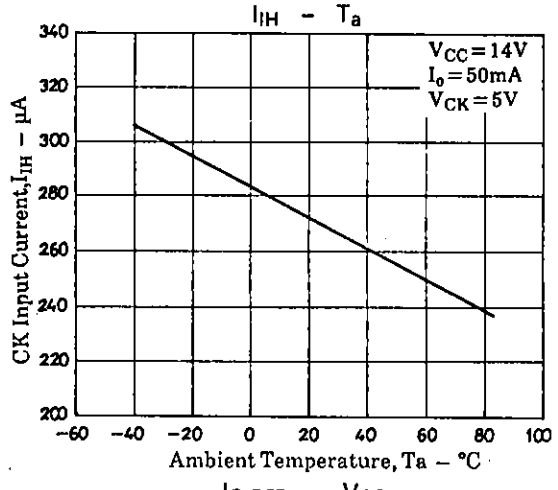
t_{WR} – T_a



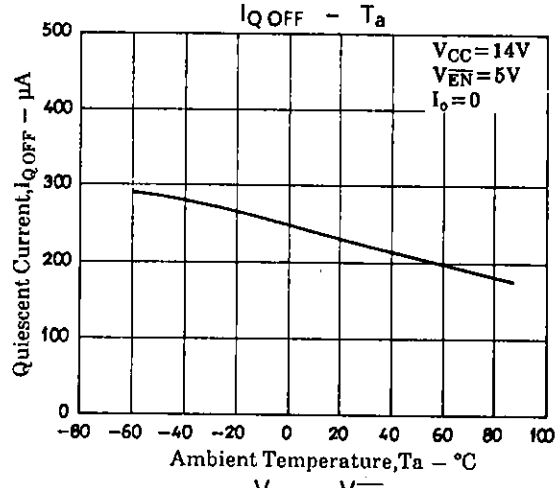
V_{IN} – T_a



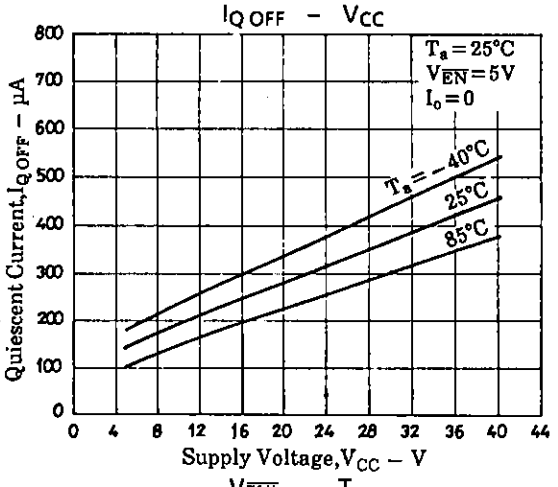
I_{IH} – T_a



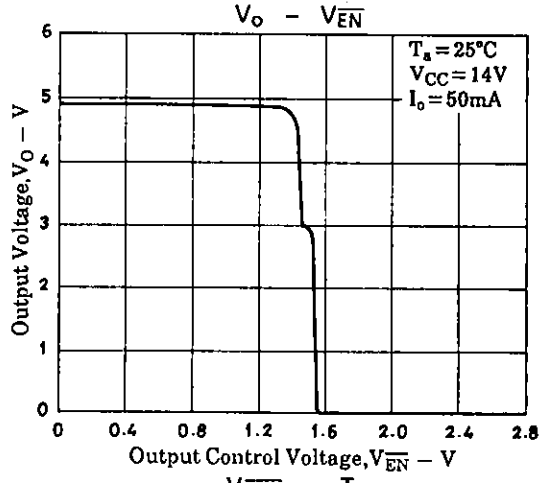
$I_{Q\,OFF}$ – T_a



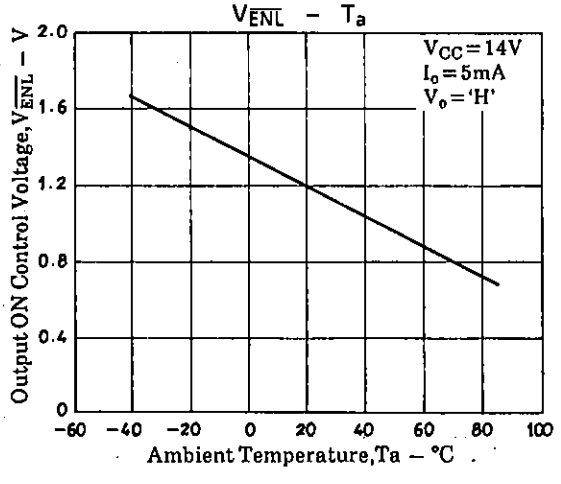
$I_{Q\,OFF}$ – V_{CC}



V_o – $V_{\overline{EN}}$



$V_{\overline{ENL}}$ – T_a



$V_{\overline{ENH}}$ – T_a