



# LA5677M

## Dual Switching Regulator Control IC

### Overview

The LA5677M supports single-input control of the outputs of two converters of arbitrary types, including step up, step down and inverting. Since the LA5677M supports low voltage (3.6 to 18 V) and high frequency (1 to 500 kHz) operation, it is ideal for use in power supplies in battery powered portable equipment.

### Features

- Operates at low voltages (3.6 to 18 V)
- Can be used with high frequency oscillators (1 to 500 kHz)
- Built-in low input malfunction prevention circuit
- Built-in timer-latch short circuit protection circuit

### Specifications

#### Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}$ max		20	V
Error amplifier input voltage	$V_I$		20	V
Collector output voltage	$V_O$		20	V
Collector output current	$I_O$		21	mA
Allowable power dissipation	$P_d$ max		330	mW
Operating temperature	$T_{opr}$		-20 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-40 to +125	$^\circ\text{C}$

#### Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Recommended supply voltage	$V_{CC}$		3.6		18	V
Error amplifier input voltage	$V_I$		1.05		1.45	V
Collector output voltage	$V_O$		-0.3		+18	V
Collector output current	$I_O$				20	mA
Feedback pin current	$I_{FT}$				45	$\mu\text{A}$
Feedback resistance	$R_{NF}$		100			$\text{k}\Omega$
Timing capacitance	$C_T$		150		15000	pF
Timing resistance	$R_T$		5.1		100	$\text{k}\Omega$
Oscillator frequency	$f_{OSC}$		1		500	kHz

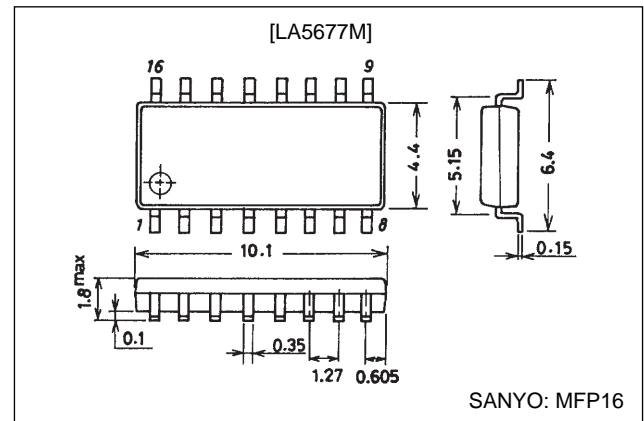
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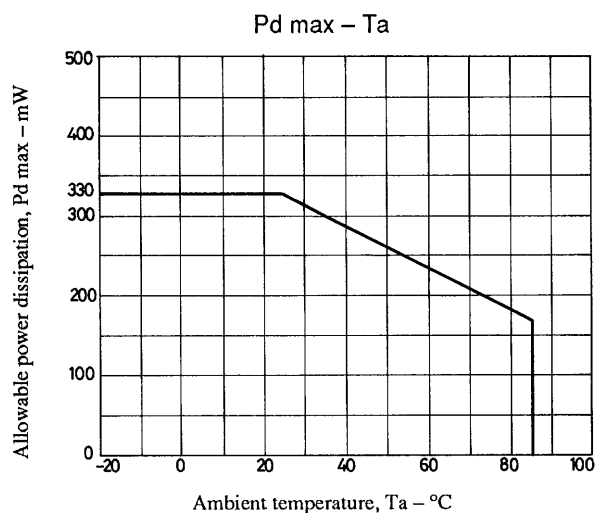
### Package Dimensions

unit: mm

#### 3035A-MFP16



## LA5677M



Parameter		Symbol	Conditions	Ratings			Unit	
				min	typ	max		
Reference voltage block	Output voltage	Vref	I <sub>OR</sub> = 1 mA	2.40	2.50	2.60	V	
	Line regulation	V <sub>line</sub>	V <sub>CC</sub> = 3.6 to 18 V		2	10	mV	
	Load regulation	V <sub>load</sub>	I <sub>OR</sub> = 0.1 to 1 mA		1	7.5	mV	
	Output voltage temperature variation				±0.2		%	
	Short circuit output current	I <sub>OSC</sub>	Vref = 0 V	3	10	30	mA	
Low input malfunction prevention block	High level threshold voltage	V <sub>tH</sub>	I <sub>OR</sub> = 0.1 mA		2.70		V	
	Low level threshold voltage	V <sub>tL</sub>	I <sub>OR</sub> = 0.1 mA		2.58		V	
	Hysteresis	V <sub>hys</sub>	I <sub>OR</sub> = 0.1 mA	80	120		mV	
	Reset voltage	V <sub>r</sub>	I <sub>OR</sub> = 0.1 mA	1.5	1.9		V	
Protection circuit block	Input threshold voltage	V <sub>tpc</sub>		1.02	1.16	1.30	V	
	Input standby voltage	V <sub>stby</sub>	No pull-up		0.78		V	
	Input latch voltage	V <sub>l</sub>	No pull-up		0.74		V	
	Input source current	I <sub>bpc</sub>	When VS.C.P is 1.0 V	12	18	27	µA	
	Comparator threshold voltage	V <sub>tc</sub>	Pins 5, 12		1.2		V	
Oscillator block	Oscillator frequency	f <sub>osc</sub>	C <sub>t</sub> = 330 pF, R <sub>t</sub> = 10 kΩ		200		kHz	
	f <sub>osc</sub> standard deviation	Δf <sub>A</sub>	All values agree		10		%	
	Frequency variation 1 (V <sub>CC</sub> )	Δf <sub>V</sub>	V <sub>CC</sub> = 3.6 to 18 V		1		%	
	Frequency variation 2 (Ta)	Δf <sub>T</sub>			±0.4		%	
Idle period adjustment circuit block	Input bias current	I <sub>bdt</sub>				1	µA	
	Latch mode source current	I <sub>dt</sub>			230		µA	
	Latch input voltage	V <sub>dt</sub>	I <sub>odt</sub> = 40 µA	2.3			V	
	Input threshold voltage	V <sub>t0</sub>	With a duty cycle of 0%		2.05	2.25		V
		V <sub>t100</sub>	f <sub>osc</sub> = 10 kHz, With a duty cycle of 100%	1.20	1.45			V

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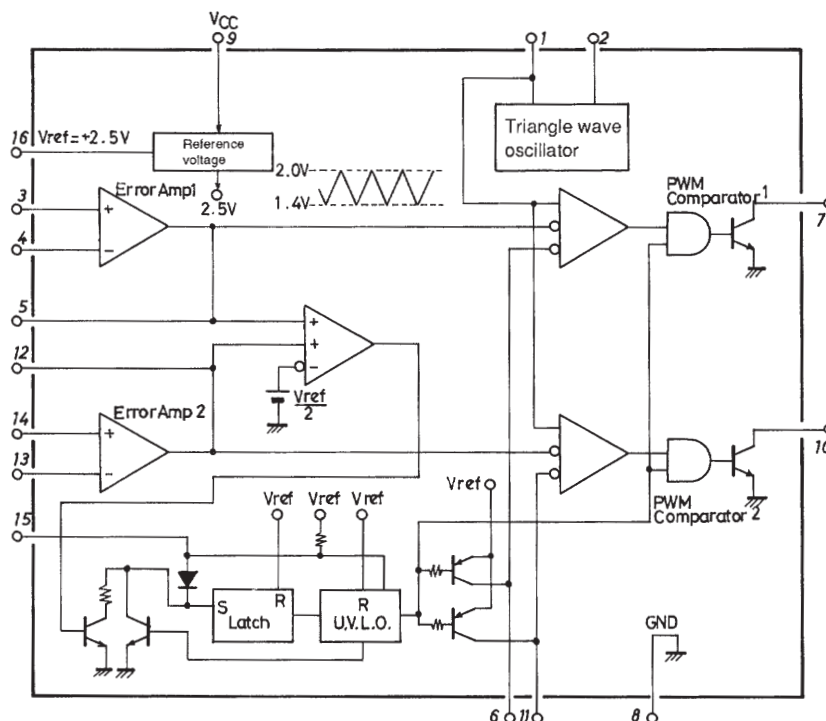
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Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Error amplifier block	Input offset voltage	$V_{IO}$	With $V$ (pins 5, 12) = 1.25 V	-6		+6	mV
	Input offset current	$I_{IO}$	With $V$ (pins 5, 12) = 1.25 V	-100		+100	nA
	Input bias current	$I_B$	With $V$ (pins 5, 12) = 1.25 V		160	500	nA
	Common mode input voltage range	$V_{ICR}$	$V_{CC} = 3.6$ to 18 V	1.05		1.45	V
	Open loop gain	$A_V$	$R_{NF} = 200$ k $\Omega$		80		dB
	Unity gain bandwidth	$G_B$			1.5		MHz
	Common mode rejection ratio	CMRR			80		dB
	Maximum output voltage amplitude (1)	$V_O + m$		$V_{ref} - 0.1$			V
	Maximum output voltage amplitude (2)	$V_O - m$				1.0	V
	Output sink current (pins 5, 12)	$I_O + m$	$V_{ID} = -0.1$ V, $V_O = 1.25$ V		1.6		mA
	Output source current (pins 5, 12)	$I_O - m$	$V_{ID} = 0.1$ V, $V_O = 1.25$ V		-70		$\mu$ A
Output block	Output leakage current	$I_{leak}$	$V_O = 18$ V			10	$\mu$ A
	Output saturation voltage	$V_{sat}$	$I_O = 10$ mA		1.0	2	V
	Short circuit output current	$I_{OS}$	$V_O = 6$ V		60		mA
PWM comparator block	Input threshold voltage	$V_{t0}$	With a duty cycle of 0%		2.05	2.25	V
		$V_{t100}$	$f_{osc} = 10$ kHz, With a duty cycle of 100%	1.20	1.45		V
	Input sink current (pins 5, 12)		With $V$ (pins 5, 12) = 1.25 V		1.6		mA
	Input source current (pins 5, 12)		With $V$ (pins 5, 12) = 1.25 V		-70		$\mu$ A
Whole device	Standby current	$I_{CC1}$	Output off state		1.6	2.2	mA
	Average supply current	$I_{CC2}$	$R_T = 10$ k $\Omega$		1.9	2.6	mA

## Pin Functions

No.	Pin	Function	No.	Pin	Function
1	$C_T$	Triangle wave oscillator capacitor connection	9	$V_{CC}$	Power supply input
2	$R_T$	Triangle wave oscillator resistor connection	10	OUT2	Output 2
3	OP1+	Error amplifier 1 + input	11	DEAD TIME2	Dead time 2 control
4	OP1-	Error amplifier 1 - input	12	OP2 <sub>OUT</sub>	Error amplifier 2 output
5	OP1 <sub>OUT</sub>	Error amplifier 1 output	13	OP2-	Error amplifier 2 - input
6	DEAD TIME1	Dead time 1 control	14	OP2+	Error amplifier 2 + input
7	OUT1	Output 1	15	S. C. P	Short circuit protection circuit connection
8	GND	Ground connection	16	$V_{ref}$	Reference voltage (2.5 V)

## Equivalent Circuit Block Diagram



## Operation Overview

### 1. Reference Voltage Block

The reference voltage block uses a 2.5 V reference voltage. This voltage is made available to external circuits from pin 16, and at the same time is used as the reference power supply by internal circuits.

### 2. Low Input Malfunction Prevention Circuit Block

The low input malfunction prevention circuit prevents incorrect operation when the power supply is brought up or during brief voltage drops. After power is applied and the reference voltage reaches  $V_{be}$ , the output transistors are held off until the power supply voltage becomes 2.72 V (typical). The dead time control pin voltage is held at the high level ( $V_{ref}$ ) and the short circuit protection pin is held low (the initial state). Since this circuit has a hysteresis of 120 mV (typical) chattering due to power supply ripple can be prevented to a certain extent.

### 3. Timer-Latch Short Circuit Protection Circuit

During output overload, the timer-latch short circuit protection circuit's short circuit protection comparator turns off Q86 when the error amplifier inputs a low level signal (a voltage less than  $V_{ref}/2$ ) to one or both of the short circuit protection comparator's two non-inverting inputs. At this time the pin 15 voltage increases from about 0.75 V (steady state) towards  $V_{ref}$  as the external capacitor is charged from  $V_{ref}$  through resistor R41 (80 k $\Omega$ ). When the capacitor is charged to about 1.2 V, the protection latch is set, the output transistors are turned off, and the idle time becomes 100%. This also turns on Q97 which resets the protection enable state. The latch circuit reset voltage is under 1.9 V (typical).

$$V_{PE1} = V_{ref} \{1 - \exp(-t1/R41 \cdot C_{PT})\}$$

$$V_{PE2} = V_{ref} \{1 - \exp(-t2/R41 \cdot C_{PT})\}$$

$$0.75 = 2.5 \{1 - \exp(-t1/80 \text{ k} \cdot C_{PT})\}$$

$$1.20 = 2.5 \{1 - \exp(-t2/80 \text{ k} \cdot C_{PT})\}$$

$$t1 = 28.56 \text{ k} \cdot C_{PT}$$

$$t2 = 52.31 \text{ k} \cdot C_{PT}$$

$$t_{PT} = t2 - t1 = 23.75 \text{ k} \cdot C_{PT}$$

$$C_{PT} = 42.1 \times t_{PT} [\mu\text{F}]$$

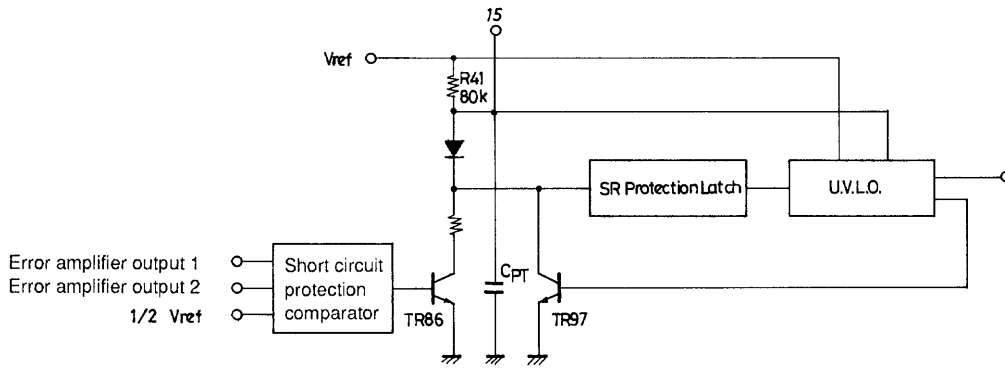


Figure 1 Timer-Latch Short Circuit Protection Circuit

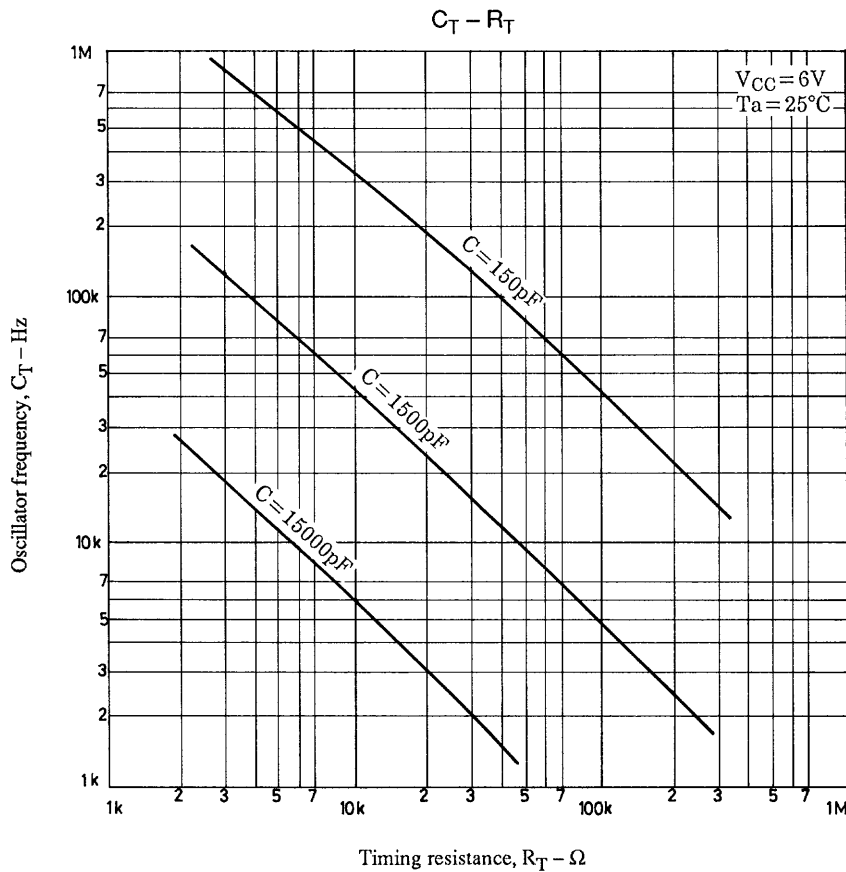


Figure 2 Timing Resistance/Oscillator Frequency Characteristics

4. Triangle Wave Oscillator Block

The triangle wave oscillator generates an essentially symmetric triangle wave using a timing capacitor and resistor attached to the  $C_T$  pin (pin 1) and the  $R_T$  pin (pin 2), respectively. The voltage amplitude is between 1.4 and 2.0 V with pin 2 stabilized at 1 V. The oscillator frequency is determined by the external capacitor and resistor.

5. Idle Period Adjustment Circuit Block

The idle period adjustment circuit consists of PWM comparators 1 and 2, each of which has one non-inverting and two inverting inputs. The output pulse width (on time) is controlled according to the input voltage. Pins 6 and 11 are dead time control pins, and are used to limit the maximum value of the pulse width. A pin voltage of 2.05 V (Typical) or over results in the output being off for the whole period, and a pin voltage of 1.45 V (Typical) or lower results in the output being on for the whole period.

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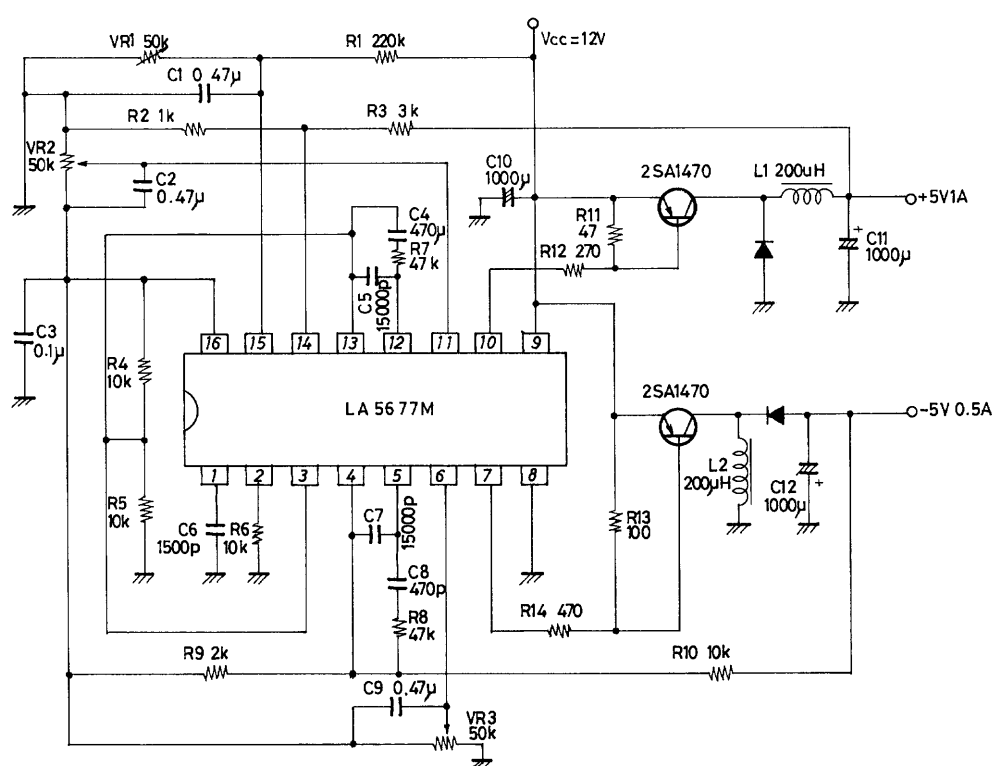
### 6. Error Amplifier Block

Error amplifiers 1 and 2 are amplifiers for detecting the output voltages, i.e., the LA5677M application system output voltages. Since the common mode input voltage range is 1.05 to 1.45 V, we recommend setting their input voltages to  $V_{ref}/2$ . Pins 5 and 12 are the output pins, and the gain is set and the frequency characteristics adjusted with a resistor and a capacitor connected between the outputs and the non-inverting inputs of each amplifier. The outputs are also connected to the short circuit protection circuit detection circuit.

### 7. Output Block

The outputs are single end open collector outputs with an NPN Darlington pair structure.

**Sample Application Circuit:** +5 V, 1 A step-down converter and -5 V, 0.5 A polarity inverting converter using a 12 V input



Unit (resistance:  $\Omega$ , capacitance: F)

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