Ordering number: EN 4145

Monolithic Linear IC

SANYO No.4145

LA5318M

Variable Divided Voltage Generator for LCD Use

Overview

The LA5318M is a valiable divided voltage generator IC for multiple drive of LCD matrix.

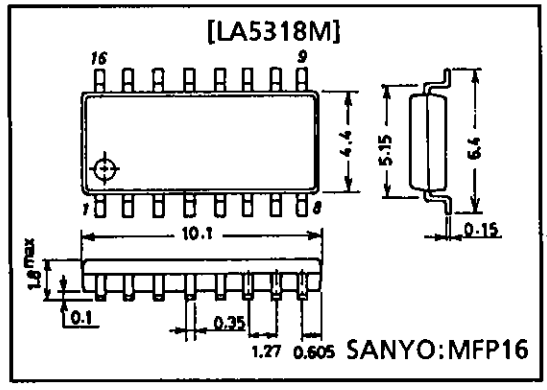
Features

- Power supply for variable bias LCD division drive (1/5 to 1/19 bias available by built-in resistances)
- Four operational amplifiers to deliver 5 voltage outputs
- Low current drain (0.35 mA typ)
- V1 , V2 output current source side variable pin
- Output on/off function V_{REF} control pins
- Miniflat package

Package Dimensions

unit : mm

3035A-MFP16



Specifications

Maximum Ratings at Ta = 25 °C

				Unit
Maximum supply voltage	V_{EE}max	V_{CC} –V_{EE}	36	V
Maximum output current	I_{OUT}max	V1 to V4	Internal *	mA
Allowable power dissipation	Pdmax		330	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–30 to +135	°C

Note: 1. Continuous operation (nonbreakdown) is guaranteed when operated at the maximum ratings shown above.
2. *The maximum output current is a value specified under the conditions otherwise specified separetely.
3. Output pins V1 to V4 to Vcc, GND short circuit not lasting more than 1ms is acceptable. ($|V_{CC} - V_{EE}| < 35V$)

Operating Conditions at Ta = 25 °C

				Unit
Supply voltage	V_{EE}	$V_{REF} \geqq V_{EE}$	–35.5 to –6	V
Input voltage	V_{REF}		–35 to –6	V
Input current	I_{INR}		–0.2 to 0	mA
Output current	I_{OUTR}		0 to +50	mA
	I_{OUT}1,2		–5 to +5	mA
	I_{OUT}3,4		–10 to +5	mA

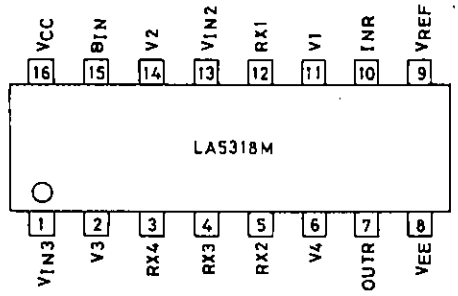
Note:4.Set V_{CC} and V_{EE} so that |V1| and $|V_{EE}$–V4| become 1V or greater.

Operating Characteristics at Ta = 25 °C, V_{CC} — V_{EE} = 20 V, V_{REF} = V_{EE}, R_X = 8R, B_{IN} = Open

				min	typ	max	Unit
Current drain		I_{CC},I_{EE}	V_{CC} –V_{EE} = 20V, R_X = 8R, INR = V_{CC}		0.35	0.5	mA
Output voltage ratio	1	Ra1	V2/V1	1.96	2.00	2.04	-
	2	Ra2	(V_{REF}—V3) / (V_{REF}—V4)	1.96	2.00	2.04	-
	3	Rb1	V_{REF} / V1	11.64	12.00	12.36	-
	4	Rb2	V_{REF}/ V2	5.82	6.00	6.18	-
	5	Rb3	V_{REF} /(V_{REF}V—3)	5.82	6.00	6.18	-
	6	Rb4	V_{REF} /(V_{REF}V—4)	11.64	12.00	12.36	-
Internal resistance ratio	1	R_X1	R_X1—R_X2 *		8		-
	2	R_X2	R_X2—R_X3 *		12		-
	3	R_X3	R_X3—R_X4 *		14		-
	4	R_X4	R_X4—V_{IN}3 *		15		-
Resistance		R	R value when 0.5V isapplied across R_X4 and V_{IN}3		30		kΩ
Load regulation	1	ΔV1	+0.1mA < I_{OUT}1 < +5mA			±20	mV
	2	ΔV2	+0.1mA < I_{OUT}2 < +5mA			±20	mV
	3	ΔV3	+0.1mA < I_{OUT}3 < +5mA			±20	mV
	4	ΔV4	+0.1mA < I_{OUT}4 < +5mA			±20	mV
	—1A	—ΔV1A	—0.5mA < I_{OUT}1 < —0.1mA			±20	mV
	—2A	—ΔV2A	—0.5mA < I_{OUT}2 < —0.1mA			±20	mV
	—3	—ΔV3	—10mA < I_{OUT}3 < —0.1mA			±20	mV
	—4	—ΔV4	—10mA < I_{OUT}4 < —0.1mA			±20	mV
	—1B	—ΔV1B	—5mA < I_{OUT}1 < —0.1mA, B_{IN} = GND			±20	mV
	—2B	—ΔV2B	—5mA < I_{OUT}2 < —0.1mA, B_{IN} = GND			±20	mV
OUTR saturation voltage		V_{OUTR}	I_{OUT} = 20mA, V_{CC}—INR = 2.7V (Source I_{OUT} is negative(—) and sink .I_{OUT} is positive(+).)			0.5	V

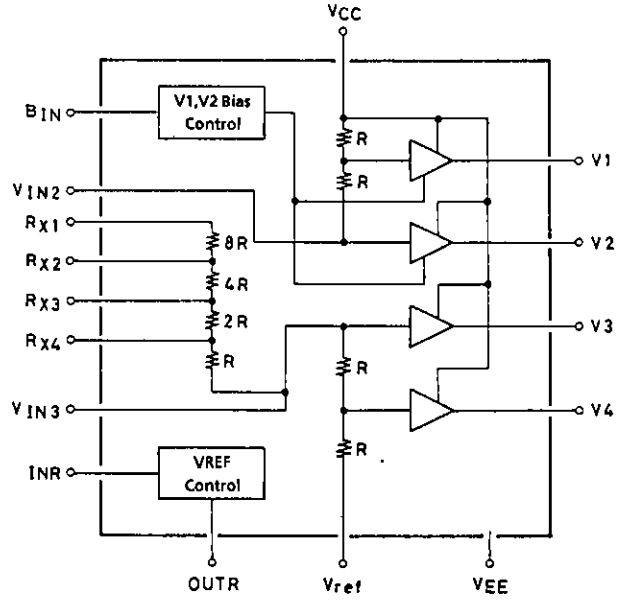
Note*: Referenced to R between R_X4 and V_{IN}3

Pin Assignment



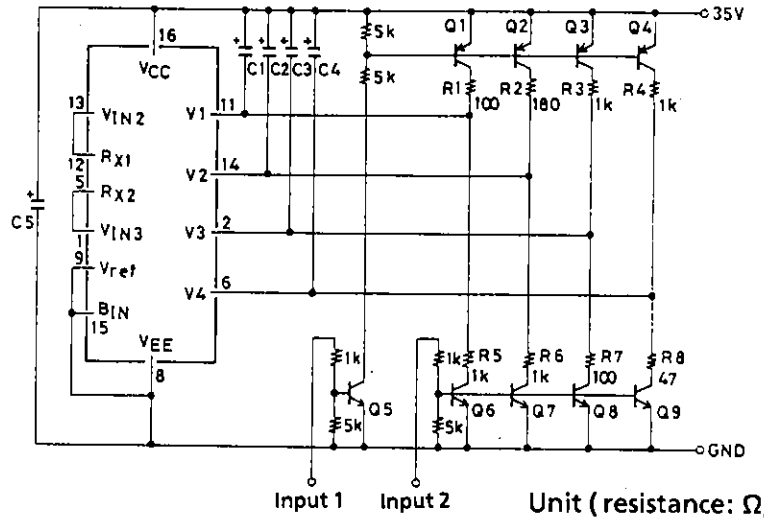
Top view

Block Diagram



Note: Use the IC so that $V_{RX}1 \geqq V_{RX}2 \geqq V_{RX}3 \geqq V_{RX}4$ must be obeyed.

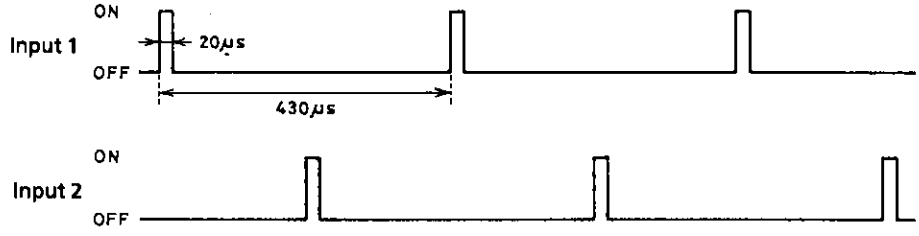
Maximum Output Current Load Test Conditions



Unit (resistance: Ω, capacitance: F)

$V_{CC} - V_{EE} = 35V$ $R_X = 8R$ C1 to C4 = 10μF C5 = 33μF R ; 1W or more
Q1 to 4 ; 2SA984 E or F rank
Q5 to 9 ; 2SC2274 E or F rank

Output load resistances R1 to R8 are set in order that current of 25 to 30 mA max. (V3, V4 source side: about 60 mA) are supplied to both source and sink sides when an on-level input is applied to the inputs 1or 2 .



V_{REF} Control Block

How to calculate the Q1 drive current

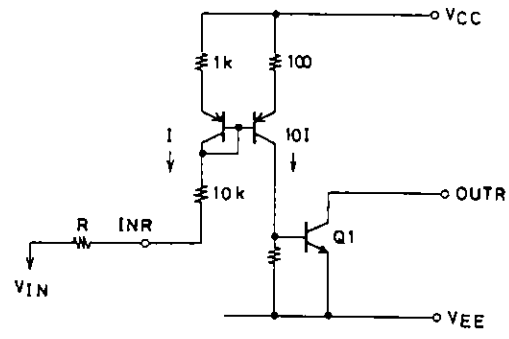
$$I = \frac{V_{CC} - V_{BE} - V_{IN}}{11k + R}$$

($V_{BE} \fallingdotseq 0.7V$)

Drive current

$$I_O \fallingdotseq 10\,I = \frac{V_{CC} - 0.7 - V_{IN}}{11k + R} \times 10$$

Q1 h_{FE} is assumed to be 50.



Unit (resistance: Ω)

*Set V_{CC} = INR when INR and OUTR are not used.