Ordering number: EN5204A

Monolithic Linear IC

LA4587M

Preamplifier + Power Amplifier for 1.5 V Headphone Stereos

Overview

The LA4587M is a system IC that includes all of the necessary functions for a playback set on a single chip, reducing the number of external components needed.

Functions

- Stereo preamplifier (supports auto reverse function, switchable between metal and normal tape)
- Stereo power amplifier (OCL, mute function)
- Ripple filter
- Low boost function (BTL operation in low-frequency range)
- AMSS (Automatic Music Select System)
- Power switch

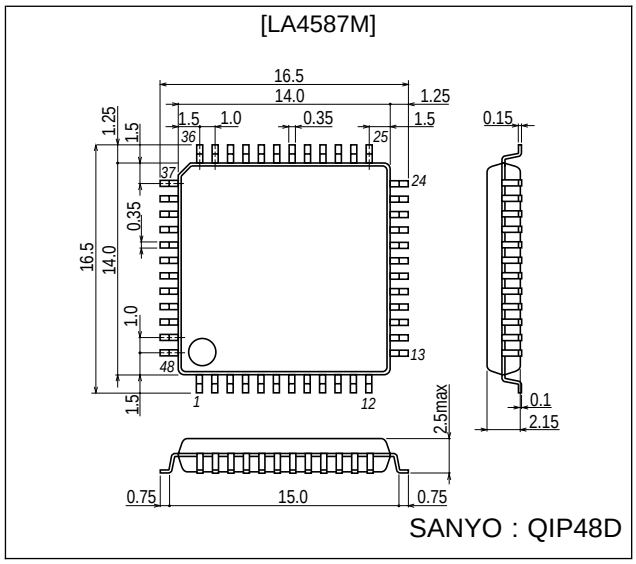
Features

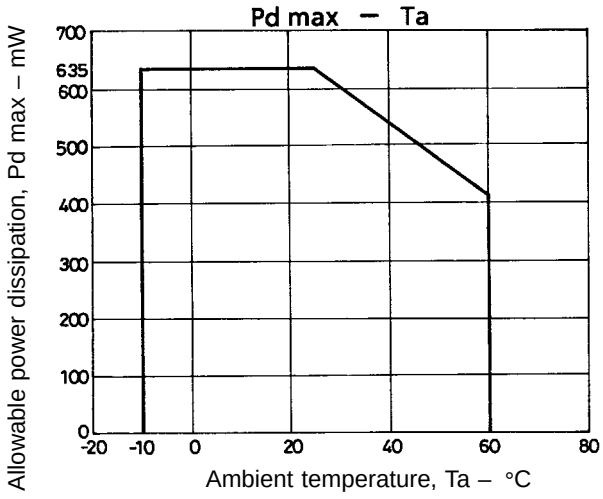
- Preamplifier has a high open-loop gain (VG_O = 73 dB).
- Preamplifier requires no NF capacitor.
- Virtual ground capacitor can be 1 µF or less. (Lower impedance is achieved by having a V_{REF} amplifier built in.)
- Ripple filter requires no capacitor for preventing oscillation.
- Powerful output is obtained in low boost output (Po = 21 mW/V_{CC} = 1.2 V, f = 100 Hz).
- A high-frequency cutoff capacitor is built into the preamplifier and power amplifier inputs; anti-buzz provision.

Package Dimensions

unit : mm

3102-QIP48D





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Specifications

Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		3.0	V
Allowable power dissipation	Pd max		635	mW
Operating temperature	Topr		–10 to +60	°C
Storage temperature	Tstg		–40 to +125	°C

Operating Conditions at Ta = 25 °C

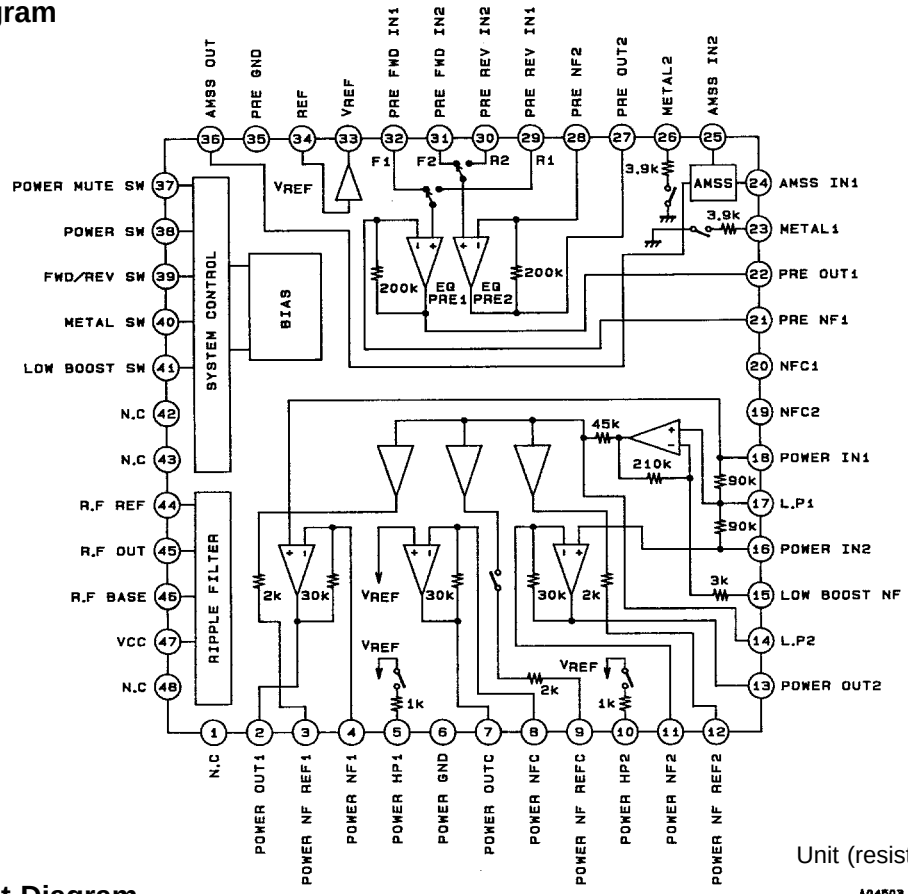
Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		1.5	V
Operating supply voltage range	V_{CC} op		0.95 to 2.2	V

Operation Characteristics at Ta = 25 °C, V_{CC} = 1.2 V, f = 1 kHz, 0.775 V = 0 dBm, R_L = 10 kΩ (preamplifier), R_L = 16 Ω (power amplifier)

Parameter	Symbol	Conditions	min	typ	max	Unit
[Preamplifier + Power Amplifier]						
Quiescent current	$I_{CCO}1$	Rg = 2.2 kΩ, Rv = 0 Ω	8	15	24	mA
	$I_{CCO}2$	When power switch is off		0.1	5	μA
Voltage gain (closed)	VG_T	V_O = –20 dBm, R_V = 10 kΩ	54	57	60	dB
[Preamplifier]						
Voltage gain (open)	VG_0	V_O = –20 dBm	60	73		dB
Voltage gain (closed)	VG_1	V_O = –20 dBm	34	35.5	37	dB
	VG_2	V_O = –20 dBm, f = 10 kHz, metal on	25.5	28	30.5	dB
Maximum output voltage	V_O max	THD = 1 %	100	210		mV
Total harmonic distortion	THD_1	VG = 35.5 dB/NAB, V_O = 100 mV		0.1	0.5	%
Equivalent input noise voltage	V_{NI}	Rg = 2.2 kΩ, BPF: 20 Hz to 20 kHz		1.3	3.0	μV
Interchannel crosstalk	CT_1	Rg = 2.2 kΩ, 1 kHz TUNE, V_O = –20 dBm	45	56		dB
Interchannel crosstalk between F and R	CT_2	Rg = 2.2 kΩ, 1 kHz TUNE, V_O = –20 dBm	65	78		dB
Ripple rejection ratio	Rr1	Rg = 2.2 kΩ, Vr = –30 dBm, fr = 100 Hz, 100 Hz TUNE	45	52		dB
[Low Boost + Power Amplifier]						
Voltage gain (closed)	VG_3	V_O = –20 dBm	20.5	23	25.5	dB
	VG_4	V_O = –20 dBm, L.B. = on	20.5	23	25.5	dB
	VG_5	V_O = –20 dBm, L.B. = on, f = 10 kHz	24.5	27.5	30.5	dB
	VG_6	V_O = –20 dBm, L.B. = on, f = 100 Hz	30	34	38	dB
Output power	P_{O1}	THD = 10 %	5	9		mW
	P_{O2}	THD = 10 %, f = 100 Hz, L.B. = on	13	21		mW
Total harmonic distortion	THD_2	P_O = 1 mW		0.5	1.5	%
Interchannel crosstalk	CT_3	V_O = –20 dBm, R_V = 0 Ω	38	43		dB
Output noise voltage	V_{NO}	R_V = 0 Ω, BPF: 20 Hz to 20 kHz		35	48	μV
Ripple rejection ratio	Rr_2	R_V = 0 Ω, Vr = –30 dBm, fr = 100 Hz, 100 Hz TUNE	50	74		dB
Output mute voltage	V_M	V_{IN} = –30 dBm, 1 KHz TUNE, mute on			–85	dBm
Input resistance	Ri		8	10	12	kΩ
Voltage gain difference	ΔVG_3			0	+1.5	dB
[Ripple Filter]						
Ripple rejection ratio	Rr_3	fr = 100 Hz, Vr = –30 dBm, V_{CC} = 1.0 V, I_{RF} = 25 mA, 2SB1295, h_{FE}6 rank used	33	39		dB
Output voltage	V_{RF}	V_{CC} = 1.0 V, I_{RF} = 25 mA	0.89	0.93		V
[AMSS]						
Operating output voltage	V_{OAMSS}	Preout voltage when AMSS V_O = 0.6 Vp-p Pin 34 is short-circuited through 270 kΩ.	1.80	2.55	3.60	mV

Note: L.B. = Low boost

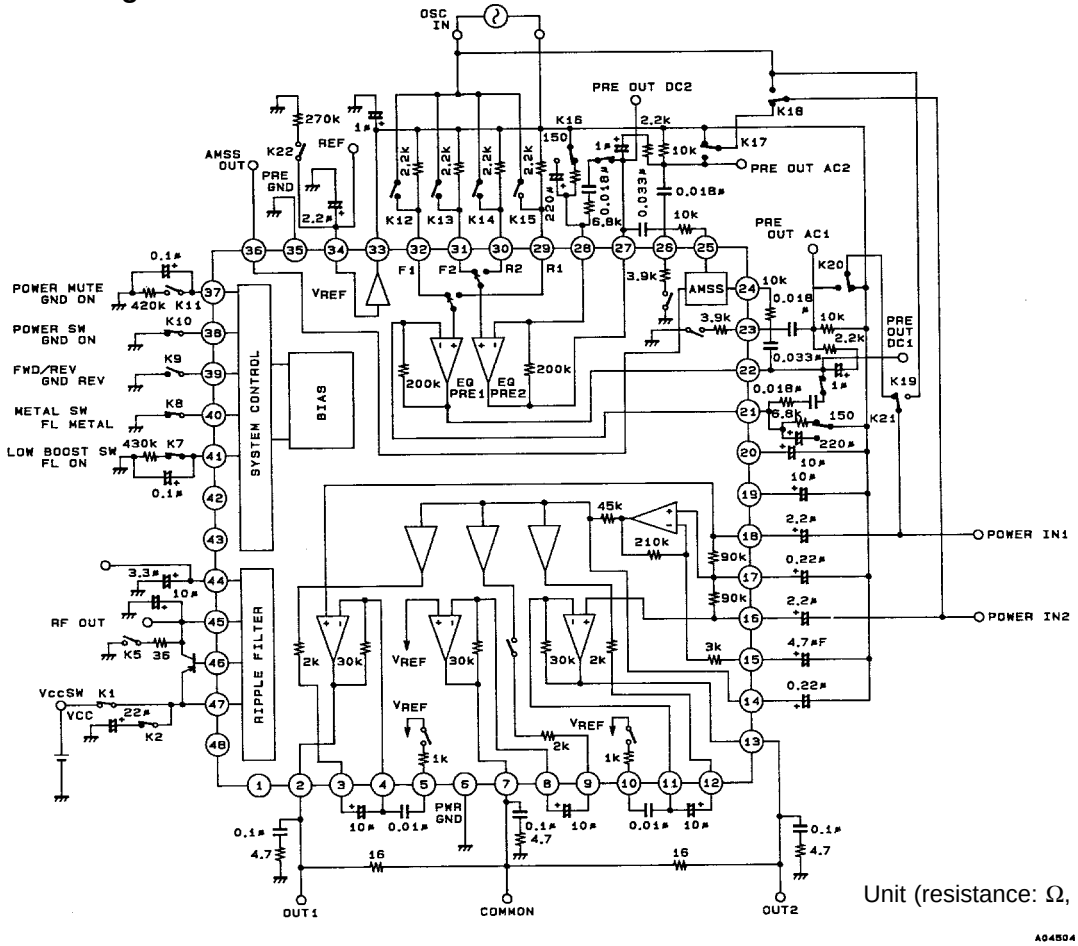
Block Diagram



Unit (resistance: Ω)

A04503

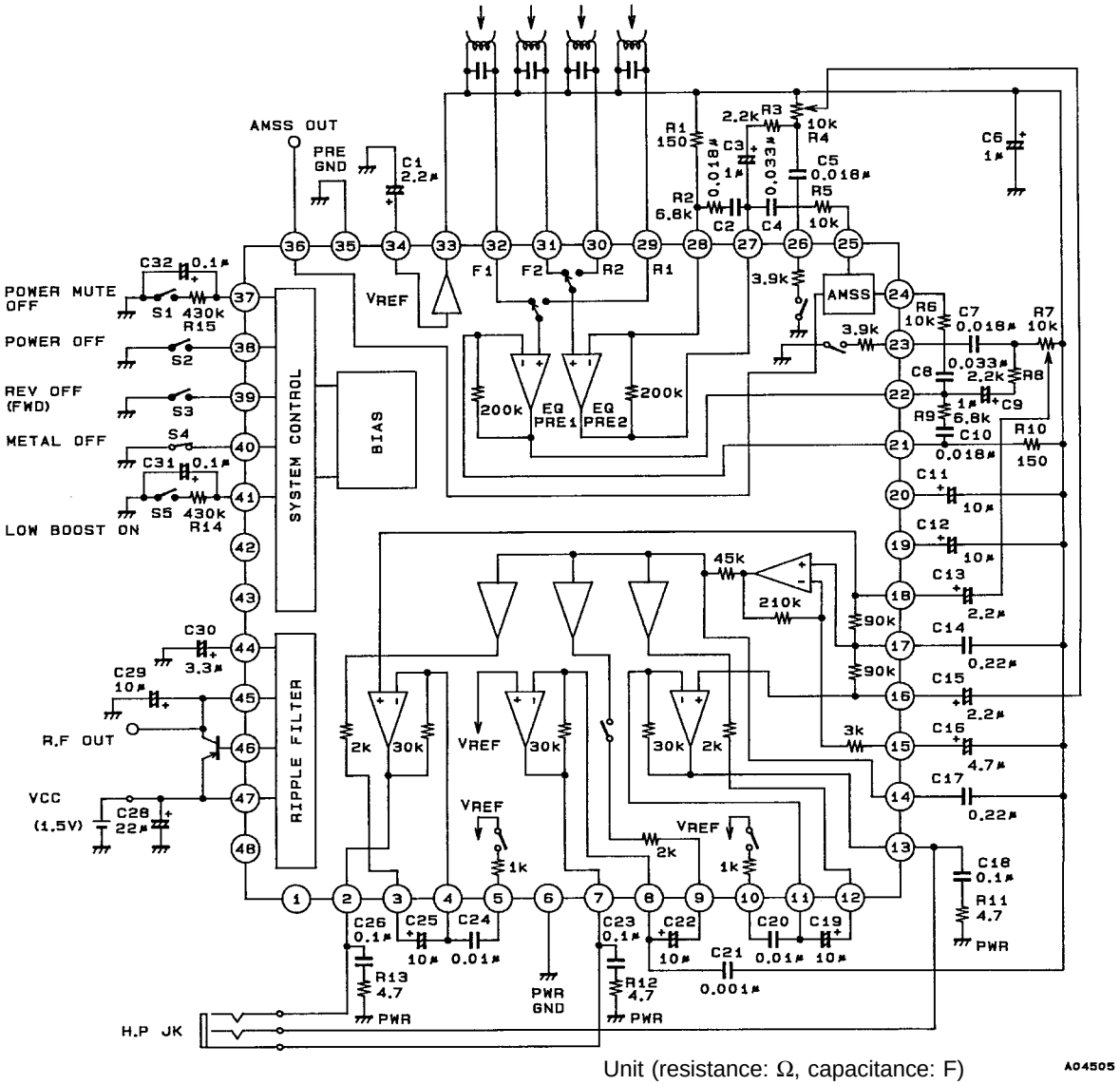
Test Circuit Diagram



Unit (resistance: Ω, capacitance: F)

A04504

Sample Application Circuit



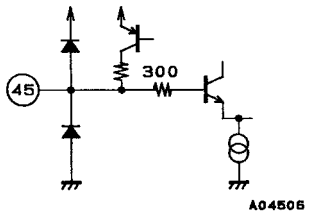
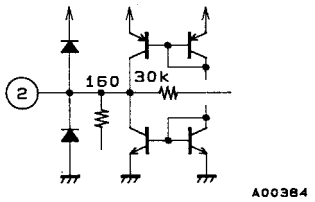
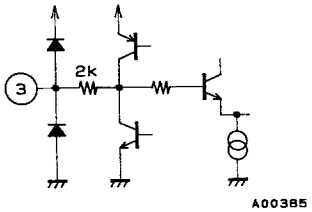
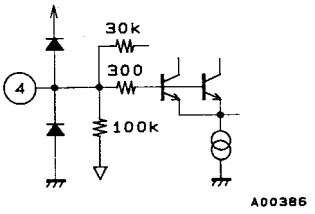
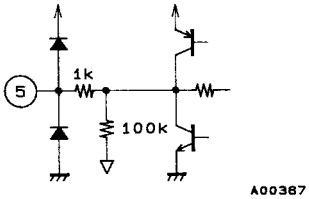
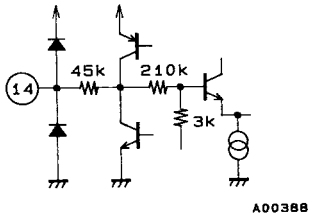
Unit (resistance: Ω, capacitance: F) A04505

Note 1: Transistors equivalent to the 2SB1295 with h_{FE}6 rank and upward are recommended.

Note 2: C18, C23, and C26 are oscillation prevention capacitors; a polyester film or ceramic capacitor (which can guarantee the specified capacitance at operating temperatures) is recommended.

Pin Functions

Unit (resistance:Ω, capacitance: F) * Pin voltage is when V_{CC} = 1.2 V

Pin No.	Pin name	Pin voltage [V]	Internal equivalent circuit	Remarks
45	R.F OUT	1.13		
2 7 13	POWER OUT1 POWER OUTC POWER OUT2	0.6		• A 160 Ω resistor is connected between individual outputs (between pins 2 and 7, and between pins 13 and 7).
3 9 12	POWER NF REF1 POWER NF REFC POWER NF REF2	0.75		• Each power NF connection
4 8 11	POWER NF1 POWER NFC POWER NF2	0.75		• Each power NF connection.
5 10	POWER H.P1 POWER H.P2	0.75		• Grounded to V_{REF} through a 1 kΩ resistor when low boost is on (pin 41: floating).
14	L.P2	0.75		• Low boost secondary LP connection.

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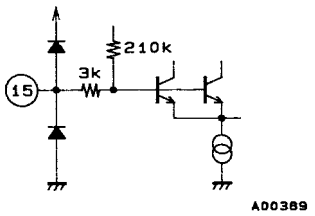
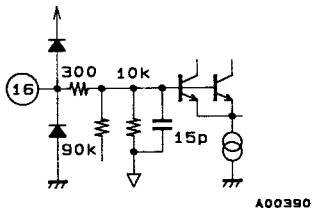
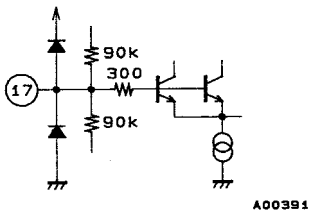
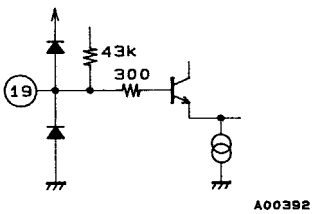
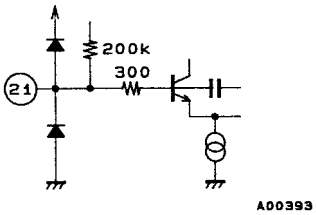
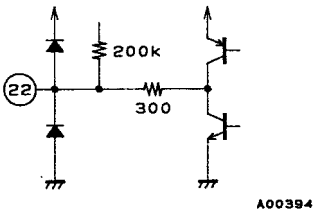
Pin No.	Pin name	Pin voltage [V]	Internal equivalent circuit	Remarks
15	Low Boost NF	0.75		• Low boost amplifier NF connection.
16 18	POWER IN2 POWER IN1	0.75		• Each power input connection. • The input resistance is 10 kΩ. • An anti-buzz capacitor is built in.
17	L.P1	0.75		• Low boost primary LP. connection.
19 20	NFC2 NFC1	0.75		
21 28	PRE NF1 PRE NF2	0.75		• Each preamplifier NF connection. • NF requires no capacitor.
22 27	PRE OUT1 PRE OUT2	0.45		• 200 kΩ is connected between each output pin and NF pin.

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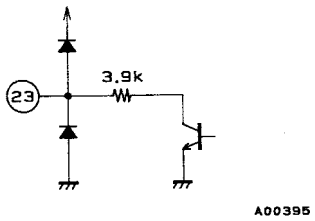
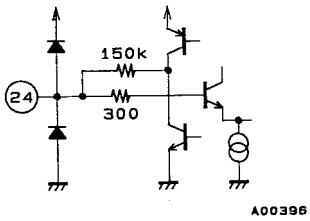
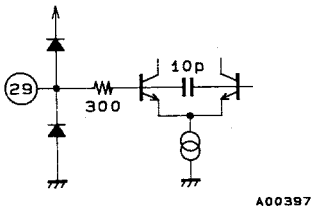
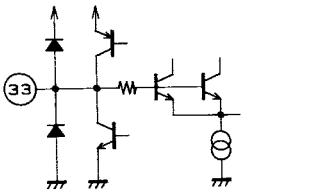
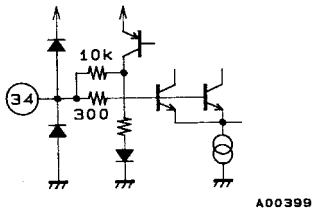
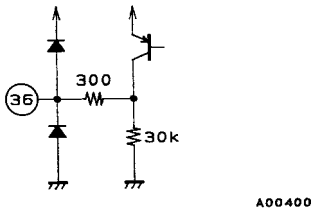
Unit (resistance: Ω, capacitance: F)

Pin No.	Pin name	Pin voltage [V]	Internal equivalent circuit	Remarks
23 26	METAL1 METAL2	0		• Connected to GND through 3.9 kΩ in metal on mode (pin 40: floating)
24 25	AMSS IN1 AMSS IN2	0.75		• AMSS inverting input connection. • An external input resistor is required.
29 30 31 32	PRE REV IN1 PRE REV IN2 PRE FWD IN2 PRE FWD IN1	0.75		▪ Pins 29 and 30 turn on in REV mode (pin 39: GND). • Pins 31 and 32 turn on in FWD mode (pin 39: floating) • When not using the head, a bias resistor (2.2 kΩ) is required between these pins and V_{REF} (pin 33). • An anti-buzz capacitor is built in.
33	V_{REF}	0.75		• V_{REF} amplifier output. Low impedance is achieved due to the output resistor (ro = 10 Ω). • Inflow/outflow current: 200 μA max.
34	REF	0.75		• The V_{REF} amplifier is referenced hereto.
36	AMSS OUT			• Outputs a pulse waveform in accordance with the AMSS IN (pins 24 and 25) input level.

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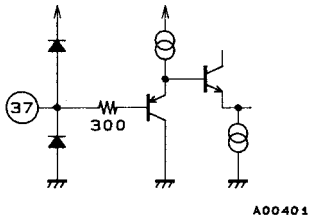
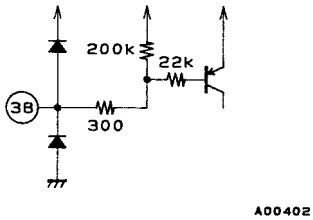
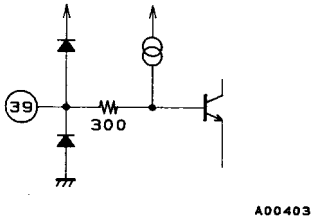
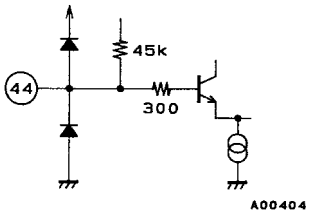
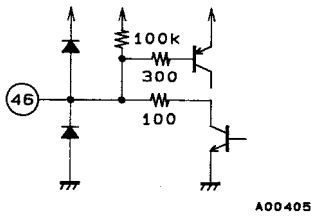
Continued from preceding page. Unit (resistance: Ω, capacitance: F)

Pin No.	Pin name	Pin voltage [V]	Internal equivalent circuit	Remarks
37 41	POWER MUTE SW Low Boost SW			• When pin 37 is grounded, mute is on. • When pin 41 is floating, low boost is on.
38	POWER SW			• Power on when grounded.
39 40	FWD/REV SW METAL SW			• When pin 39 is floating: FWD mode; when grounded: REV mode. • When pin 40 is in FL mode: metal on.
44	R.F REF	1.13		• RF is referenced hereto. An external capacitor can be used to vary RF SVRR.
46	R.F BASE	0.5		• Used for external PNP transistor base drive.

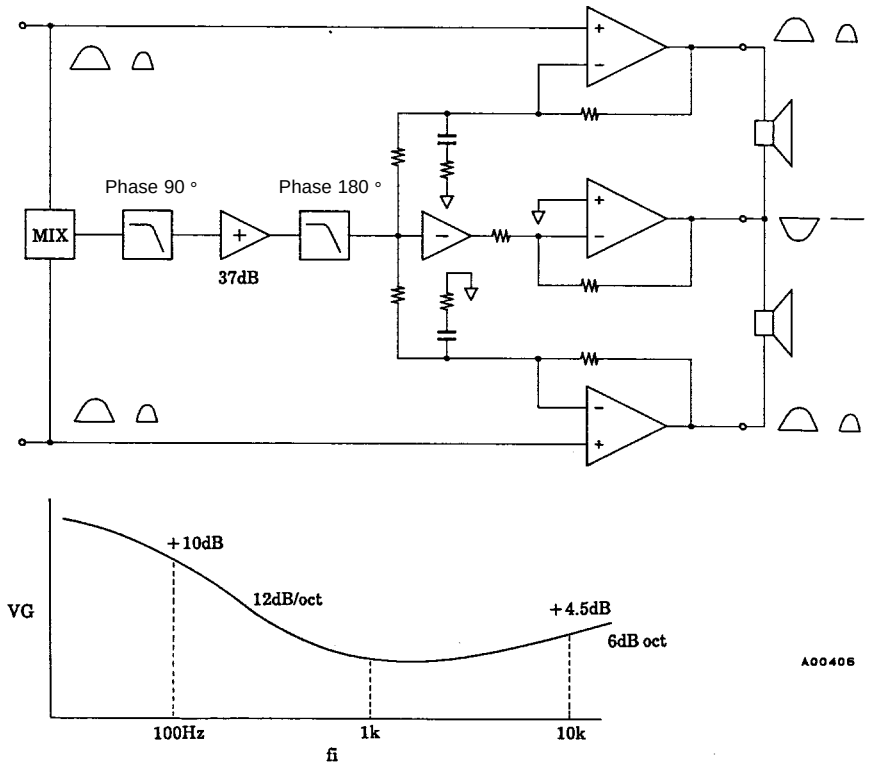
Description of External Components

- C_1 (1.0 to 10 µF): V_{REF} amplifier is referenced to this decoupling capacitor. The V_{REF} SVRR depends on the value of this capacitor. Note that if the capacitance is reduced, the SVRR worsens.
- C_2, C_{10}: Playback preamplifier EQ constant.
- C_3, C_9 (0.47 to 3.3 µF): Preamplifier output capacitor.
- C_4, C_8: AMSS input HPF capacitor.
- C_5, C_7: EQ constant for metal (built-in resistance 3.9 kΩ ±15%).
- C_6 (0.1 to 22 µF): V_{REF} decoupling capacitor. For high-frequency noise rejection.
- C_{11}, C_{12} (3.3 to 10 µF): NFC decoupling capacitor. Note that if the capacitance is reduced, the preamplifier low-frequency gain decreases.
- C_{13}, C_{15} (1.0 to 3.3 µF): Power amplifier input capacitor (Input resistance: 10 kΩ).
- C_{14}, C_{17}: Capacitor for low boost LPF. The low boost gain depends on the capacitance.
- C_{16} (1.0 to 4.7 µF): Boost amplifier NF capacitator. Note that if the capacitance is reduced, the low boost low-frequency gain decreases.
- C_{18}, C_{23}, C_{26} (0.1 to 1.0 µF): Oscillation blocking capacitator.
- C_{19}, C_{22}, C_{25} (3.3 to 10 µF): Power amplifier NF capacitor. Note that if the capacitance is reduced, the power amplifier low-frequency gain decreases.
- C_{20}, C_{24}: Bass high boost capacitor. The high gain depends on the capacitance.
- C_{21} (100 to 2200 pF): Oscillation blocking capacitator.
- C_{29} (4.7 to 10 µF): RF output decoupling capacitor. (Also serves as the power supply capacitor and the oscillation blocking capacitor.)
- C_{28} (22 to 220 µF): Power supply capacitor.
- C_{30} (2.2 to 10 µF): RF is referenced to this LPF capacitor. The RF SVRR depends on the capacitance.
- C_{31}, C_{32} (0.047 to 0.22 µF): Switching circuit smoothing capacitor. Must be adjusted according to the set timing.
- R_1, R_{10}: For preamplifier gain adjustment.
- R_2, R_9: Playback preamplifier EQ constant.
- R_3, R_8: EQ constant for metal.
- R_4, R_7: 10 kΩ volume control.
- R_5, R_6: For AMSS gain adjustment and HPF.
- R_{11}, R_{12}, R_{13}: For oscillation blocking.
- R_{14}, R_{15} (100 to 430 kΩ): For switching circuit smoothing (discharge resistors).

Operation Descprition

- Low boost system

  Low-frequency region amplification: 12 dB/oct, high-frequency region amplification: 6 dB/oct.



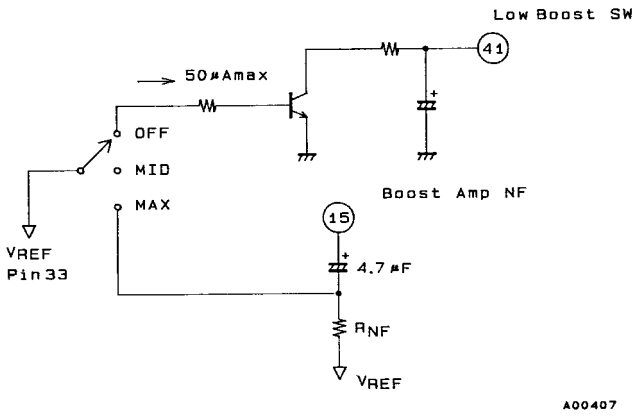
- Note on low boost
  The signals that are applied to each power input are mixed and then passed through a two-stage LPF. Because the signal levels are attenuated by the LPF, level compensation is accomplished by amplifying the signals through a low boost amplifier located in between. The phase of signals that pass through the secondary LPF is inverted relative to the input signal; these signals are then input to each power amplifier.

- Note on channels 1 and 2
  The positive phase signals that were input from the positive (“+”) input pins and the reverse phase signals that were input from the negative (“–”) input pins and then were passed through the secondary LPF are all input, amplified, and then output.

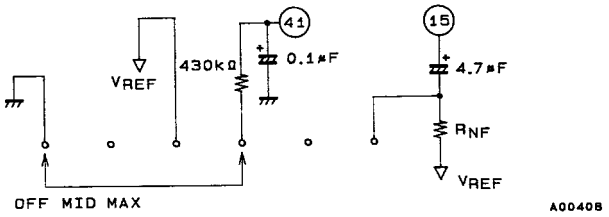
- Note on the common amplifier
  The phase of the signals that passed through the secondary LPF is inverted by the inverting amplifier; the signals (with reversed phases relative to channels 1 and 2) are then input to the negative (“–”) inputs. The positive (“+”) input signals are grounded to V_{REF}, amplified by the inverting amplifier and then output.
  The phase of the channel 1 and 2 amplifier outputs and the common amplifier outputs are made to oscillate with inverted phases, making it possible to obtain the dynamic range efficiently.

Sample Application Circuits for Low Boost Switching

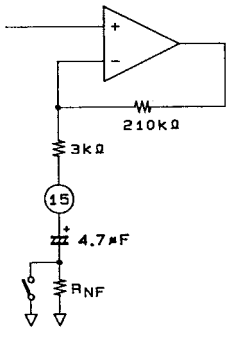
Sample 1



Sample 2

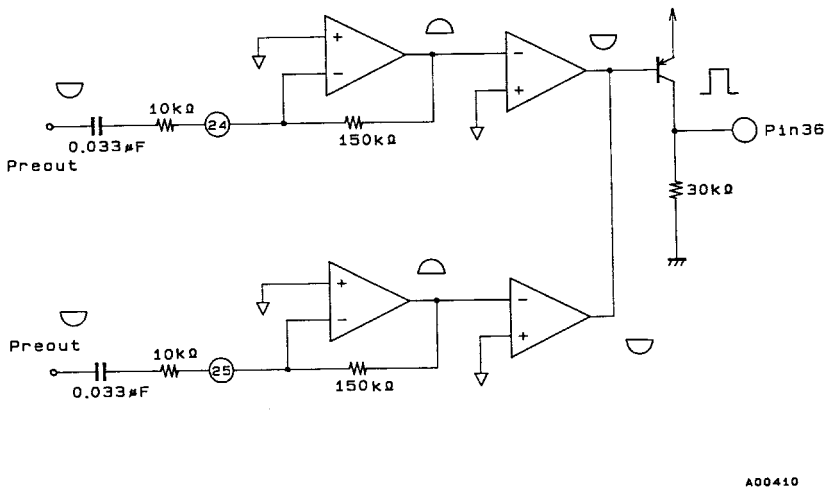


In the above circuits, MID and MAX are switched by changing the gain of the boost amplifier.



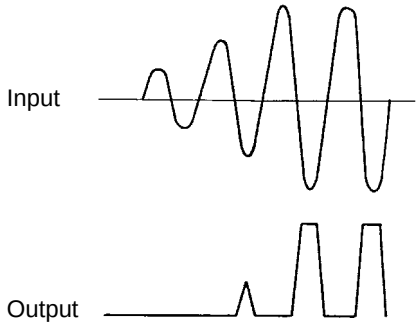
The AMSS comparator

Block Diagram



Operation Description

- The input amplifiers are inverting amplifiers. The gain and HPF characteristics can be adjusted through an external C-R (input impedance).
- The AMSS comparator outputs pulses for an input waveform that satisfies certain set conditions (frequency and voltage level).



- When AMSS is not used, the input pins (pins 24 and 25) are connected to V_{REF} (pin 33).

Notes on the ripple filter

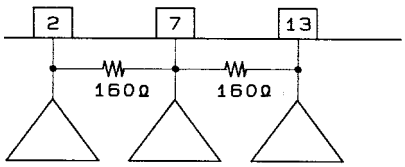
- The RF SVRR can be adjusted by an external capacitor connected to pin 44.

  3.3 µF → 39 dB
  4.7 µF → 42 dB
  10 µF → 47 dB

- It is recommended that external transistors be equivalent to the 2SB1295 with h_{FE} 6 rank and upward.

Note on power output

- The power amplifier output and the common amplifier output are connected by a resistor of approximately 160 Ω.



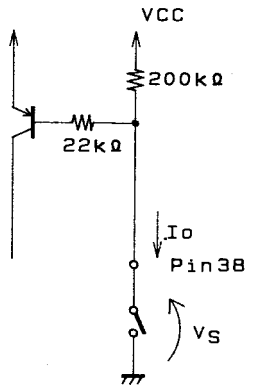
A00411

Notes on power mute

- Power mute turns off the fixed current that is supplied to the power section.
- The output DC when power mute is on is the V_{REF} electric potential (0.75 V).
- The output impedance when power mute is on is approximately 10 kΩ.

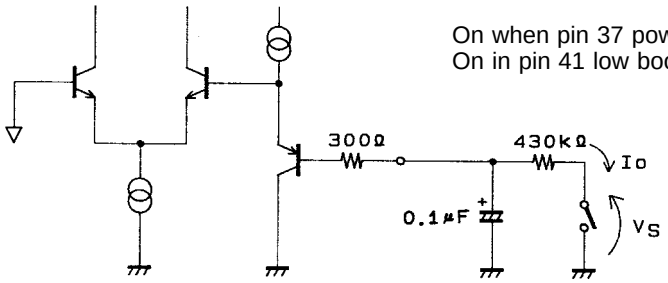
SW Pin Equivalent Circuit Diagram

1. Power switch



On when power switch is grounded
I_O = V_{CC}/200 k + V_{CC} – 0.7 V/22 kΩ
Pin 38
V_S = 100 mV or less

2. Power mute and low boost switch

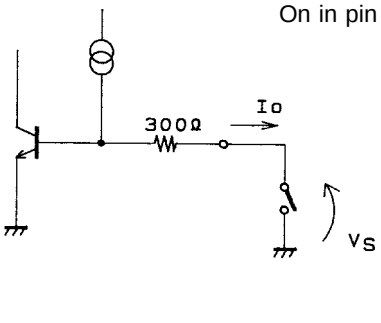


On when pin 37 power mute is grounded
On in pin 41 low boost switch floating mode

I_O = 0.1 μA or less
V_S = 80 mV or less

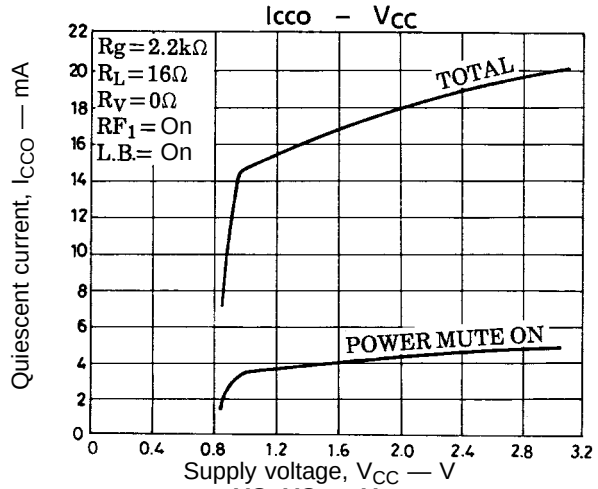
* The discharge resistance for smoothing is 430 kΩ max.

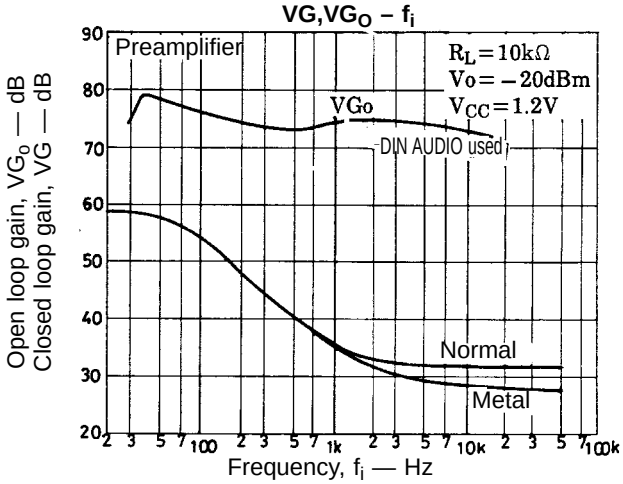
3. FWD/REV, METAL switch

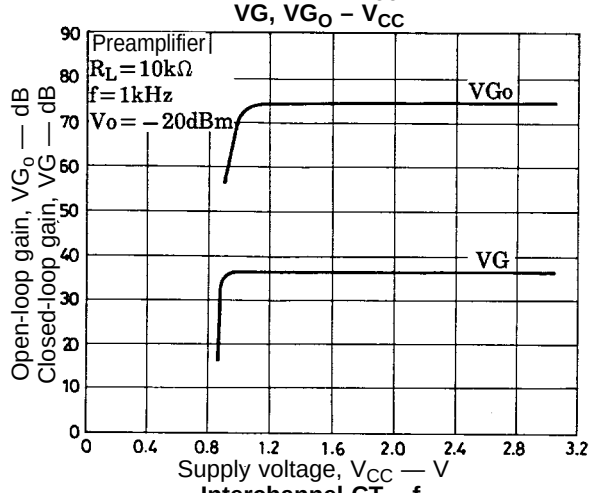


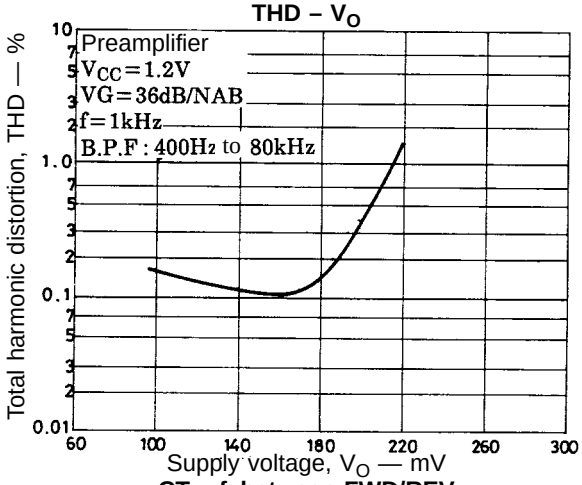
REV when pin 39 FWD/REV is grounded
On in pin 40 metal floating mode

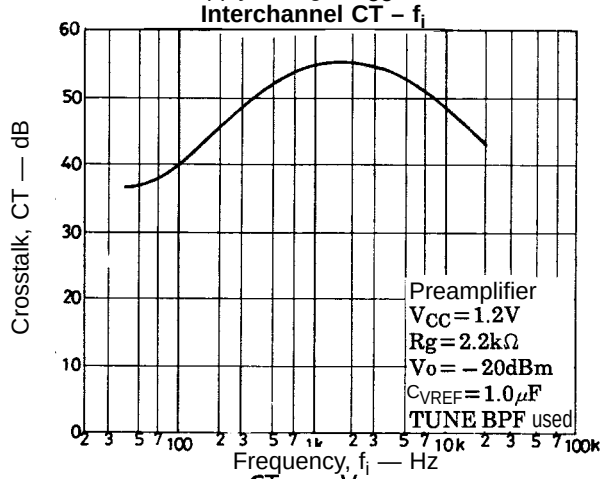
I_O = 7 μA or less
V_S = 0.5 V or less

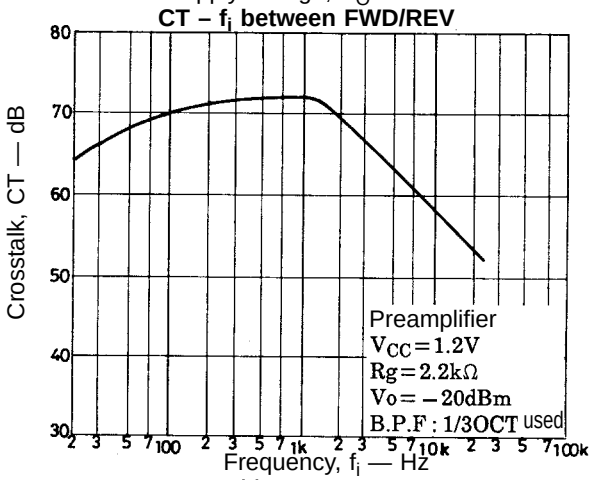

Icco – VCC
Rg=2.2kΩ
RL=16Ω
RV=0Ω
RF1=On
L.B.= On
TOTAL
POWER MUTE ON
Quiescent current, ICCO — mA
Supply voltage, VCC — V

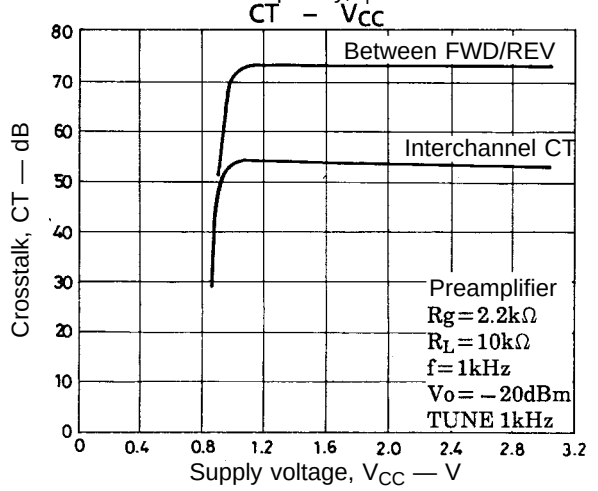

VG,VGO – fi
Preamplifier
RL=10kΩ
Vo=–20dBm
VCC=1.2V
VGo
DIN AUDIO used
Normal
Metal
Open loop gain, VGo — dB
Closed loop gain, VG — dB
Frequency, fi — Hz

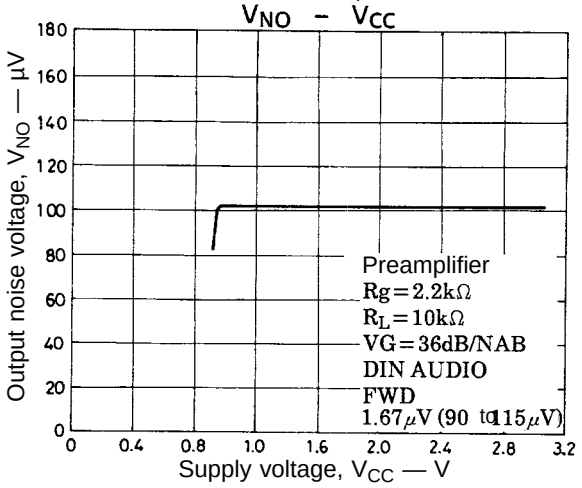

VG, VGO – VCC
Preamplifier
RL=10kΩ
f=1kHz
Vo=–20dBm
VGo
VG
Open-loop gain, VGo — dB
Closed-loop gain, VG — dB
Supply voltage, VCC — V

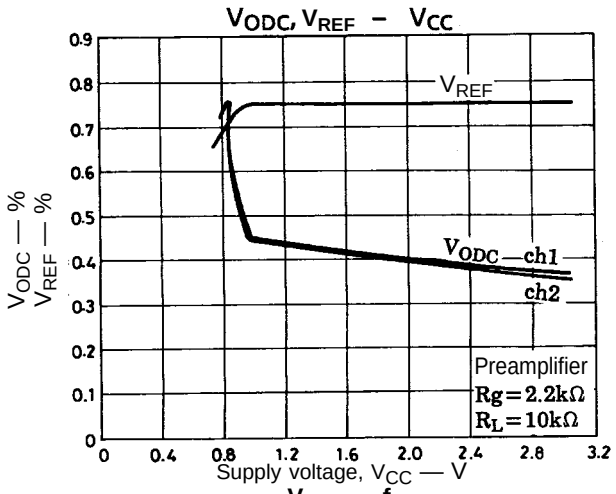

THD – VO
Preamplifier
VCC=1.2V
VG=36dB/NAB
f=1kHz
B.P.F : 400Hz to 80kHz
Total harmonic distortion, THD — %
Supply voltage, VO — mV

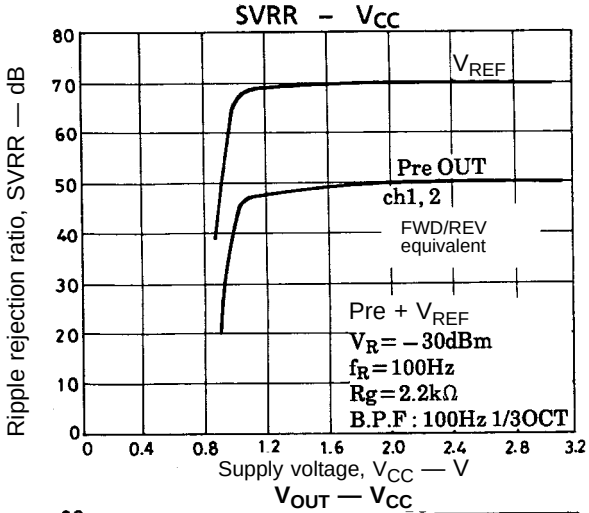

Interchannel CT – fi
Preamplifier
VCC=1.2V
Rg=2.2kΩ
Vo=–20dBm
CVREF=1.0μF
TUNE BPF used
Crosstalk, CT — dB
Frequency, fi — Hz

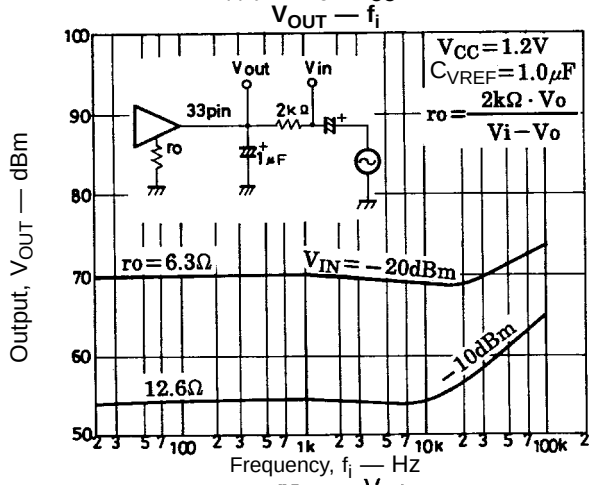

CT – fi between FWD/REV
Preamplifier
VCC=1.2V
Rg=2.2kΩ
Vo=–20dBm
B.P.F : 1/3OCT used
Crosstalk, CT — dB
Frequency, fi — Hz

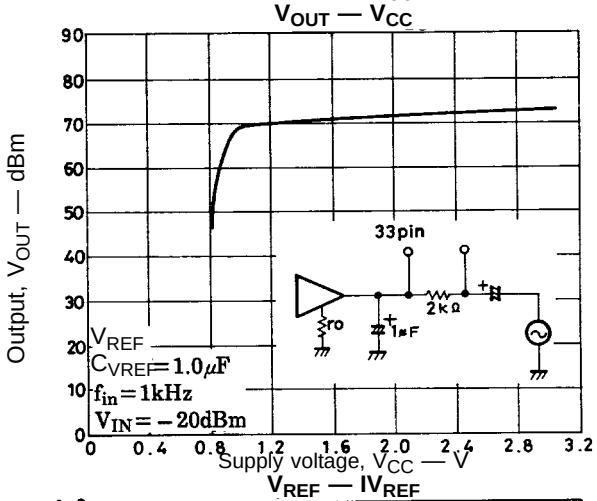

CT – VCC
Between FWD/REV
Interchannel CT
Preamplifier
Rg=2.2kΩ
RL=10kΩ
f=1kHz
Vo=–20dBm
TUNE 1kHz
Crosstalk, CT — dB
Supply voltage, VCC — V

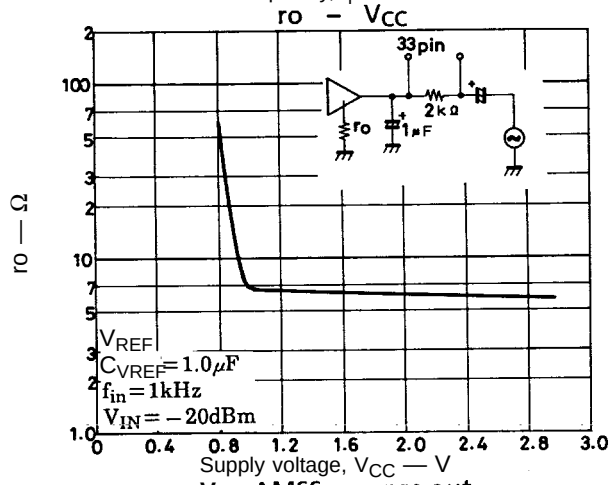

VNO – VCC
Preamplifier
Rg=2.2kΩ
RL=10kΩ
VG=36dB/NAB
DIN AUDIO
FWD
1.67μV (90 to 115μV)
Output noise voltage, VNO — μV
Supply voltage, VCC — V

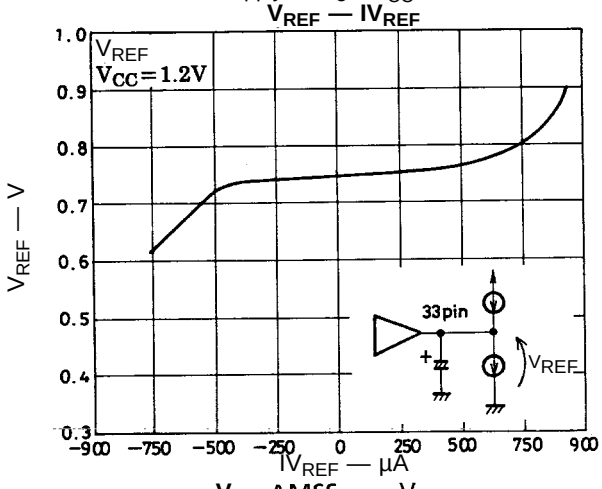

VODC, VREF – VCC
VREF
VODC—ch1
ch2
Preamplifier
Rg=2.2kΩ
RL=10kΩ
VODC — %
VREF — %
Supply voltage, VCC — V

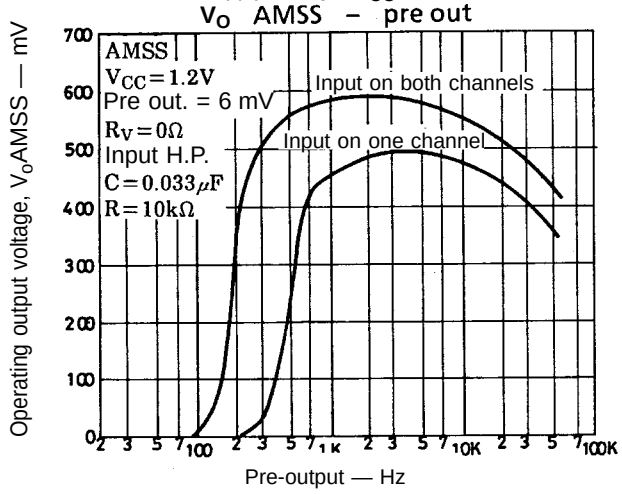

SVRR – VCC
VREF
Pre OUT
ch1, 2
FWD/REV
equivalent
Pre + VREF
VR=–30dBm
fR=100Hz
Rg=2.2kΩ
B.P.F : 100Hz 1/3OCT
Ripple rejection ratio, SVRR — dB
Supply voltage, VCC — V

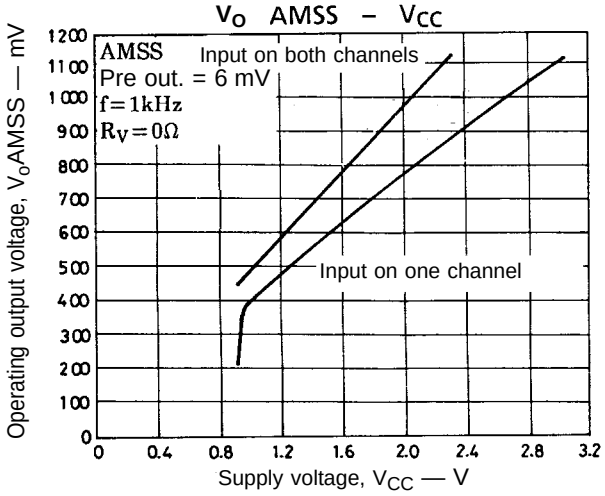

VOUT — fi
VCC=1.2V
CVREF=1.0μF
ro=2kΩ·Vo / Vi–Vo
Vout
Vin
33pin
2kΩ
ro
1μF
ro=6.3Ω
VIN=–20dBm
–10dBm
12.6Ω
Output, VOUT — dBm
Frequency, fi — Hz

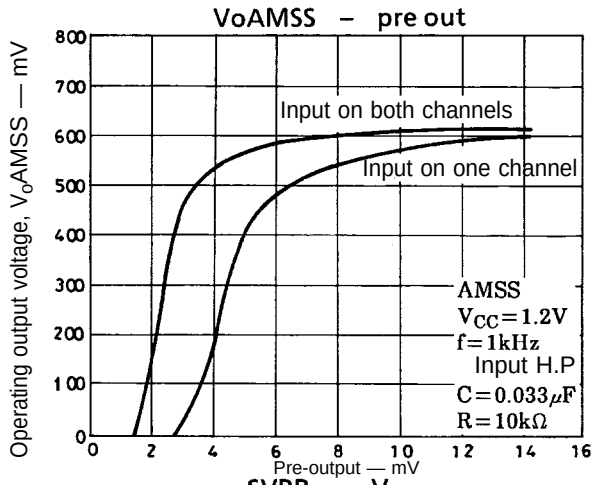

VOUT — VCC
33pin
2kΩ
ro
1μF
VREF
CVREF=1.0μF
fin=1kHz
VIN=–20dBm
Output, VOUT — dBm
Supply voltage, VCC — V

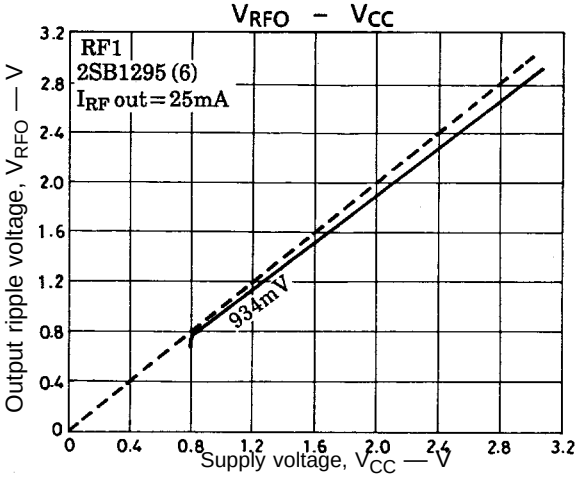

ro – VCC
33pin
2kΩ
ro
1μF
VREF
CVREF=1.0μF
fin=1kHz
VIN=–20dBm
ro — Ω
Supply voltage, VCC — V

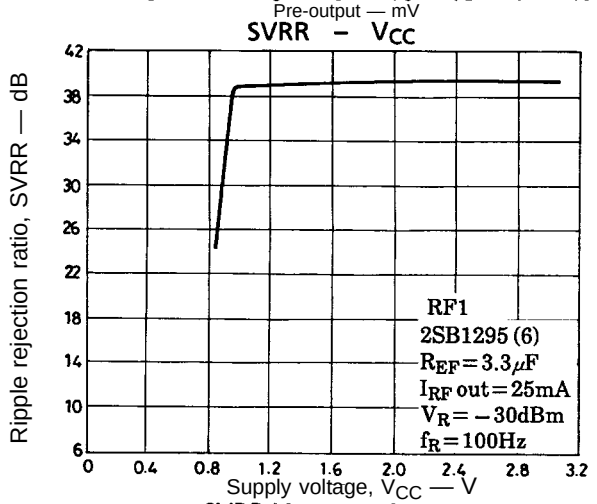

VREF — IVREF
VREF
VCC=1.2V
33pin
VREF
VREF — V
IVREF — μA

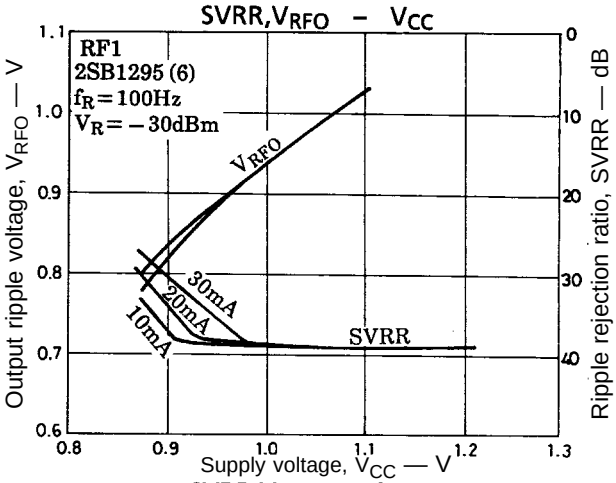

Vo AMSS – pre out
AMSS
VCC=1.2V
Pre out. = 6 mV
RV=0Ω
Input H.P.
C=0.033μF
R=10kΩ
Input on both channels
Input on one channel
Operating output voltage, VoAMSS — mV
Pre-output — Hz

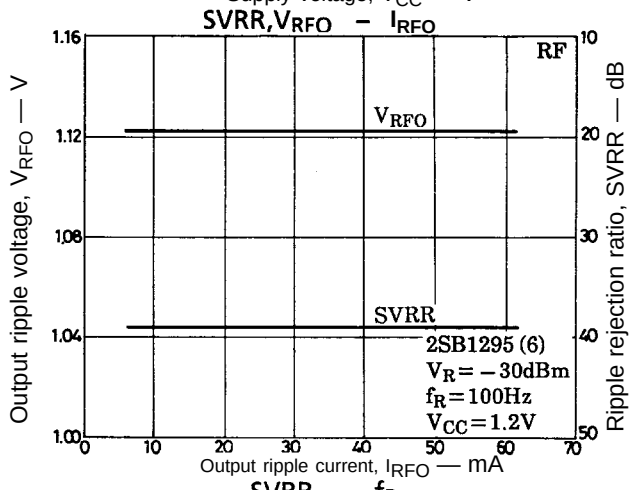

Vo AMSS – VCC
AMSS
Pre out. = 6 mV
f=1kHz
RV=0Ω
Input on both channels
Input on one channel
Operating output voltage, VoAMSS — mV
Supply voltage, VCC — V

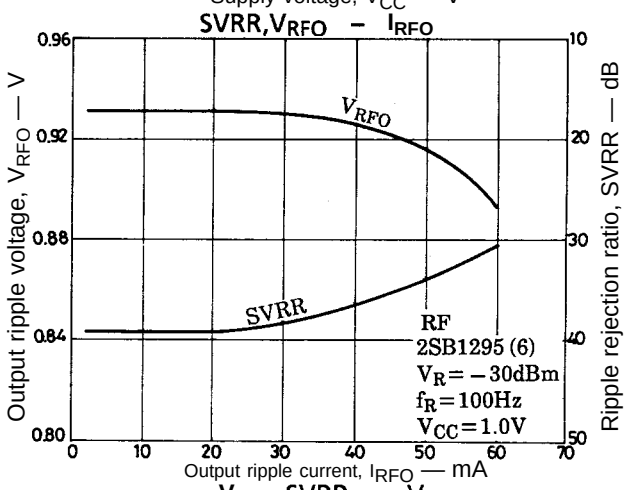

VoAMSS – pre out
Operating output voltage, VoAMSS — mV
Pre-output — mV
Input on both channels
Input on one channel
AMSS
VCC=1.2V
f=1kHz
Input H.P
C=0.033μF
R=10kΩ

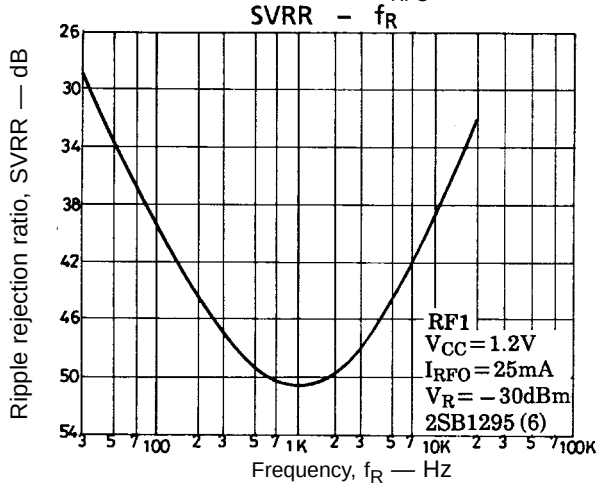

VRFO – VCC
Output ripple voltage, VRFO — V
Supply voltage, VCC — V
RF1
2SB1295 (6)
IRF out=25mA
934mV

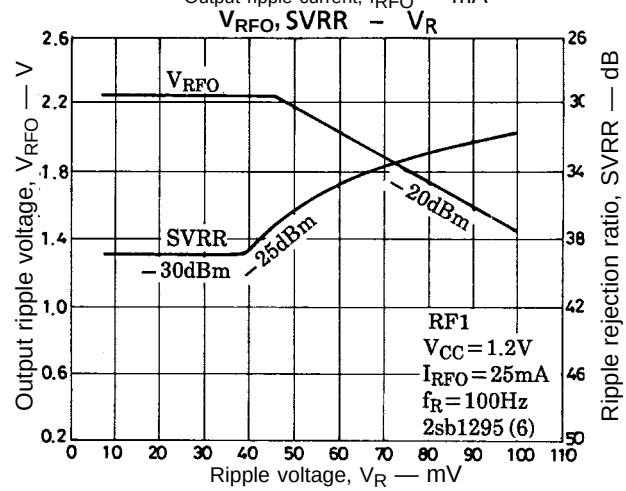

SVRR – VCC
Ripple rejection ratio, SVRR — dB
Supply voltage, VCC — V
RF1
2SB1295 (6)
REF=3.3μF
IRF out=25mA
VR=–30dBm
fR=100Hz

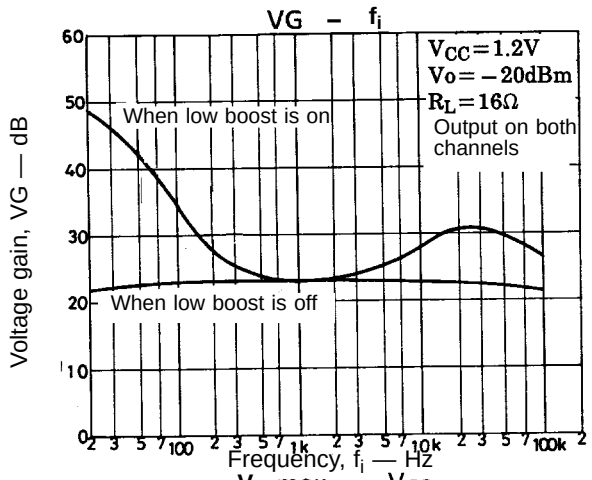

SVRR,VRFO – VCC
Output ripple voltage, VRFO — V
Ripple rejection ratio, SVRR — dB
Supply voltage, VCC — V
RF1
2SB1295 (6)
fR=100Hz
VR=–30dBm
VRFO
30mA
20mA
10mA
SVRR

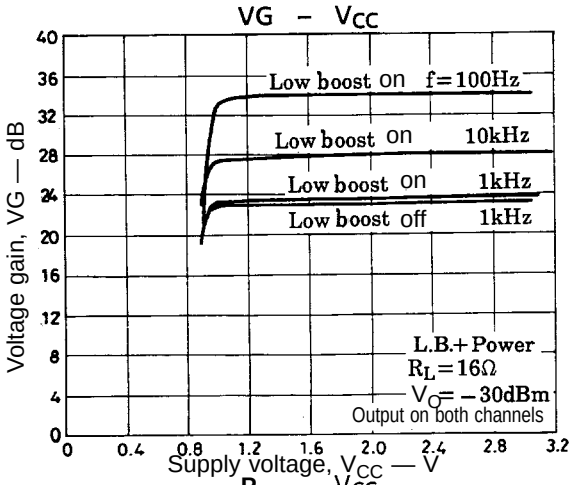

SVRR,VRFO – IRFO
Output ripple voltage, VRFO — V
Ripple rejection ratio, SVRR — dB
Output ripple current, IRFO — mA
RF
VRFO
SVRR
2SB1295 (6)
VR=–30dBm
fR=100Hz
VCC=1.2V

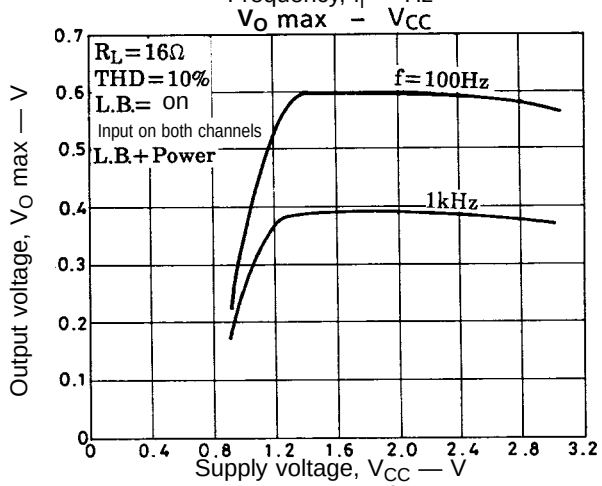

SVRR,VRFO – IRFO
Output ripple voltage, VRFO — V
Ripple rejection ratio, SVRR — dB
Output ripple current, IRFO — mA
VRFO
SVRR
RF
2SB1295 (6)
VR=–30dBm
fR=100Hz
VCC=1.0V

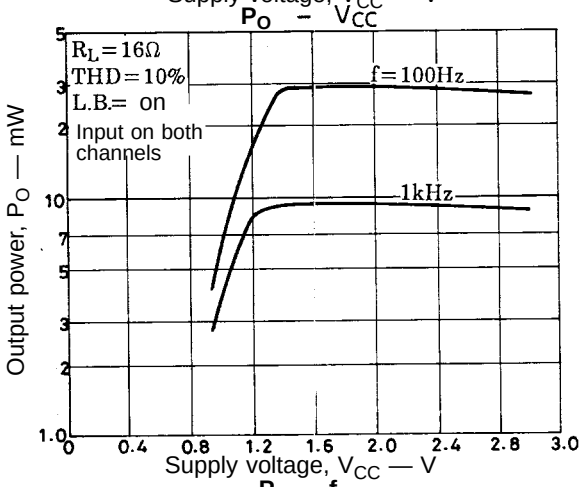

SVRR – fR
Ripple rejection ratio, SVRR — dB
Frequency, fR — Hz
RF1
VCC=1.2V
IRFO=25mA
VR=–30dBm
2SB1295 (6)

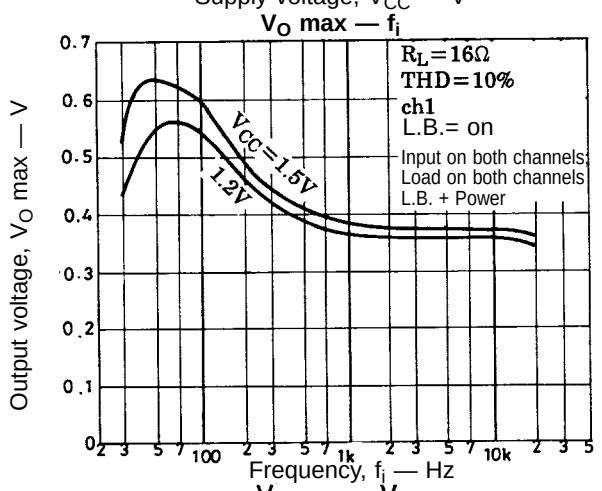

VRFO, SVRR – VR
Output ripple voltage, VRFO — V
Ripple rejection ratio, SVRR — dB
Ripple voltage, VR — mV
VRFO
SVRR
–20dBm
–25dBm
–30dBm
RF1
VCC=1.2V
IRFO=25mA
fR=100Hz
2sb1295 (6)

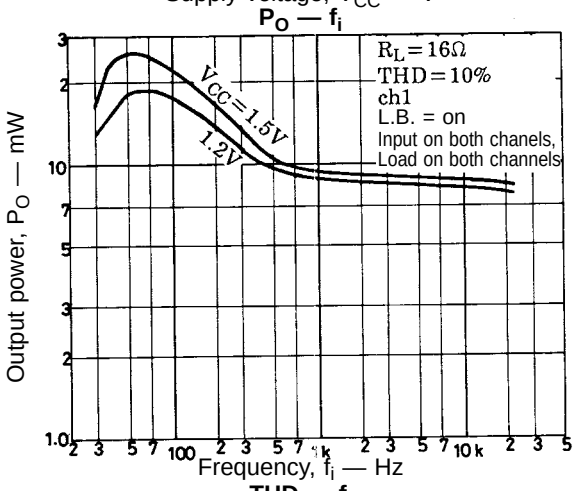

VG – fi
VCC=1.2V
Vo=–20dBm
RL=16Ω
Output on both channels
When low boost is on
When low boost is off
Voltage gain, VG — dB
Frequency, fi — Hz

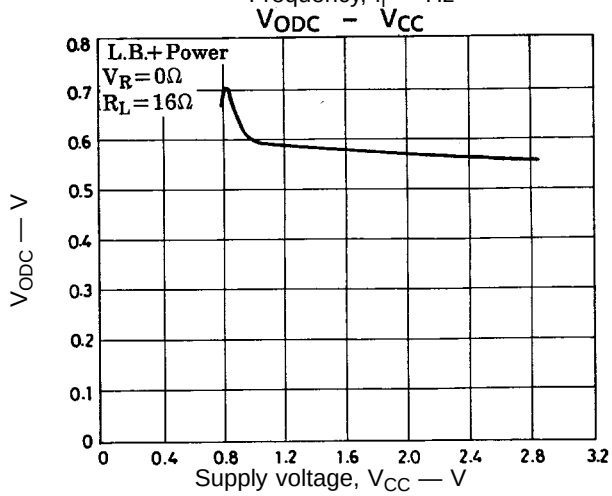

VG – VCC
Low boost on f=100Hz
Low boost on 10kHz
Low boost on 1kHz
Low boost off 1kHz
L.B.+Power
RL=16Ω
Vo=–30dBm
Output on both channels
Voltage gain, VG — dB
Supply voltage, VCC — V

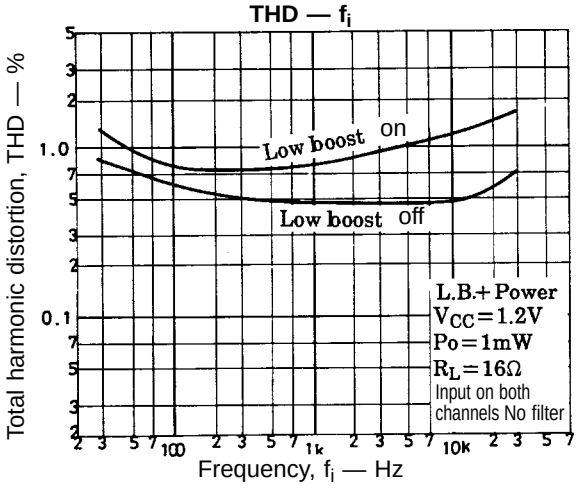

Vo max – VCC
RL=16Ω
THD=10%
L.B.= on
Input on both channels
L.B.+Power
f=100Hz
1kHz
Output voltage, Vo max — V
Supply voltage, VCC — V


Po – VCC
RL=16Ω
THD=10%
L.B.= on
Input on both channels
f=100Hz
1kHz
Output power, Po — mW
Supply voltage, VCC — V


Vo max — fi
RL=16Ω
THD=10%
ch1
L.B.= on
Input on both channels
Load on both channels
L.B. + Power
VCC=1.5V
1.2V
Output voltage, Vo max — V
Frequency, fi — Hz


Po — fi
RL=16Ω
THD=10%
ch1
L.B. = on
Input on both chanels,
Load on both channels
VCC=1.5V
1.2V
Output power, Po — mW
Frequency, fi — Hz


VODC – VCC
L.B.+Power
VR=0Ω
RL=16Ω
VODC — V
Supply voltage, VCC — V


THD — fi
Low boost on
Low boost off
L.B.+Power
VCC=1.2V
Po=1mW
RL=16Ω
Input on both channels No filter
Total harmonic distortion, THD — %
Frequency, fi — Hz