Ordering number : EN5661

Monolithic Linear IC

LA4585M

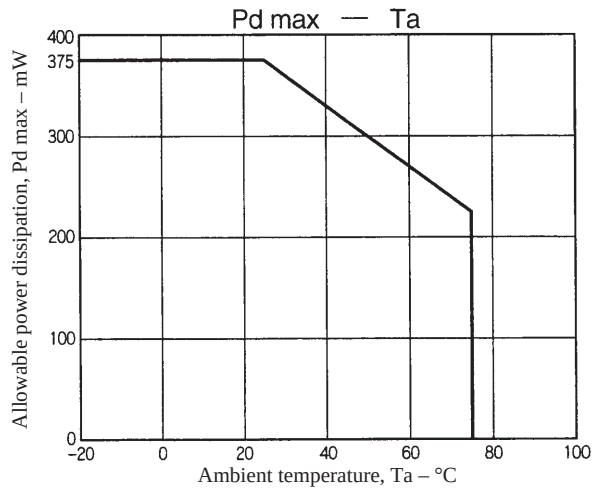
3-V Preamplifier + Power Amplifier for Headphone Stereo Products

Overview

The LA4585M is a preamplifier plus power amplifier IC that supports auto-reverse and was developed for use in 3-V headphone stereo products.

Features

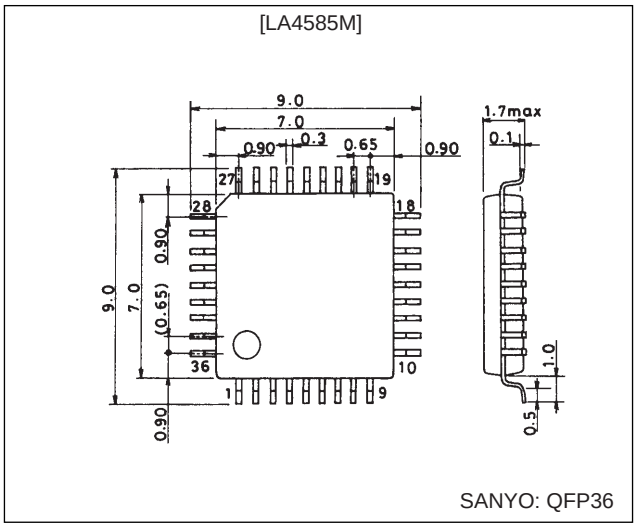
- The LA4585M is designed for use in playback-only compact cassette players. In addition to preamplifier and power amplifier functions, the LA4585M also provides low boost and automatic power output limiter (PVSS:Peak Volume Select System) functions.
- Provided in a mini-flat 36-pin quad package (0.65 mm lead pitch) optimal for miniature end products.
- Two auto-reverse playback preamplifiers
- Two headphone power amplifiers (16 Ω)
- Low boost function (auto-loudness effect)
- Output limiter function (PVSS)
- Two radio input switches (pre-muting switches)
- Power muting switch



Package Dimensions

unit: mm

3162B-QFP36



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		4.5	V
Allowable power dissipation	Pd max		375	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–40 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		3.0	V
Operating supply voltage range	V_{CC}op		1.8 to 3.6	V

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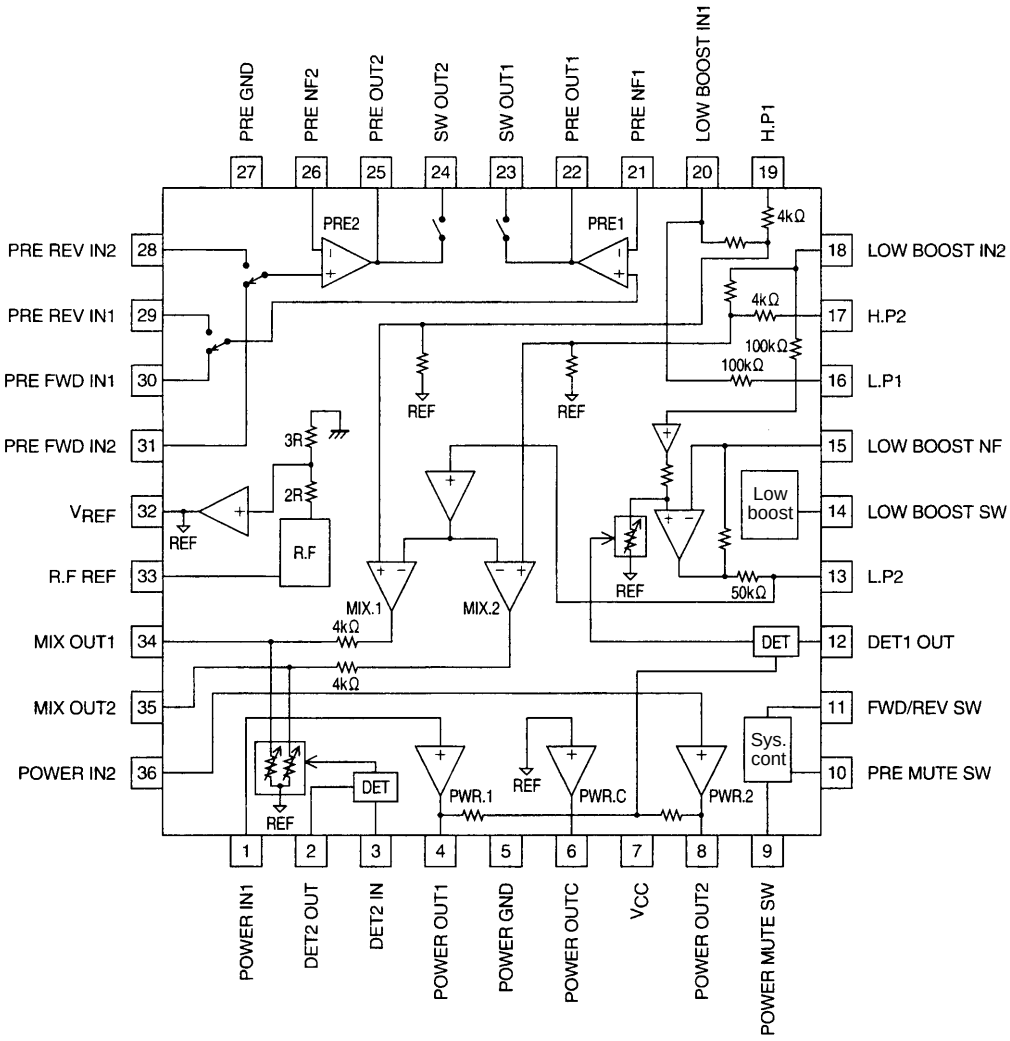
Operating Characteristics at Ta = 25°C, V_{CC} = 3.0 V, fi = 1 kHz, 0.775 = 0 dBm, preamplifier R_L = 10 kΩ, low boost, power amplifier R_L = 10 Ω

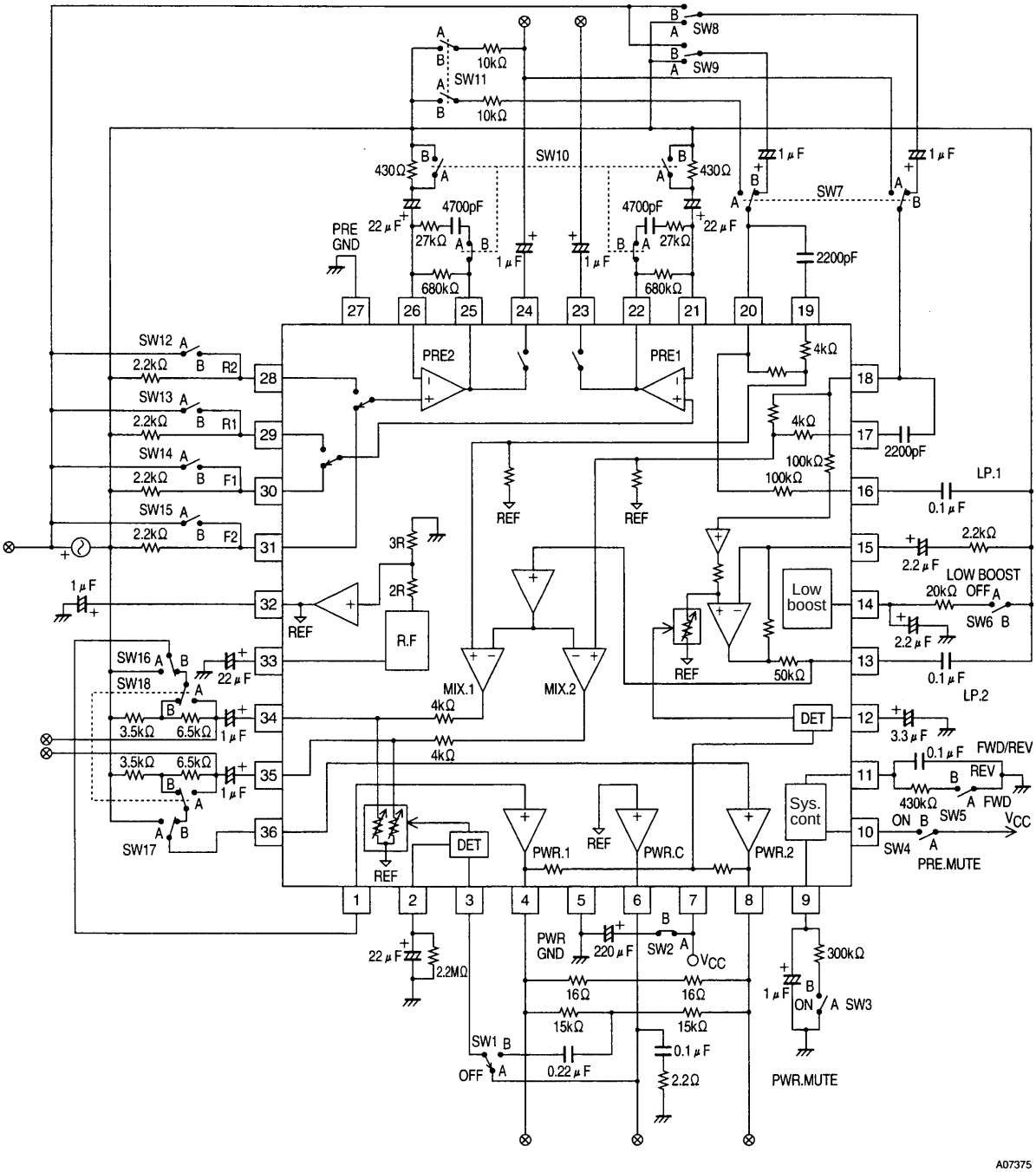
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[PRE + LOW BOOST + PVSS + PWR]						
Quiescent current	$I_{CCO}1$	Rg = 2.2 kΩ, low boost off, PVSS off	12	15	21	mA
	$I_{CCO}2$	Rg = 2.2 kΩ, low boost on, PVSS on	12	15	21	µA
Voltage gain (closed loop)	VG_T	V_O = –5 dBm	62	64	67	dB
[PRE AMP]						
Voltage gain (open loop)	VG_0	V_O = –5 dBm	70	83		dB
Voltage gain (closed loop)	VG1	V_O = –5 dBm		40		dB
Maximum output voltage	V_O max1	THD = 1 %, V_{CC} = 1.8 V	0.1	0.2		V
Total harmonic distortion	THD1	V_O = 0.2 V, VG = 40 dB/NAB		0.05	0.5	%
Equivalent input noise voltage	V_{NI}	Rg = 2.2 kΩ, BPF = 20 Hz to 20 kHz		1.3	2.0	µV
Crosstalk	CT1	Rg = 2.2 kΩ, TUNE 1 kHz	60	80		dB
Ripple rejection ratio	SVRR	Rg = 2.2 kΩ, V_{CC} = 1.8 V, Vr = –20 dBm, fr = 100 Hz	40	50		dB
[POWER AMP]						
Output voltage	P_O	THD = 10 %	23	34		mW
Voltage gain	VG2	V_O = –5 dBm	27	29	32	dB
Total harmonic distortion	THD2	P_O = 1 mW		0.4	1.0	%
Interchannel crosstalk	CT2	V_O = –5 dBm, R_V = 0 Ω	30	40		dB
Output noise voltage	$V_{NO}1$	R_V = 0 Ω, BPF = 20 Hz to 20 kHz		25	40	µV
Ripple rejection ratio	R_r2	R_V = 0 Ω, Vr = –20 dBm, fr = 100 Hz, V_{CC} = 1.8 V	45	55		dB
Input resistance	Ri		22	30	38	kΩ
DC offset voltage	$V_{ODC\ OFF}$	Between pin 6 and pins 4 and 8	–90		+90	mV
[LOW BOOST]						
Voltage gain	VG3	Vi = –30 dBm, boost on/off	–2.3	–3.8	–5.3	dB
Boost*	BST1	Vi_{BST} = –30 dBm, f = 100 Hz, boost on	11.2	14.7	18.2	dB
	BST2	Vi_{BST} = –30 dBm, f = 10 kHz, boost on	7.0	8.5	10	dB
Maximum output voltage	V_O max2	THD = 1%, boost on	0.25	0.4		V
Total harmonic distortion	THD3	V_O = 0.1 V, boost on		0.1	0.5	%
Interchannel crosstalk	CT3	V_O = –20 dBm, Rg = 0, boost on	25	32		dB
Output noise voltage	$V_{NO}2$	Rg = 0, BPF = 20 Hz to 20 kHz, boost on		2.0	5.0	µV
Ripple rejection ratio	R_r3	Rg = 0, f_R = 100 Hz, V_R = –20 dBm, V_{CC} = 1.8 V, boost on	45	53		dB
[LOW BOOST + PVSS + POWER] The following items are measured at an R_V of 10 kΩ maximum.						
Voltage gain	VG4	Vi = –40 dBm, f = 1 kHz, boost off/on	22	24	27	dB
LOW BOOST output voltage	V_O1	Vi = –43 dBm, f = 100 Hz, boost on	0.13	0.23	0.33	V
LOW BOOST output voltage	V_O2	Vi = –28 dBm, f = 100 Hz, boost on	0.25	0.40	0.55	V
LOW BOOST total harmonic distortion	THD4	Vi = –40 dBm, f = 100 Hz, boost on		0.5	1.2	%
Output noise voltage	$V_{NO}3$	Rg = 0, CCIR-ARM, boost off, with the power input switch K18 set to B.	–88	–85	–82	dBm
PVSS voltage	V_O3	Vi = –40 dBm, PVSS 2	–40	–37	–34	dBm
PVSS width	W_{PVSS}	The input amplitude between the start point and the point where the output is +4 dB. PVSS on	30	40		dB
PVSS harmonic distortion	THD5	Vi = –40 dBm, PVSS 2		0.5	1.2	%
PVSS start input level	V_{OPi}	PVSS 2	–67	–63	–59	dBm

Note: *The amount of boost for a 1-kHz input.

Block Diagram



Test Circuit Diagram



Sample Application Circuit