

<b>SANYO</b>	No. 3988A	<b>LA2230, LA2230M</b>
		<b>RDS Decoder</b>

## OVERVIEW

The LA2230 and LA2230M are RDS demodulator ICs with an on-chip 57 kHz bandpass filter and ARI-SK and DK signal identifiers. A high-performance, cost-effective RDS decoder system with group/block synchronization and error detection/correction can be built using an LC7070 series device with the LA2230 or LA2230M.

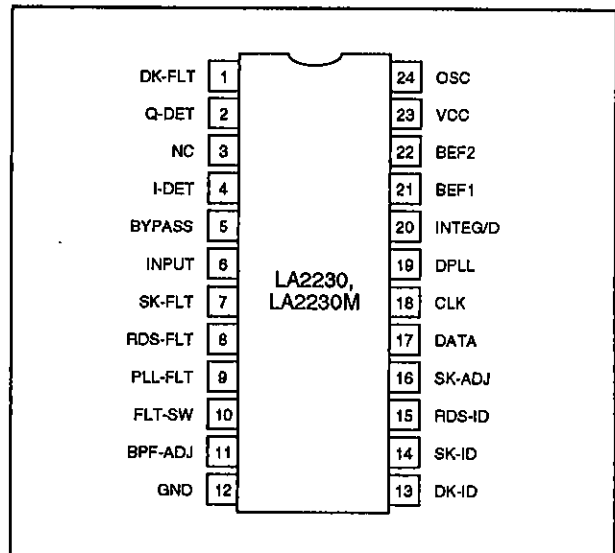
The LA2230 and LA2230M feature adjustable ARI detection sensitivity for improved interference rejection and a high-speed charging circuit for rapid power-on start-up. Including the 57 kHz bandpass filter on-chip results in lower-cost designs that use less PCB area.

The LA2230 and LA2230M operate from a 5 V supply and are available in 24-pin DIPs and 24-pin MFPs, respectively.

## FEATURES

- 57 kHz bandpass filter
- Adjustable ARI detection sensitivity
- High-speed charging circuit
- ARI and RDS signal demodulation
- Bit-rate clock recovery
- RDS, DK and SK identification outputs
- 5 V supply
- 24-pin DIP (LA2230) and 24-pin MFP (LA2230M)

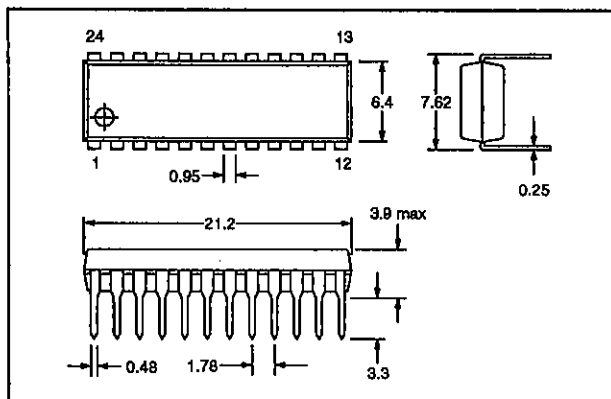
## PINOUT



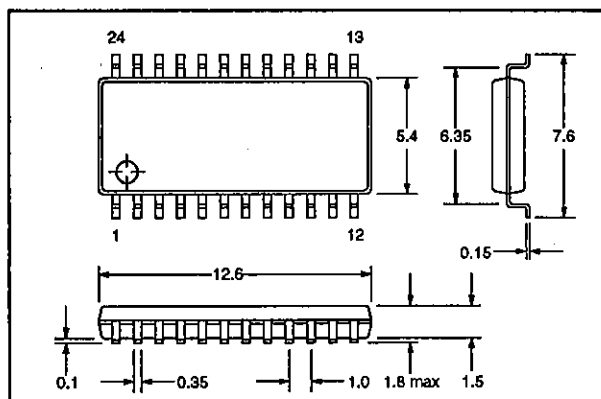
**PACKAGE DIMENSIONS**

Unit: mm

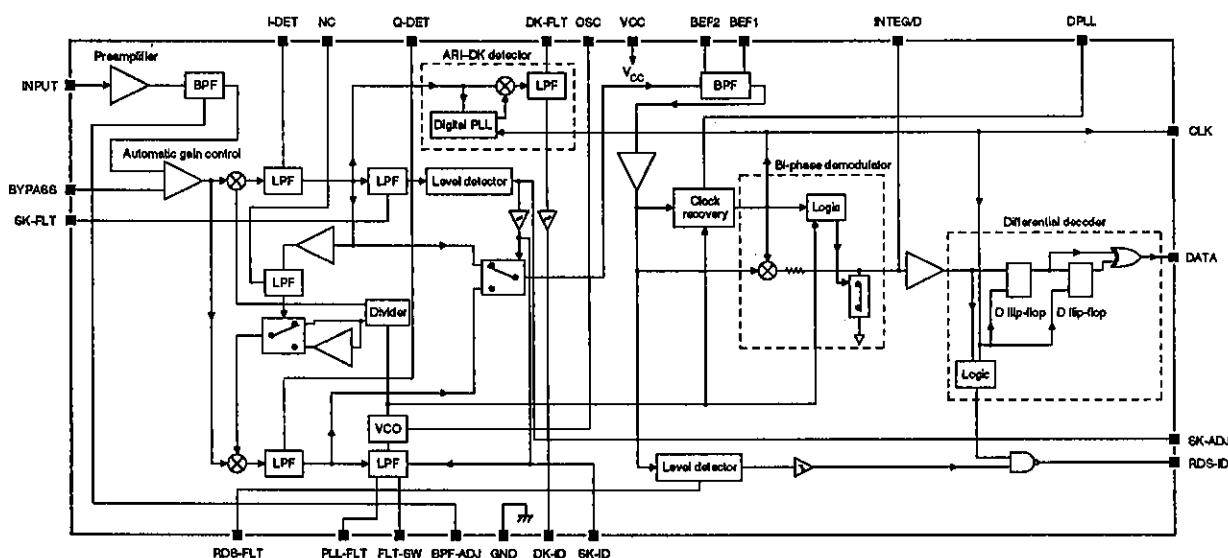
**3067-DIP24S (LA2230)**



**3112-MFP24S (LA2230M)**



**BLOCK DIAGRAM**



**PIN DESCRIPTION**

Number	Name	Description
1	DK-FLT	DK in-phase detector lowpass filter connection
2	Q-DET	Quadrature detection output
3	NC	No connection. Should be left open.
4	I-DET	In-phase detector output
5	BYPASS	Bandpass filter bypass capacitor connection
6	INPUT	ARI and RDS signal input
7	SK-FLT	SK lowpass filter capacitor connection
8	RDS-FLT	RDS lowpass filter capacitor connection
9	PLL-FLT	PLL loop filter connection
10	FLT-SW	PLL loop filter switch

## LA2230, LA2230M

Number	Name	Description
11	BPF-ADJ	Bandpass filter adjustment variable resistor connection
12	GND	Ground
13	DK-ID	ARI-DK signal identification output
14	SK-ID	ARI-SK signal identification output
15	RDS-ID	RDS signal identification output
16	SK-ADJ	ARI detection sensitivity adjustment variable resistor connection
17	DATA	Data output
18	CLK	Bit-rate clock output
19	DPLL	Digital PLL lowpass filter connection
20	INTEG/D	Integrator and dump capacitor connection
21	BEF1	Band-elimination filter connections
22	BEF2	
23	VCC	5 V supply
24	OSC	Ceramic resonator connection

## SPECIFICATIONS

### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	12	V
Power dissipation	$P_D$	450 (LA2230)	mW
		450 (LA2230M, $T_a \leq 37.5^\circ\text{C}$ )	
		280 (LA2230M, $T_a = 80^\circ\text{C}$ )	
Operating temperature range	$T_{opr}$	-30 to 80	$^\circ\text{C}$
Storage temperature range	$T_{stg}$	-40 to 125 (LA2230)	$^\circ\text{C}$
		-40 to 150 (LA2230M)	

### Recommended Operating Conditions

$T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	5	V
Supply voltage range	$V_{CC}$	4.7 to 5.5	V

### Electrical Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Quiescent supply current	$I_{CCQ}$		14	22	28	mA
RDS detection sensitivity	$V_{IT}$	$V_{INPUT}$ = minimum signal for HIGH-to-LOW transition on RDS-ID	-	0.4	1.0	mV

LA2230, LA2230M

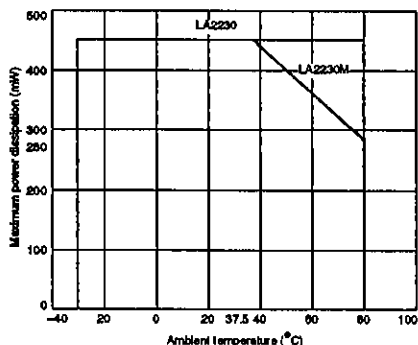
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
SK detection sensitivity	$V_{I2}$	$V_{INPUT}$ = minimum signal for HIGH-to-LOW transition on SK-ID	-	1.0	2.0	mV
DK detection sensitivity	$V_{I3}$	$V_{INPUT}$ = minimum signal for HIGH-to-LOW transition on DK-ID	-	1.1	2.0	mV
RDS detection maximum input signal	$V_{I4}$	$V_{INPUT}$ = maximum (ARI + RDS) signal for HIGH-to-LOW transition on RDS-ID	30	50	-	mV
	$V_{I5}$	$V_{INPUT}$ = maximum RDS signal for RDS data correctly demodulated	250	-	-	mV
DK detection maximum input signal	$V_{I6}$	$V_{INPUT}$ = maximum ARI signal for HIGH-to-LOW transition on DK-ID	75	100	-	mV
CLK and DATA LOW-level output voltage	$V_{OL}$		0	0.1	0.3	V
CLK and DATA HIGH-level output voltage	$V_{OH}$		4.7	4.9	5.0	V
Bandpass filter voltage gain	$V_G$	$f = 57$ kHz	9.0	12.5	17.0	dB
Bandpass filter attenuation	$\alpha$	$f = 60$ kHz. See note 1.	0	2.5	6.0	dB
		$f = 54$ kHz. See note 1.	0	3.5	6.0	dB
		$f = 38$ kHz. See note 1.	33	39	-	dB
PLL capture range	CR	Low side, $V_{INPUT} = 5$ mV sine wave	-	-0.9	-	%
		High side, $V_{INPUT} = 5$ mV sine wave	-	1.5	-	
Bit-rate clock jitter	$t_j$		$\pm 8$	$\pm 9$	$\pm 10$	$\mu$ s
RDS lock-up time	$t_{RDS}$	Period from $V_{INPUT} = 3$ mV RDS signal to HIGH-to-LOW transition on RDS-ID	-	35	-	ms
SK lock-up time	$t_{SK}$	Period from $V_{INPUT} = 8$ mV ARI signal to HIGH-to-LOW transition on SK-ID	-	45	-	ms
SK + RDS lock-up time	$t_{SK + RDS}$	Period from $V_{INPUT} = 8.5$ mV (ARI + RDS) signal to HIGH-to-LOW transition on RDS-ID	-	80	-	ms
VCO free-running frequency	$f_{VCO}$		453	456	459	kHz
BPF adjustment resistance	$R_{ADJ}$	$V_{INPUT} = 100$ mV at 57 kHz. See note 2.	5.6	8.0	10.6	k $\Omega$

Notes

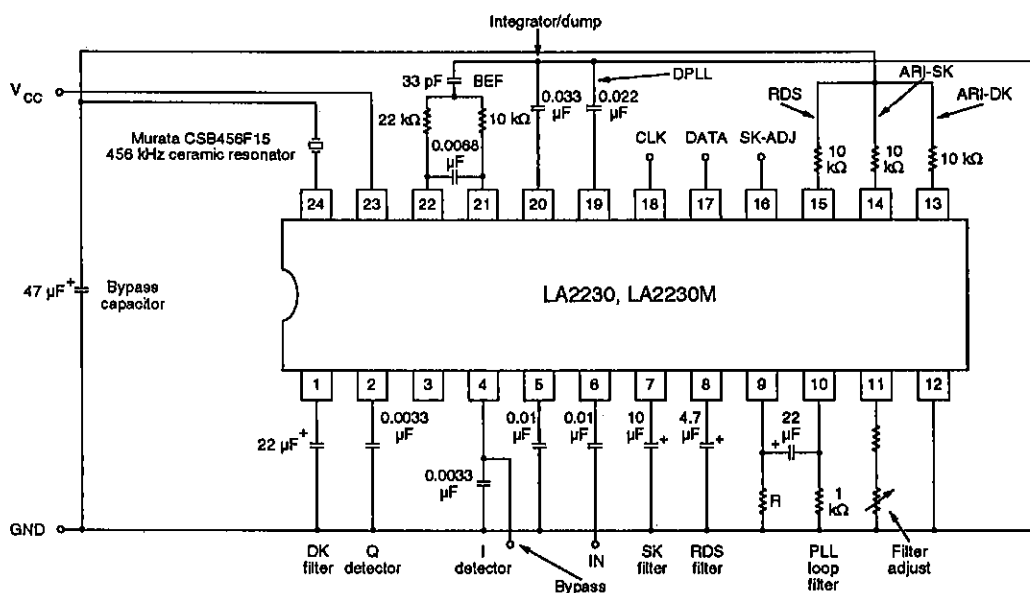
- 0 dB is referenced to the filter output with  $f = 57$  kHz.
- Resistance between BPF-ADJ and GND when  $V_{BYPASS}$  is at its maximum.

Typical Performance Characteristics

Maximum power dissipation vs. ambient temperature



Measurement Circuit



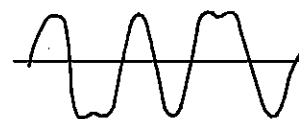
Note

R = 1.2 MΩ for the LA2230, and 1.5 MΩ for the LA2230M

OPERATING INFORMATION

57 kHz Bandpass Filter Adjustment

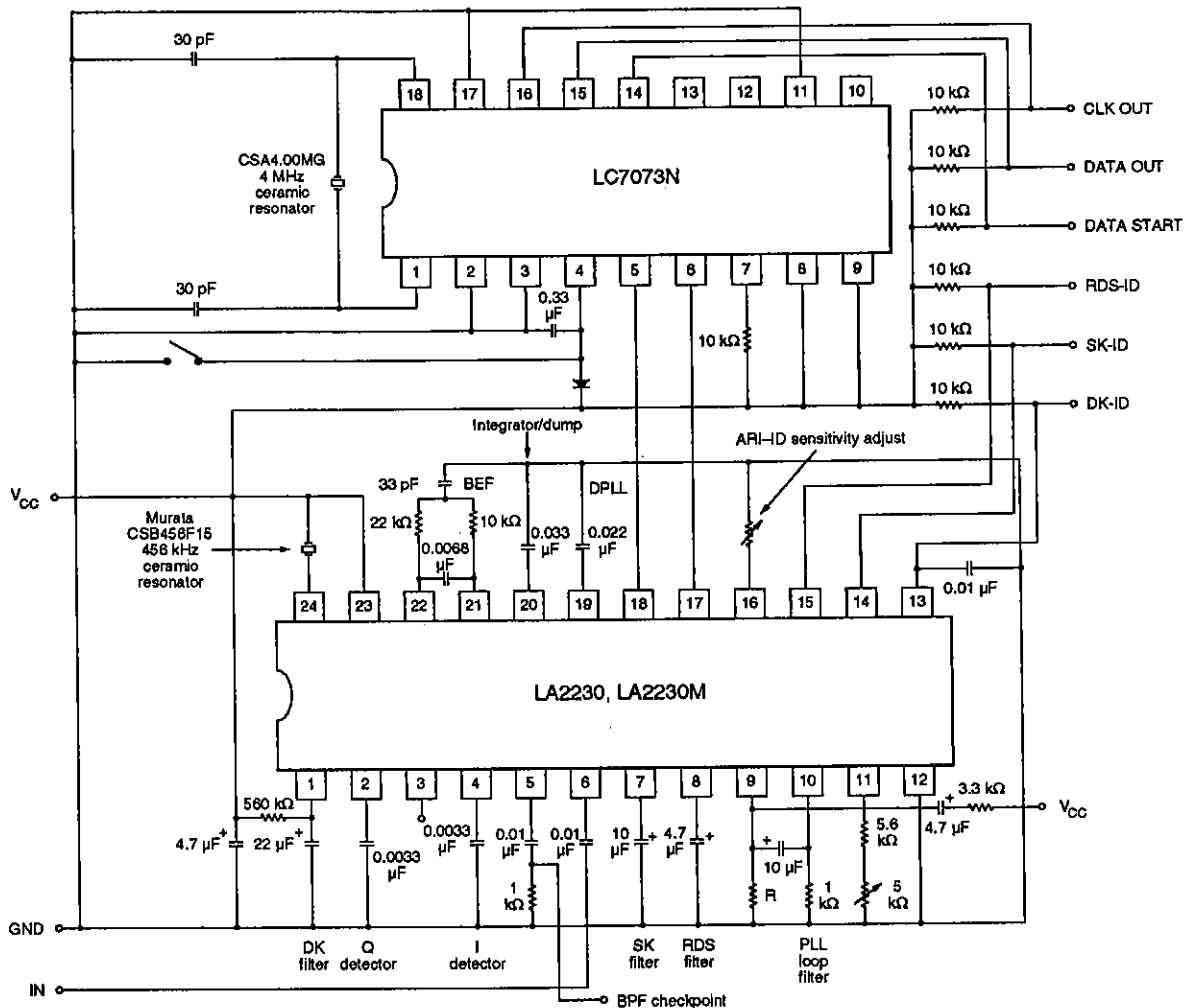
1. Adjust the variable resistor connected to BPF-ADJ to obtain the maximum signal level measured at I-DET or BEF2.
2. When  $V_{INPUT} = 1$  mV RDS signal, check I-DET or BEF2 for a bi-phase output signal as shown in the following figure. Note that the ALC circuit will not operate when  $V_{INPUT} \leq 1$  mV.



3. Check the BPF checkpoint signal level when  $V_{INPUT} = 3$  to 6 mV or greater RDS signal.

**TYPICAL APPLICATION**

The recommended input is a 3 to 6 mV RDS signal with  $\Delta f = \pm 2$  kHz.



**Note**

R = 1.2 MΩ for the LA2230, and 1.5 MΩ, for the LA2230M

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