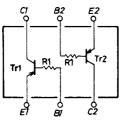


FC135 PNP Epitaxial Planar Silicon Composite Transistor Switching Applications (with Bias Resistance)

Features

- · On-chip bias resistance (R1=4.7k Ω)).
- Composite type with 2 transistors contained in the CP package currently in use, improving the mounting efficiency greatly.
- \cdot The FC135 is formed with two chips, being equivalent to the 2SA1510, placed in one package.
- \cdot Excellent in thermal equilibrium and pair capability.

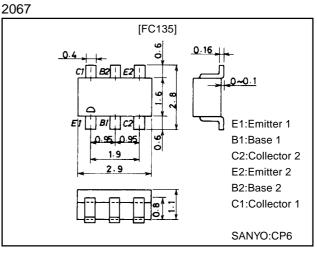
Electrical Connection



E1:Emitter 1 B1:Base 1 C2:Collector 2 E2:Emitter 2 B2:Base 2 C1:Collector 1

Package Dimensions

unit:mm



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	VCBO		-50	V
Collector-to-Emitter Voltage	VCEO		-50	V
Emitter-to-Base Voltage	VEBO		-5	V
Collector Current	IC		-100	mA
Peak Collector Current	ICP		-200	mA
Collector Dissipation	PC	1 unit	200	mW
Total Power Dissipation	PT		300	mW
Junction Temperature	Tj		150	°C
Storage Temperature	Tstg		-55 to +150	°C

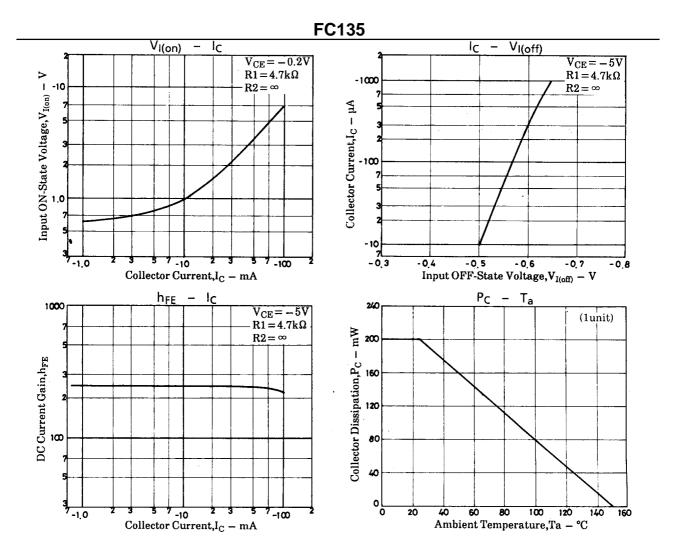
Electrical Characteristics at Ta = 25°C

Parameter	Symbol	Conditons	Ratings			Unit
			min	typ	max	Unit
Collector Cutoff Current	ICBO	V _{CB} =-40V, I _E =0			-0.1	μA
Emitter Cutoff Current	IEBO	V _{EB} =-5V, I _C =0			-0.1	μA
DC Current Gain	hFE	V _{CE} =-5V, I _C =-10mA	100			
Gain-Bandwidth Product	fT	V _{CE} =-10V, I _C =-5mA		200		MHz
Output Capacitance	Cob	V _{CB} =-10V, f=1MHz		5.1		pF
C-E Saturation Voltage	V _{CE(sat)}	IC=-10mA, IB=-0.5mA		-0.1	-0.3	V
C-B Breakdown Voltage	V(BR)CBO	I _C =-10µA, I _E =0	-50			V
C-E Breakdown Voltage	V(BR)CEO	I _C =–100µA, R _{BE} =∞	-50			V
Input OFF-State Voltage	V _{I(off)}	V _{CE} =-5V, I _C =-100µA	-0.4	-0.55	-0.8	V
Input ON-State Voltage	V _{I(on)}	V _{CE} =-0.2V, I _C =-10mA	-0.6	-1.0	-2.0	V
Input Resistance	R1		3.3	4.7	6.1	kΩ

Note: The specifications shown above are for each individual transistor.

Marking:135

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