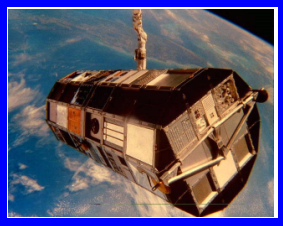
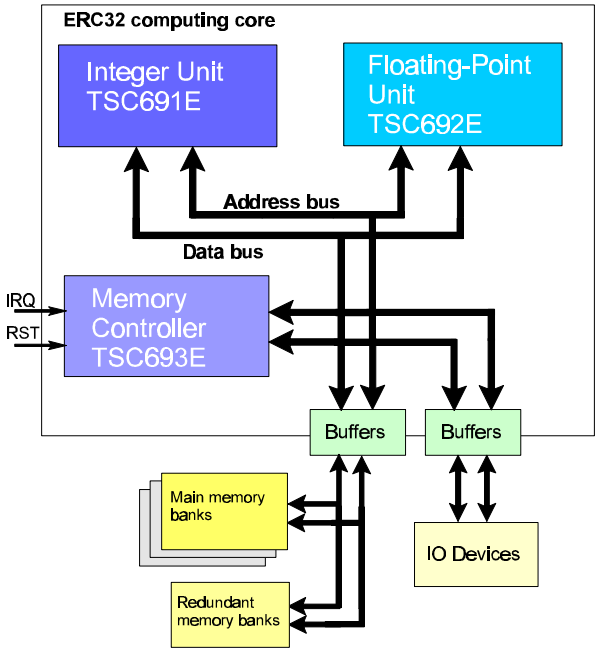


SPARC Processor for SPACE Applications

TEMIC Semiconductors is offering a SPARC RT (Radiation Tolerant) processor, based on SPARC V7 architecture, for space applications, consisting of three devices:

- integer unit (IU), the TSC691E,
- floating point unit (FPU), the TSC692E,
- memory controller (MEC), the TSC693E.

It has been designed on purpose for space, as it has on-chip concurrent transient and permanent errors detection.
The chip-set, also called ERC32, has been developed with the support of the European Space Agency, and is offering a full development environment for embedded space applications.
The chips are manufactured using the TEMIC 0.8 µm radiation tolerant CMOS process.



Chip-Set Characteristics

- Concurrent error detection : more than 99% of all SEU induced errors are detected and trapped
- JTAG interface
- VHDL models available
- Performance : 10 Mips / 2 Mflops (SP) @ 14 MHz
- Power consumption : better than 5 W @ 10 Mips
- Voltage range : 4.5 to 5.5 V
- Temperature range : -55 to +125 °C
- Total dose radiation capability : better than 50 Krads (Si)
- SEU LET threshold :
  - TSC691E : 13 MeV / cm2 / mg
  - TSC692E : 17 MeV / cm2 / mg
  - TSC693E : 50 MeV / cm2 / mg
- Latch up better than 100 MeV
- Quality grades : any ESA SCC or MIL-I-38510 (QML / MIL-I-38535 certification on going)

TSC693E Memory Controller

- Address decoding & memory interface
- Wait state generation
- Interrupt controller
- Block protection unit
- 32-bit SEC/DED EDAC
- Two 32-bit timers
- Two UARTS
- Boot PROM interface
- DMA PROM interface
- Error manager
- Watchdog
- Package: 256 MQFPF

TSC692E Floating-Point Unit

- Full compliance with ANSI/IEEE 754 standard for binary Floating-Point Arithmetic
- Supports single and double precision Floating-Point operations
- Direct interface to TSC691E Integer Unit
- 64-bit ALU and Multiplier/Divide/Square root
- 16 64-bit registers or 32 32-bit registers in three-port Floating-Point Register File
- Package: 160 MQFPL

TSC691E 32-bit Integer Unit

- 8 window Register Files
- FPU interface allows concurrent execution of Floating-Point instructions
- User/supervisor modes for multitasking
- Package: 256 MQFPF

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TSC691E Integer Unit

The TSC691E Integer Unit is a high-speed CMOS implementation of the SPARC 32-bit RISC processor. It is designed for highly dependable space and military applications, and includes support for error detection. The RISC architecture makes possible the creation of a processor that can execute instructions at a rate of one instruction per processor clock.

The TSC691E supports a tightly coupled floating-point interface and coprocessor interface that allows concurrent execution of floating-point, coprocessor, and integer instructions.

Description

One of the major contributing factors to the TSC691E's very high performance is an instruction execution rate approaching one instruction per clock cycle. To achieve that rate of execution, the TSC691E employs a four-stage instruction pipeline that permits parallel execution of multiple instructions.

- Fetch—The processor outputs the instruction address to fetch the instruction.
- Decode—The instruction is placed in the instruction register and decoded. The processor reads the operands from the register file and computes the next instruction address.
- Execute—The processor executes the instruction and saves the results in temporary registers. Pending traps are prioritized and internal traps taken during this stage.
- Write—If no trap is taken, the processor writes the result to the destination register.

All four stages operate in parallel, working on up to four different instructions at a time. A basic "single-cycle" instruction enters the pipeline and completes in four cycles. By the time it reaches the write stage, three more instructions have entered and are moving through the pipeline behind it. So, after the first four cycles, a single-cycle instruction exits the pipeline and a single-cycle instruction enters the pipeline on every cycle.

Of course, a "single-cycle" instruction actually takes four cycles to complete, but they are called single cycle because with this type of instruction the processor can complete one instruction per cycle after the initial four-cycle delay.

Concurrent Error Detection

Fault tolerance is supported using error detection logic. Almost all the registers of the chip are provided with parity bits so that concurrent self-checking is performed, transparent to the programmer. If an error occurs, the TSC691E will signal an error and trap to a special address depending of the error type. Six error types are defined: Restartable/Precise error, Non restartable/Precise error, Restartable/Late error, Non-restartable/Imprecise error, Register file error and Program Flow error.

Program flow Control: A checksum is verified against a precomputed value at each branch in the program flow. The TSC691E can also be used in checker mode. It is then possible to connect the checker IU in parallel with a master one, allowing comparison of the two chips.

Testability

A test access port (TAP) according to IEEE 1149.1, is included. The testability logic consists of four test data registers: bypass, boundary scan, internal scan and a device identification register. This interface provides standardized approaches to support of testing the integrated circuit itself and observing or modifying activity during the component's normal operation

TSC692E Floating-Point

The TSC692E Floating–Point Unit (FPU) is a high-performance, single–chip implementation of the SPARC reference floating–point unit. The TSC692E is designed to provide execution of single and double–precision floating–point instructions concurrently with execution of integer instructions by the TSC691E Integer Unit (IU). The TSC692E is compliant to the ANSI/IEEE-754 (1985) floating–point standard.

The TSC692E is designed for highly dependable space and military applications, and includes support for concurrent error detection and testability.

Description

The TSC692E uses a four stage instruction pipeline consisting of fetch, decode, execute and write stages (F, D, E and W). The fetch unit captures instructions and their addresses from the D[31:0] and A[31:0] busses. The decode unit contains logic to decode the floating–point instruction opcodes. The execution unit handles all instruction execution. The execution unit includes a floating–point queue (FP queue), which contains stored floating–point operate (FPop) instructions under execution and their addresses. The execution unit controls the load unit, the store unit, and the datapath unit.

The TSC692E depends upon the TSC691E to assert all addresses and control signals for memory access. Floating–point loads and stores are executed in conjunction with the TSC691E, which provides addresses and control signals while the TSC692E supplies or stores the data. Instruction fetch for integer and floating–point instructions is provided by the TSC691E.

The TSC692E provides three types of registers: f registers, FSR, and the FP queue. The FSR is a 32–bit status and control register. It keeps track of rounding modes, floating–point trap

types, queue status, condition codes, and various IEEE exception information. The floating–point queue contains the floating–point instruction currently under execution, along with its corresponding address.

Concurrent Error Detection

Fault tolerance is supported using error detection logic. Almost all the registers of the chip are provided with parity bits so that concurrent self-checking of the chip is performed, transparent to the programmer. Since the FPU only performs calculations, the solution for handling all errors detected by the internal concurrent error detection in the FPU is to handle them as exceptions. If an error occurs, the TSC692E will signal an error. Analysis of error type is possible by software assistance by reading FSR. Three error types are defined: Data Bus error, restartable error and non restartable error.

The TSC692E can also be used in checker mode. It is then possible to connect the checker FPU in parallel with a master one, allowing comparison of the two chips. If a discrepancy occurs, the TSC692E will signal an error.

Testability

A test access port (TAP) according to IEEE 1149.1, is included. The testability logic consists of four test data registers: bypass, boundary scan, internal scan and a device identification register. This interface provides standardized approaches to support of testing the integrated circuit itself and observing or modifying activity during the component's normal operation.

TSC693E Memory Controller

The TSC693E Memory Controller (MEC) is an ASIC which is designed for use with the SPARC Integer Unit (IU) TSC691E and SPARC Floating Point Unit (FPU) TSC692E. It interfaces directly to the address, data and control buses of the IU and FPU, requiring no additional components. It also interfaces directly to external memory and I/O units, only requiring additional buffers for the address and data bus. The TSC693E contains all necessary support functions to build a fault tolerant SPARC based computer.

Memory Interface

The TSC693E is configurable via register programming to interface with a number of different memory sizes and bit organizations. The TSC693E provides eight RAM memory chip selects. One, two, four or eight chip selects can be used depending on the programmed number of memory blocks. The TSC693E also provides two additional RAM chip selects to handle redundant memory blocks.

To decrease area, power consumption and mass, it is possible to boot the system from a single byte wide PROM.

In systems with multiple units accessing the main memory, there is a possibility of in-derterminism and deadlock. To avoid this, the TSC693E supports a dedicated exchange memory area (Dual Port RAM), which is used for interchange of data.
Four memory mapped I/O peripherals are supported.

The number of wait-states for different memory and I/O areas can be individually programmed :

- RAM Read 0 to 3 waitstates
- RAM Write 0 to 3 waitstates
- PROM Read 0 to 15 waitstates
- PROM Write 0 to 15 waitstates
- DPRAM Read / Write 0 to 15 waitstates
- I/O peripherals Read / Write 0 to 15 waitstates

The TSC693E also includes a memory access protection mechanism with a resolution of 64 pages for the RAM, one page for each I/O unit and one for the DPRAM area. It is possible to protect each page for read access, write access, execution access or combination of read, write and execution access.
If an access is attempted to a protected page, a memory exception is issued and the memory will not be updated.

Power Down Mode

There is a mode to reduce the power consumption which stops the IU execution and tri-states the bus drivers. This mode is entered by writing to a register in the TSC693E and left when it receives an interrupt.

Interrupts

Five external interrupts are provided by the TSC693E. They are programmable to be either active low or high, as well as either edge-trigged or level sensitive. The input signals are double latched in order to avoid glitches. An acknowledge signal is provided which is set if the specified external interrupt is active.

Test and Debug

The TSC693E has several mechanisms for test and debug purposes, including on-line test of hardware, software debug and error analysis:

- a Test Access Port (TAP) interface (IEEE standard 1149.1) for internal scan
- Testable error handling and error mask register
- Testable interrupt controller
- Testable system data bus parity
- Testable EDAC function
- Possibility to halt (freeze) the IU / FPU execution
- Possibility to use the write protection segments as watchpoints

Error Detection

The TSC693E includes parity checking on the external data bus, address bus, IU control bus and on all internal registers. The TSC693E also detects illegal register accesses, e.g. write to internal register in non supervisor mode or use of erroneous data sizes.
A watchdog with a separate watchdog clock and a programmable time-out is available. When the watchdog timer reaches zero, an interrupt occurs. If the watchdog is not written to within a programmable time after the interrupt, a system reset is issued.

Error Handler

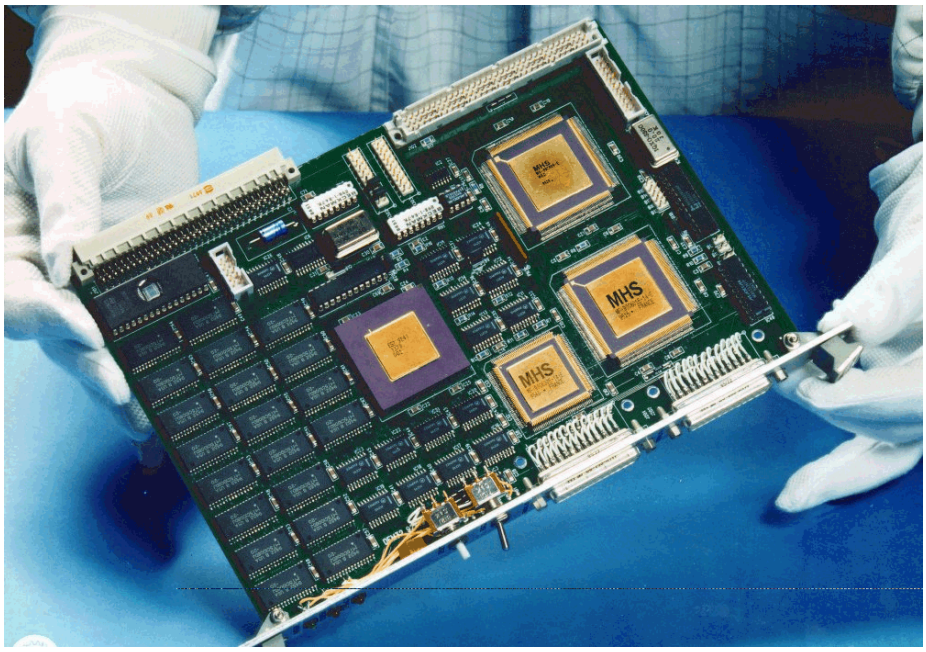
The TSC693E handles all error signals from the IU and FPU. When the TSC693E detects an internal or an external error, it performs one of the following four programmable actions :

1- Enters halt mode and stays there until reset
2- Issues a reset
3- Asserts an interrupt to the processor
4- Does nothing

UART

The TSC693E includes two double buffered full duplex asynchronous receiver-transmitters (UARTs). It is possible to use even parity, odd parity or no parity. One or two stop bits can be selected. It is also possible to select either 9600 baud or 19200 baud speed.
The UARTs generate an interrupt whenever a data word has been received, a data word has been transmitted or if an error is detected. The UART clock is either derived from the system clock or from the watchdog clock.

ESA / ERC32 evaluation board.



On-line Support

- World Wide Web (http://...):
  TEMIC: www.temic.de
  ESA: www.estec.esa.nl/wsmwww

Available Documentation

- TSC691E Datasheet / Users guide
- TSC692E Datasheet / Users guide
- TSC693E Datasheet / Users guide
- SPARC V7 instruction set

for more information on our products:
TEMIC Semiconductors Sales offices:
Europe : France Tel: (33) 1 30 60 7000 Fax: (33) 1 30 60 7111 / Germany Tel: (49) 7131 67 0 Fax: (49) 7131 67 2100 /
Italy Tel: (39) 2 332 12 332 Fax: (39) 2 332 12 234 / Spain Tel: (34) 1 564 5181 Fax: (34) 1 562 7514 /
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Japan : Tel.: (81) 35 562 33 21 Fax.: (81) 35 562 33 16
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Korea Tel.: (822) 785 1136 Fax.: (822) 785 1137 / Singapore Tel.: (65) 788 66 68 Fax.: (65) 788 00 31 /
Taiwan Tel.: (886) 2 755 61 08 Fax.: (886) 2 755 47 77
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