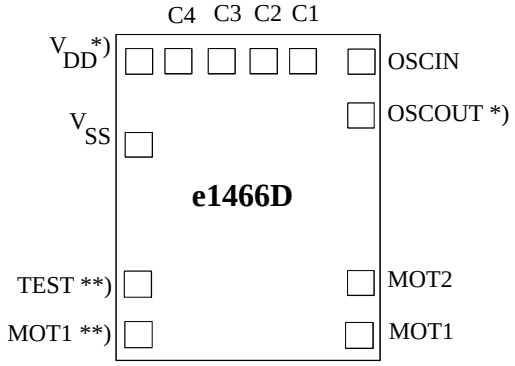
32 kHz Clock CMOS IC with Digital Trimming

Features

- 32 kHz crystal oscillator
- 1.1 - 2.2 V operating voltage range
- Integrated capacitors for digital trimming
- Suitable for up to 12.5 pF quartz
- Output pulse formers
- Mask options for motor period and pulse width
- Low resistance output for bipolar stepping motor
- Motor fast-test function

Pad Configuration



*) The pads V_{DD} and OSCOUT are interchangeable per mask option

**) The pads TEST and MOT1 are interchangeable per mask option

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Figure 1.

General Description

The e1466D is an integrated circuit in CMOS Silicon Gate Technology for analog clocks. It consists of a 32 kHz oscillator, frequency divider, output pulse formers and push-pull motor drivers. Integrated capacitors are mask-selectable to accomodate the external quartz crystal. Additional capacitance can be selected through pad bonding for trimming the oscillator frequency.

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	V_{SS}	–0.3 to 5 V	V
Input voltage range, all inputs	V_{IN}	$(V_{SS} - 0.3V) \leqq V_{IN} \leqq (V_{DD} + 0.3\ V)$	V
Output short circuit duration		indefinite	
Power dissipation (DIL package)	P_{tot}	125	mW
Operating ambient temperature range	T_{amb}	–20 to +70	°C
Storage temperature range	T_{stg}	–40 to +125	°C
Lead temperature during soldering at 2 mm distance, 10 seconds	T_{sld}	260	°C

Absolute maximum ratings define parameter limits which, if exceeded, may permanently change or damage the device.

All inputs and outputs on TEMIC circuits are protected against electrostatic discharges. However, precautions to minimize the build-up of electrostatic charges during handling are recommended.

The circuit is protected against supply voltage reversal for typically 5 minutes.

Functional Description

Oscillator

An oscillator inverter with feedback resistor is provided for generation of the 32768 Hz clock frequency. Values for the fixed capacitors at OSCIN and OSCOUT are mask-selectable (see note 3 of operating characteristics). Four capacitor pads, C1 to C4 enable the addition of integrated trimming capacitors to OSCIN, providing 15 tuning steps.

Trimming Capacitors

A frequency variation of typ. 4 ppm for each tuning step is obtained by bonding the capacitor pads to OSCIN. As none of these pads are bonded, the IC is in an untrimmed state. Figure 3 shows the trimming curve characteristic.

Note: For applications which utilize this integrated trimming feature, TEMIC will determine optimum values for the integrated capacitors C_{OSCIN} and C_{OSCOUT}.

Capacitor pads C1 to C4: 0 = open,
1 = connected to OSCIN.
Combination C1 + C4 is redundant and therefore eliminated from the list.

Capacitor Pads				Trimming Step
C4	C3	C2	C1	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	1	0	0	3
1	0	0	0	4
0	0	1	1	5
0	1	0	1	6
0	1	1	0	7
1	0	1	0	8
1	1	0	0	9
0	1	1	1	10
1	0	1	1	11
1	1	0	1	12
1	1	1	0	13
1	1	1	1	14

Motor Drive Output

The e1466D contains two push-pull output buffers for driving bipolar stepping motors. During a motor pulse, the n-channel device of one buffer and the p-channel device of the other buffer will be activated. Both n-channel transistors are on and conducting between output pulses. The outputs are protected against inductive voltage spikes with diodes to both supply pins. The motor output period and pulse width are mask-programmable, as listed below:

Available motor periods (T_M):
125, 250, 500 ms and 2, 16 s
Available max. pulse widths (t_M):
15, 6, 23.4, 31.25, 46.9 ms and 1 s
Available motor periods for motor test (T_{MT}):
250, 500 ms and 1 s

Note: The following constraints for combination of motor period and pulse widths have to be considered:
$T_M > 4 * t_M$, $T_{MT} > 4 * t_M$ or alternatively
$T_M = 2 * t_M$, $T_{MT} = 2 * t_M$

Test Functions

For test purposes, the TEST pad is open. With a high resistance probe ($R \geq 10\,M\Omega$, $C \geq 20$ pF), a test frequency f_{TEST} of 128 Hz can be measured at the TEST pad. Connecting TEST (for at least 32 ms) to V_{DD} changes the motor period from the selected value to T_{MT} (mask-selectable) while the pulse width remains unaffected. This feature can be used for testing the mechanical parts of the clock.

Operating Characteristics

V_{SS} = 0 V, V_{DD} = 1.5 V, T_{amb} = +25°C, unless otherwise specified
All voltage levels are measured with reference to V_{SS}. Test crystal as specified below.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Operating voltage		V_{DD}	1.1	1.5	2.2	V
Operating temperature		T_{amb}	–20		+70	°C
Operating current	R_1 = ∞, note 2	I_{DD}		2	5	µA
Motor drive output						
Motor output current	V_{DD} = 1.2 V, R_1 = 200 Ω	I_M	± 4.3			mA
Motor period		T_M	Mask option			
Motor period during motor test		T_{MT}	Mask option			
Motor pulse width		t_M	Mask option			
Oscillator						
Startup voltage	Within 2 s	V_{START}	1.2		2.2	V
Frequency stability	ΔV_{DD} = 100 mV, V_{DD} = 1.1 to 2.2 V	Δf/f		1		ppm
Integrated input capacitance	Note 3	C_{OSCIN}	Mask option			
Integrated output capacitance		C_{OSCOUT}	Mask option			
Integrated capacitance for bond option	Note 4 Note 4 Note 4 Note 4	C1 C2 C3 C4		3 4 5 6		pF pF pF pF
TEST input						
Input current	TEST = V_{DD} peak current	I_{TINH}	0.6	3	10	µA
Input current	TEST = V_{SS} peak current	I_{TINL}	–0.6	–3	–10	µA
Input debounce delay		t_{TIN}	23.4		31.2	ms

Note 1: Typical parameters represent the statistical mean values
Note 2: See test circuit
Note 3: Values can be selected in 1 pF steps. A total capacitance (C_{OSCIN} + C_{OSCOUT}) of 38 pF is available
Note 4: These values are valid for 10 pF quartz applications. For C_L = 12.5 pF these values change to 4.5, 6, 7.5, 9 pF

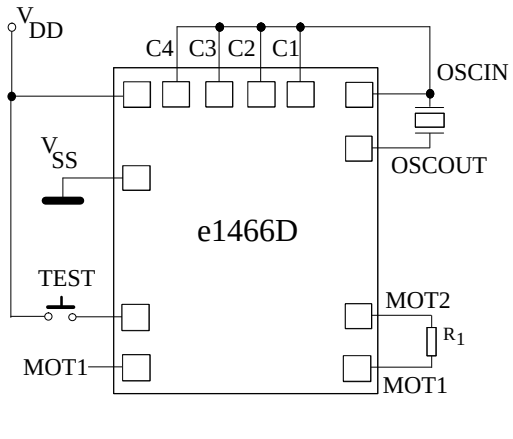

Figure 1. Functional test

Test Crystal Specification

Oscillation frequency	f_{OSC} = 32768 Hz
Series resistance	R_S = 30 kΩ
Static capacitance	C_0 = 1.5 pF
Dynamic capacitance	C_1 = 3.0 fF
Load capacitance	C_L optionally 10 or 12.5 pF

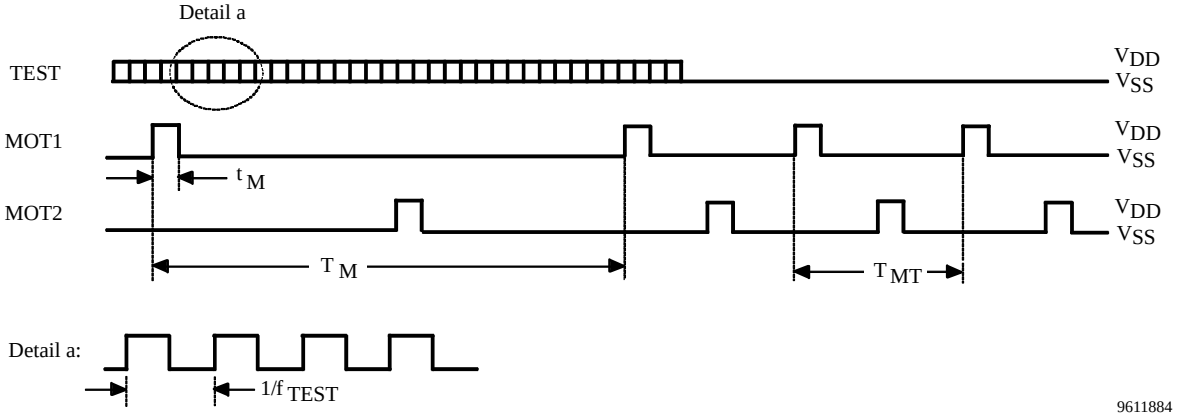

Figure 2. Motor output signal during normal operation and during motor test

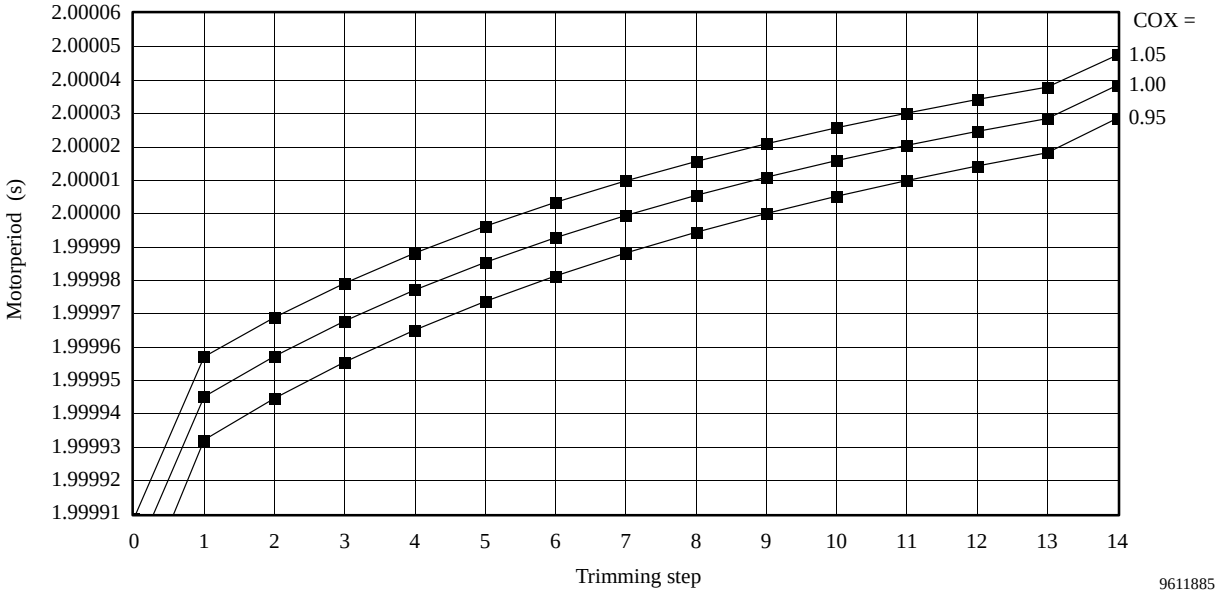

Figure 3. Typical trimming curve characteristic for T_M of 2 s

C_{OX} means frequency deviation due to production process variations.

Trimming inputs C1 ... C4 are binary weighted, i.e., C1 ... C4 = 0 corresponds to trimming step 0
C1 ... C4 = 1 corresponds to trimming step 15

LSB = C1

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