

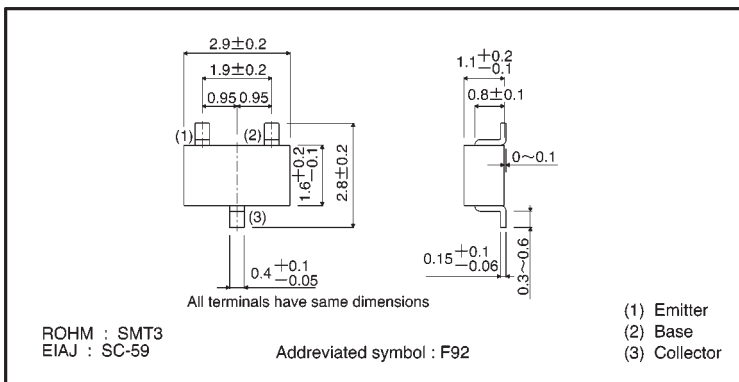
Digital transistors (built in resistor)

DTB123TK

●Features

- 1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- 2) The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- 3) Only the on/off conditions need to be set for operation, making device design easy.
- 4) Higher mounting densities can be achieved.

●External dimensions (Units: mm)



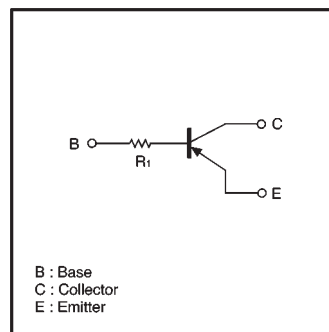
●Structure

PNP digital transistor
(Built-in resistor type)

●Absolute maximum ratings ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Collector-base voltage	V_{CBO}	-50	V
Collector-emitter voltage	V_{CEO}	-40	V
Emitter-base voltage	V_{EBO}	-5	V
Collector current	I_c	-500	mA
Collector power dissipation	P_c	200	mW
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55~+150	$^\circ\text{C}$

●Equivalent circuit



●Electrical characteristics (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV_{CBO}	-50	—	—	V	$I_C = -50 \mu A$
Collector-emitter breakdown voltage	BV_{CEO}	-40	—	—	V	$I_C = -1mA$
Emitter-base breakdown voltage	BV_{EBO}	-5	—	—	V	$I_E = -50 \mu A$
Collector cutoff current	I_{CBO}	—	—	-0.5	μA	$V_{CB} = -50V$
Emitter cutoff current	I_{EBO}	—	—	-0.5	μA	$V_{EB} = -4V$
Collector-emitter saturation voltage	$V_{CE(sat)}$	—	—	-0.3	V	$I_C/I_B = -50mA/-2.5mA$
DC current transfer ratio	h_{FE}	100	250	600	—	$V_{CE} = -5V, I_C = -50mA$
Input resistance	R_i	1.54	2.2	2.86	k Ω	
Transition frequency	f_T	—	200	—	MHz	$V_{CE} = -10V, I_E = 50mA, f = 100MHz$ *

* Transition frequency of the device

●Packaging specifications

Part No.	Package	SMT3
	Packaging type	Taping
	Code	T146
	Basic ordering unit (pieces)	3000
DTB123TK		○

●Electrical characteristic curves

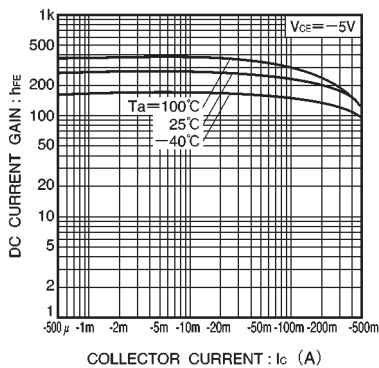


Fig.1 DC current gain vs. collector current

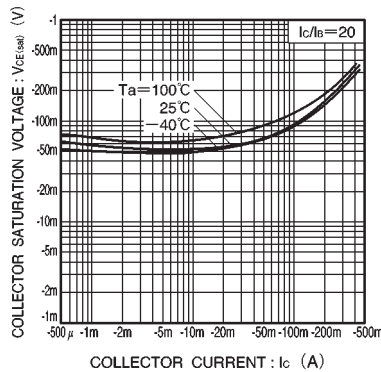


Fig.2 Collector-emitter saturation voltage vs. collector current