

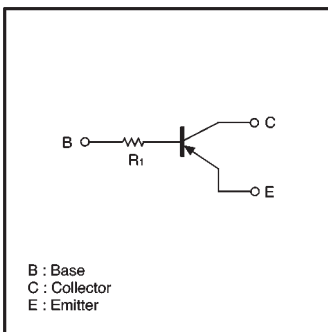
Digital transistors (built in resistor)

DTA124TE / DTA124TUA / DTA124TKA / DTA124TSA

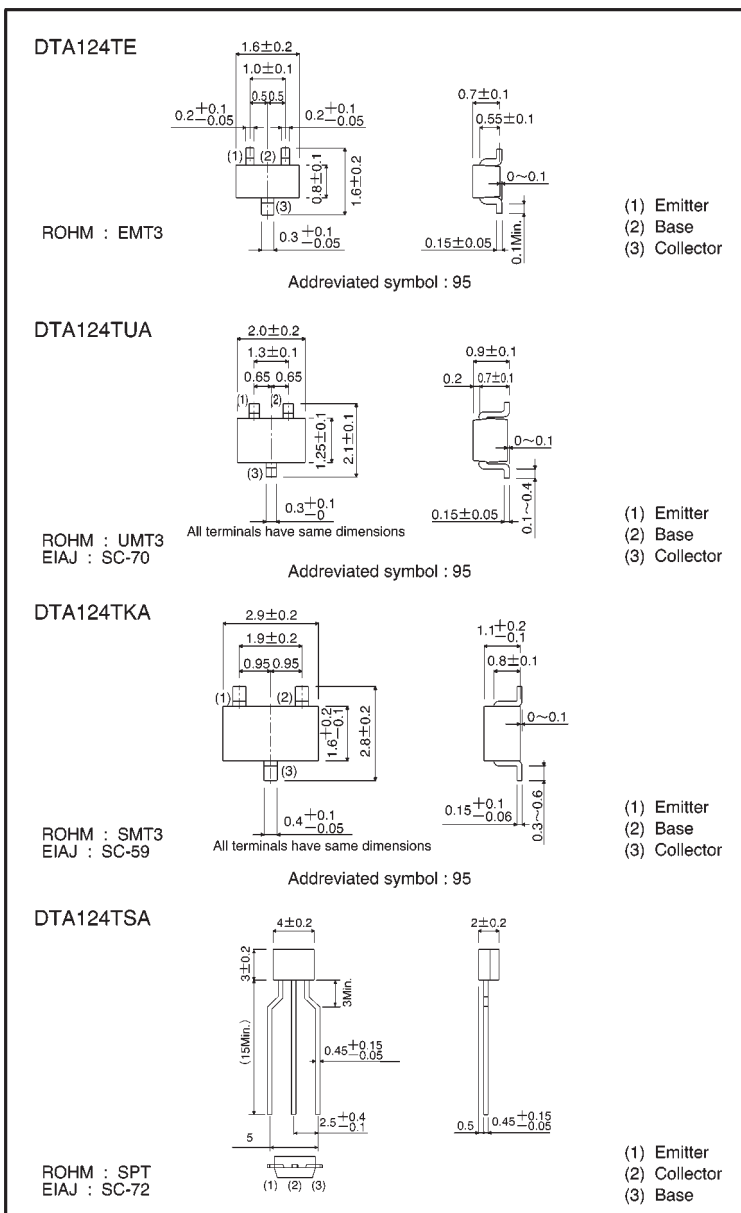
●Features

- 1) Built-in circuit enables the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- 2) The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- 3) Only the on/off conditions need to be set for operation, making device design easy.

●Equivalent circuit



●External dimensions (Units: mm)



● Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits(DTA124T□)				Unit
		E	UA	KA	SA	
Collector-base voltage	V _{CB0}	-50				V
Collector-emitter voltage	V _{CEO}	-50				V
Emitter-base voltage	V _{EB0}	-5				V
Collector current	I _c	-100				mA
Collector power dissipation	P _c	150	200	300		mW
Junction temperature	T _j	150				°C
Storage temperature	T _{stg}	-55~+150				°C

● Electrical characteristics (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV _{CB0}	-50	—	—	V	I _c = -50 μA
Collector-emitter breakdown voltage	BV _{CEO}	-50	—	—	V	I _c = -1mA
Emitter-base breakdown voltage	BV _{EB0}	-5	—	—	V	I _E = -50 μA
Collector cutoff current	I _{CB0}	—	—	-0.5	μA	V _{CB} = -50V
Emitter cutoff current	I _{EB0}	—	—	-0.5	μA	V _{EB} = -4V
Collector-emitter saturation voltage	V _{CE(sat)}	—	—	-0.3	V	I _c /I _b = -5mA/-0.5mA
DC current transfer ratio	h _{FE}	100	250	600	—	V _{CE} = -5V, I _c = -1mA
Input resistance	R _i	15.4	22	28.6	kΩ	—
Transition frequency	f _r	—	250	—	MHz	V _{CE} = -10V, I _E = 5mA, f = 100MHz *

* Transition frequency of the device

● Packaging specifications

Part No.	Package	EMT3	UMT3	SMT3	SPT
	Package type	Taping	Taping	Taping	Taping
	Code	TL	T106	T146	TP
	Basic ordering unit (pieces)	3000	3000	3000	5000
DTA124TE	○	—	—	—	—
DTA124TUA	—	○	—	—	—
DTA124TKA	—	—	○	—	—
DTA124TSA	—	—	—	○	—

● Electrical characteristic curves

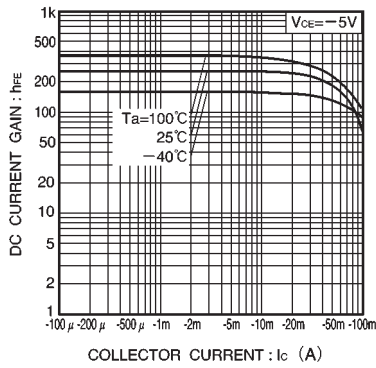


Fig.1 DC current gain vs. collector current

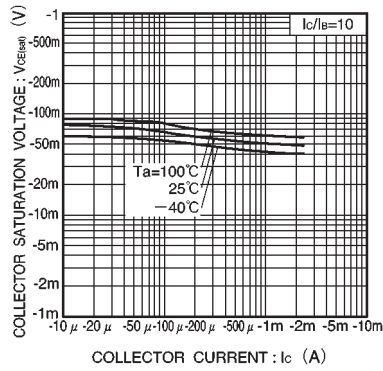


Fig.2 Collector-emitter saturation voltage vs. collector current