

SANYO	No.3053	DM1621
		16 Characters x 2 Lines LIQUID CRYSTAL DOT MATRIX DISPLAY MODULE

General Description

The DM1621 is a liquid crystal dot matrix display module that consists of LCD panel, LCD control driver, driver and is capable of providing (16 characters x 2 lines) display. It contains a controller, a data RAM, and a character generator ROM required for providing display. Data interfacing is in 8-bit parallel or 4-bit parallel and data can be written in or read from a microprocessor.

General Specifications

- | | |
|--------------------------------|---|
| 1. Display system | 1/5 bias 1/16 duty |
| 2. Display content | 16 characters x 2 lines |
| 3. Dots organizing 1 character | 5 x 8 dots/character |
| 4. Display data RAM | 80-character (80 x 8 bits) |
| 5. Character generator ROM | 160-character JIS font set + 32-character special font set
Refer to Table 1. |
| 6. Character generator RAM | 64 x 8 bits 5 x 7 dots 8 characters |
| 7. Instruction function | Refer to Table 2. |
| 8. Circuit diagram | Refer to Fig. 3. |

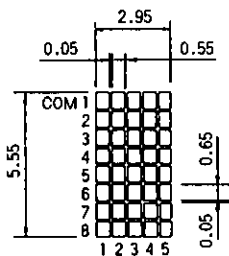
Outline

- | | |
|--------------------------------|--------------------------------|
| 1. Module outline | 44.0(W) x 84.0(L) x 10(T) [mm] |
| 2. View area | 60.5 x 14.4 [mm] |
| 3. Dot size | 0.55 x 0.65 [mm] |
| 4. Dot pitch | 0.60 x 0.70 [mm] |
| 5. Character size (5 x 8 dots) | 2.95 x 5.55 [mm] |

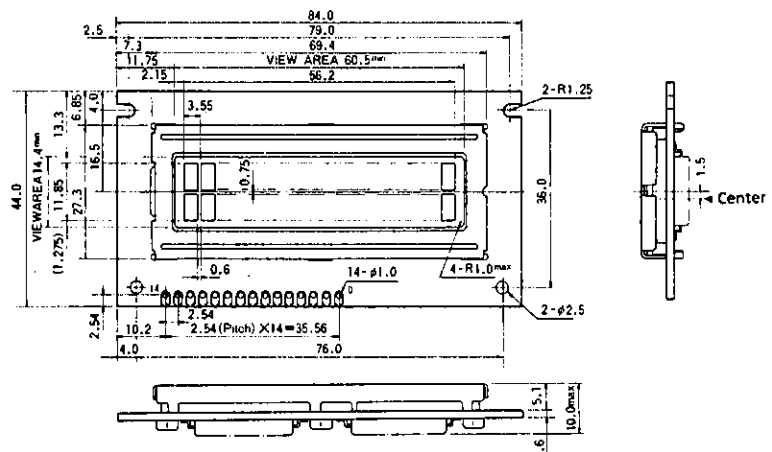
Absolute Maximum Ratings at Ta = 25°C

			unit
Supply Voltage	$V_{DD} - V_{SS}$	- 0.3 to + 6	V
Input Voltage	V_I	- 0.3 to $V_{DD} + 0.3$	V
Drive Voltage	$V_{DD} - V_O$	- 0.3 to + 13.5	V
Operating Temperature	T_{opr}	0 to + 50	°C
Storage Temperature	T_{stg}	- 20 to + 70	°C

Display Pattern



Module Dimensions 5010
(unit: mm)

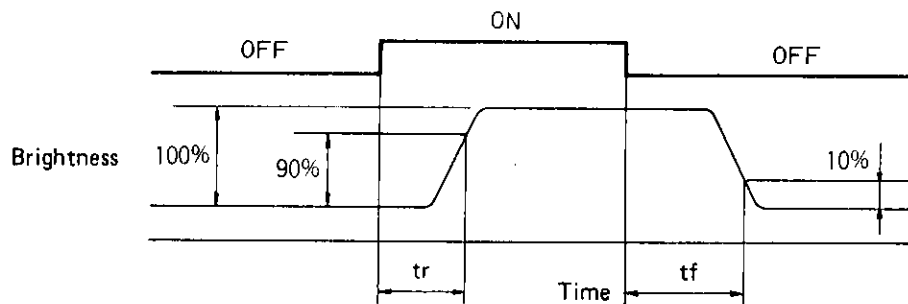


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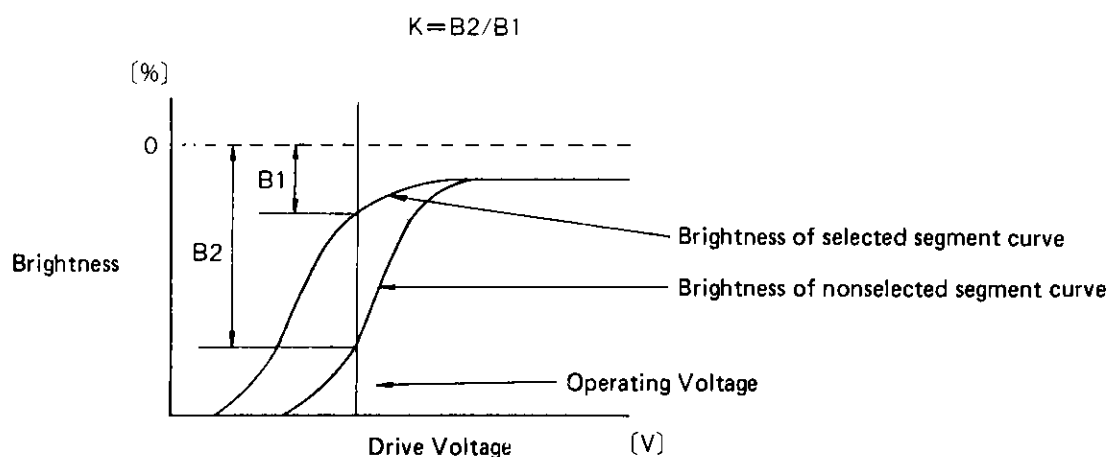
Electro Optical Characteristics at $V_{DD} - V_{SS} = 5.0V, T_a = 25^\circ C$ unless otherwise specified

			min	typ	max	unit
Input "High" Voltage	V_{IH}		2.2		V_{DD}	V
Input "Low" Voltage	V_{IL}		0		0.5	V
Output "High" Voltage	V_{OH}	DB0 to DB7, $-I_{OH} = 0.2mA$	2.4			V
Output "Low" Voltage	V_{OL}	DB0 to DB7, $I_{OL} = 1.2mA$			0.4	V
Input Current	I_P	Pull-up MOS, $V_{DD} = 5V$	50	125	250	μA
Current Dissipation	I_{DD}	No input/output current included		1.5	3.0	mA
Oscillation Frequency	F_{OSC}		190	270	350	kHz
Viewing Angle	$\phi 2 - \phi 1$	$K = 1.4 \quad \theta = 0^\circ$				degree
Contrast Ratio	K	$\phi = 20^\circ \quad \theta = 0^\circ$	3.0			
Rise Time	t_r	$\phi = 20^\circ \quad \theta = 0^\circ$		150	250	ms
Fall Time	t_f	$\phi = 20^\circ \quad \theta = 0^\circ$		150	250	ms
LCD Drive Voltage (Recommended Value)	$V_{DD} - V_O$	$T_a = 0^\circ C, \phi = 20^\circ, \theta = 0^\circ, K \geq 3$	4.4	4.5	4.6	V
		$T_a = 25^\circ C, \phi = 20^\circ, \theta = 0^\circ, K \geq 3$	4.0	4.1	4.2	V
1/16 Duty		$T_a = 50^\circ C, \phi = 20^\circ, \theta = 0^\circ, K \geq 3$	3.4	3.5	3.6	V

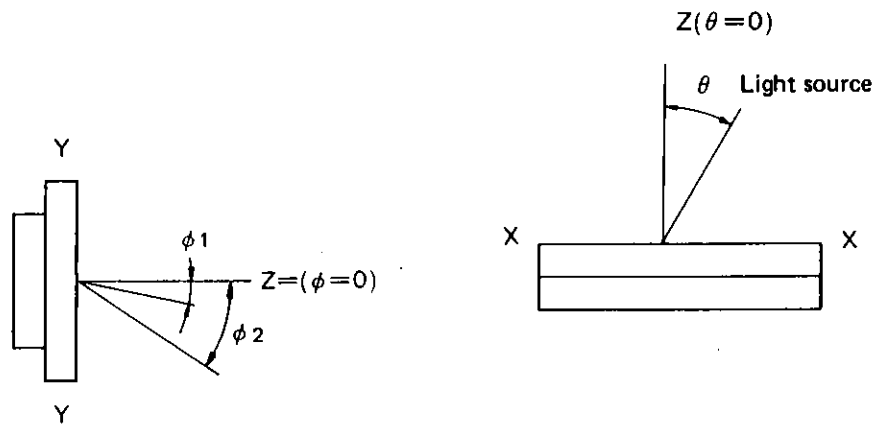
(1) Test Condition for Response Time (t_r, t_f)



(2) Definition of Contrast (K)



(3) Contrast Ratio Measuring Method



Angles ϕ and θ are defined shown above.

The light source is placed in the θ direction at an angle of 30° and the sensor is placed in the ϕ direction to measure the contrast.

Pin Description

No.	Pin Name	Function
1	V_{SS}	(-) power supply pin 0V
2	V_{DD}	(+) Power supply pin + 5V
3	V_O	Pin for applying LCD drive voltage
4	RS	Input pin HI = Data LOW = Instruction
5	R/W	Input pin HI = Read LOW = Write
6	E	Input pin Enable signal
7	DB0	Data bus line
8	DB1	
9	DB2	
10	DB3	
11	DB4	
12	DB5	
13	DB6	
14	DB7	

Note 1. The LCD drive voltage can be varied from 3V to 5V by a variable resistor of $5k\Omega$ connected across V_{SS} and V_O .

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Timing Characteristics

			min	typ	max	unit
Enable Cycle Time		t_{cyce}	1000			ns
Enable Pulse Width	High level	P_{WEH}	450			ns
Enable Rise/Fall Time		t_{Er}, t_{Ef}			25	ns
Set up Time	RS/RW-E	t_{As}	140			ns
Address Hold Time		t_{AH}	10			ns
Data Delay Time		t_{DDR}			320	ns
Data Set Up Time		t_{DSW}	195			ns
Data Hold Time		$t_H (t_{DHR})$	10 (20)			ns

Figs. 1, 2

Write Operation

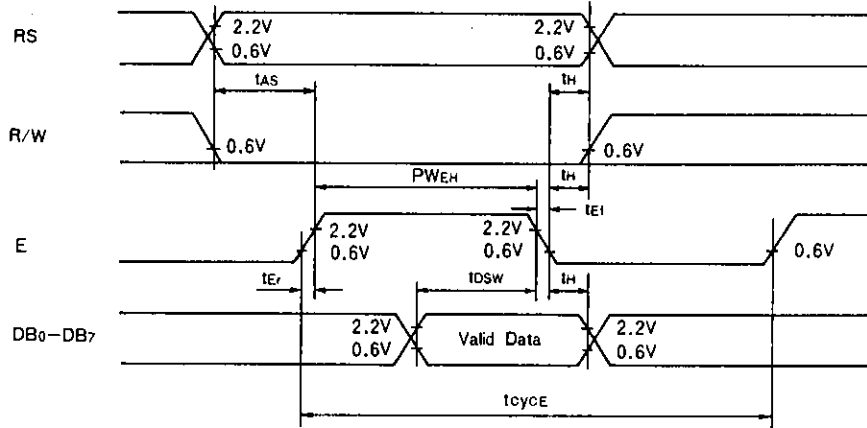


Fig.1 Interface Timing (Data Write)

Read Operation

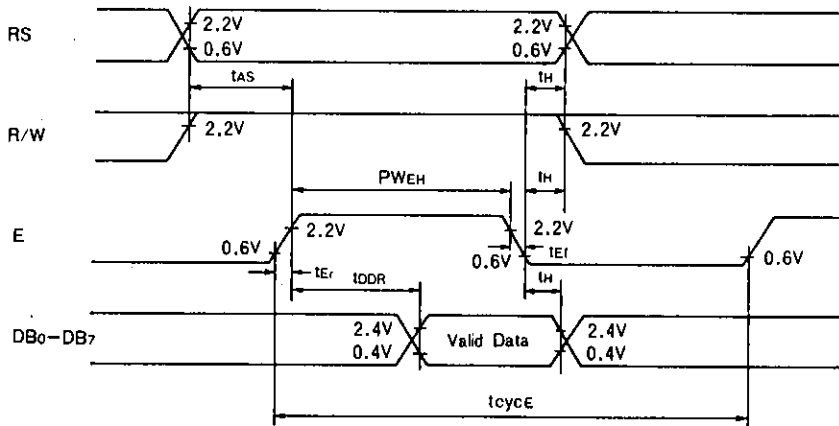


Fig.2 Interface Timing (Data Read)

Table 1 Character Code

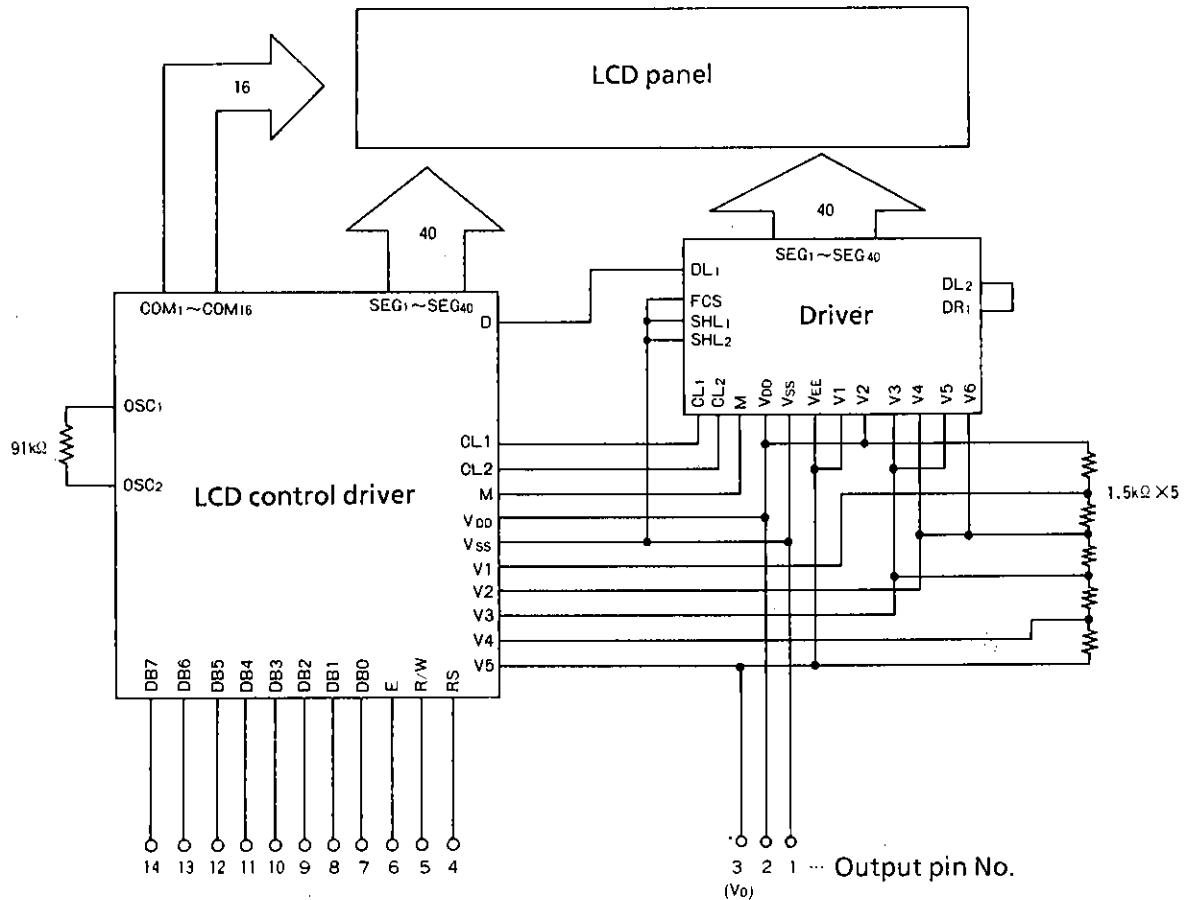
Low-order 4 bits \ Hi-order 4bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)		Q	a	P	\	P		-	9	E	o	p
xxxx0001	(2)	!	l	A	O	a	9	e	7	*	4	a	q
xxxx0010	(3)	"	2	R	b	r	r	4	u	x		p	e
xxxx0011	(4)	#	3	C	S	c	s	j	9	7	e	e	w
xxxx0100	(5)	\$	4	D	T	d	t	\	I	I	†	P	a
xxxx0101	(6)	%	5	E	U	e	u	.	*	+	1	e	o
xxxx0110	(7)	&	6	F	V	f	v	9	0	=	3	p	z
xxxx0111	(8)	'	7	G	W	g	w	7	†	7	9	g	m
xxxx1000	(1)	(B	H	K	h	k	x	4	o	*	u	r
xxxx1001	(2))	9	I	Y	i	y	e	7	1	u	'	y
xxxx1010	(3)	*	#	J	Z	j	z	x	3	n	v	j	*
xxxx1011	(4)	+	#	K	L	k	l	\	*	9	E	*	m
xxxx1100	(5)	,	<	L	*	l	l	†	9	7	9	e	m
xxxx1101	(6)	-	=	M	N	m	n	\	a	z	\	t	+
xxxx1110	(7)	.	>	N	\	n	+	9	E	†	9	n	
xxxx1111	(8)	/	?	O	_	o	+	w	v	7	#	o	

(Note) The CG RAM is a character generator RAM used to store the character patterns that can be program-rewritten, as desired, by the user.

Table 2 Instruction function

Instruction	Code										Contents	Execution Time (f _{OSC} =250kHz)	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Display clear	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (address 0).	82μs ~ 1.64ms	
Cursor home	0	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (address 0). Also returns the display being shifted to the original position. The DD RAM contents remain unaffected.	40μs ~ 1.6ms
Entry mode set	0	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies whether to or not to shift the display. These operations are performed during data write and read.	40μs
Display ON/OFF control	0	0	0	0	0	0	0	1	D	C	B	Sets all display ON/OFF(D), cursor ON/OFF(C), cursor position character blink (B).	40μs
Cursor/display shift	0	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without affecting the DD RAM contents.	40μs
Function set	0	0	0	0	1	DL	N	F	*	*	Sets the interface data length (DL), number of display lines (L), and character font (F).	40μs	
CG RAM address set	0	0	0	1	A _{CG}						Sets the CG RAM address. RAM data is sent/received after this setting.	40μs	
DD RAM address set	0	0	1	A _{DD}						Sets the DD RAM address. DD RAM data is sent/received after this setting.	40μs		
Busy flag/address read	0	1	BF	AC						Reads the contents of busy flag (BF) indicating internal operation is in progress and reads the contents of address counter.	1μs		
CG RAM/DD RAM data write	1	0	Write Data						Writes data into the DD RAM or CG RAM.	40μs			
CG RAM/DD RAM data read	1	1	Read Data						Reads data from the DD RAM or CG RAM.	40μs			
	I/D = 1 : Increment (+1) I/D = 0 : Decrement (-) S = 1 : Accompanied by display shift S/C = 1 : Display shift S/C = 0 : Cursor move R/L = 1 : Right-shift R/L = 0 : Left-shift DL = 1 : 8 bits DL = 0 : 4 bits N = 1 : 2 lines N = 0 : 1 line F = 1 : 5 x 10 dots F = 0 : 5 x 7 dots BF = 1 : Internally operating BF = 0 : Possible to accept instruction										DD RAM : Display data RAM CG RAM : Character generator RAM A _{CG} : CG RAM address A _{DD} : DD RAM address Corresponds to cursor address. AC : Address counter used for both DD RAM and CG RAM.	The change in the frequency (f _{OSC}) also causes the execution time to be changed. (Example) When f _{OSC} =270kHz, 40μs x 250/270 ≈37μs.	

Fig.3 Circuit Diagram DM1621



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