

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4511B **MSI** BCD to 7-segment latch/decoder/driver

Product specification
File under Integrated Circuits, IC04

January 1995

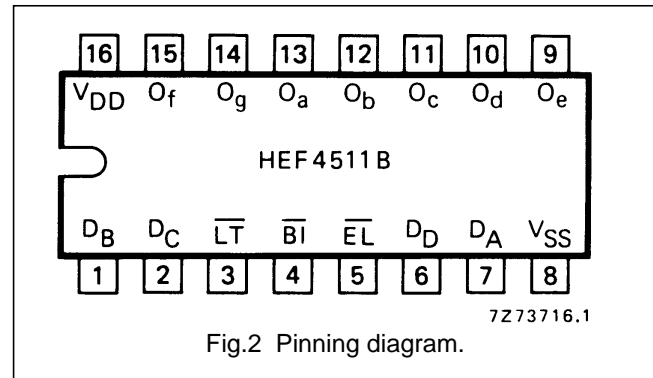
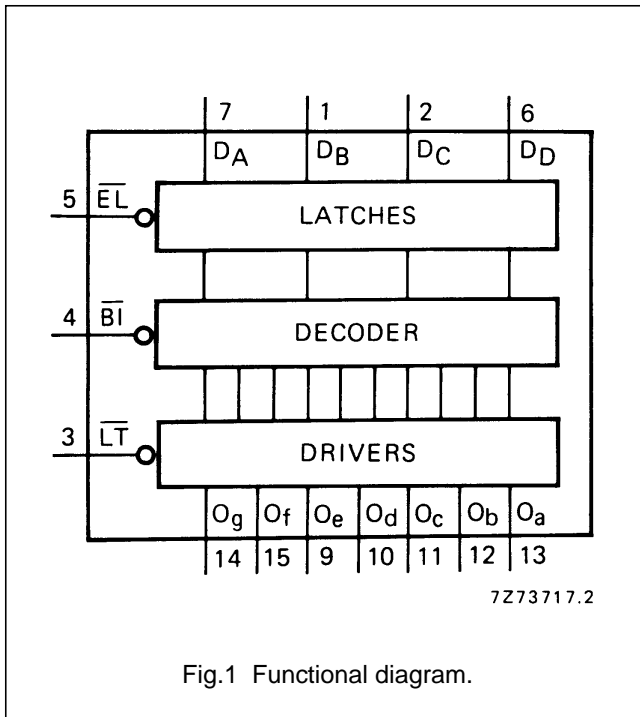
BCD to 7-segment latch/decoder/driver

HEF4511B MSI

DESCRIPTION

The HEF4511B is a BCD to 7-segment latch/decoder/driver with four address inputs (D_A to D_D), an active LOW latch enable input (\overline{EL}), an active LOW ripple blanking input (\overline{BI}), an active LOW lamp test input (\overline{LT}), and seven active HIGH n-p-n bipolar transistor segment outputs (O_a to O_g).

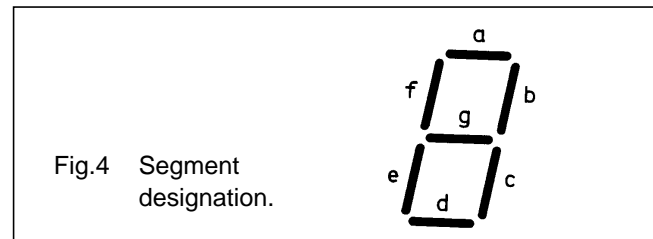
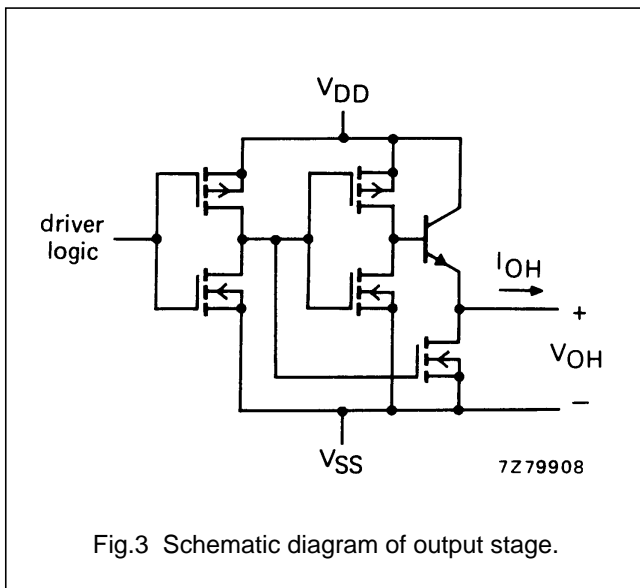
When \overline{EL} is LOW, the state of the segment outputs (O_a to O_g) is determined by the data on D_A to D_D . When \overline{EL} goes HIGH, the last data present on D_A to D_D are stored in the latches and the segment outputs remain stable. When \overline{LT} is LOW, all the segment outputs are HIGH independent of all other input conditions. With \overline{LT} HIGH, a LOW on \overline{BI} forces all segment outputs LOW. The inputs \overline{LT} and \overline{BI} do not affect the latch circuit.



- HEF4511BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4511BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4511BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

PINNING

- D_A to D_D address (data) inputs
- \overline{EL} latch enable input (active LOW)
- \overline{BI} ripple blanking input (active LOW)
- \overline{LT} lamp test input (active LOW)
- O_a to O_g segment outputs



FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

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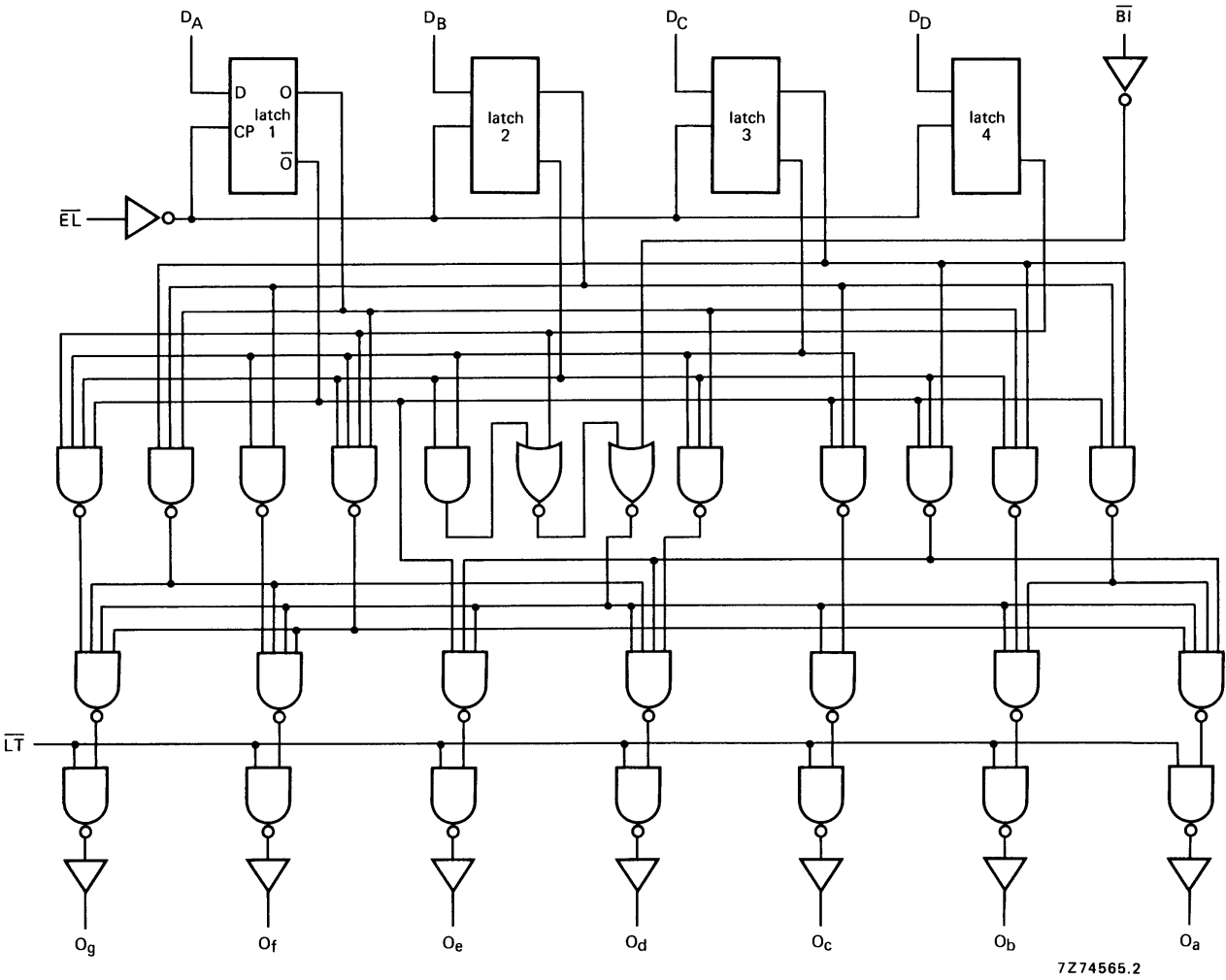


Fig.5 Logic diagram; for one latch see Fig.6.

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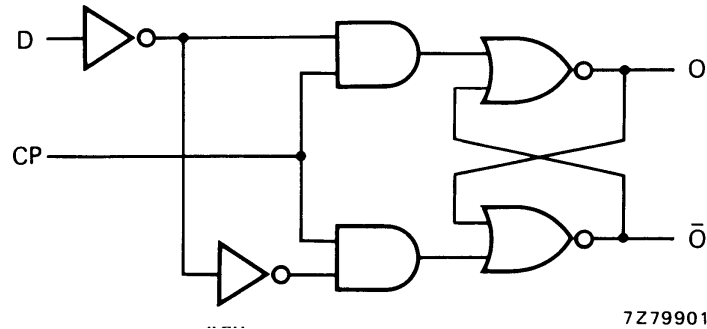


Fig.6 Logic diagram (one latch); see also Fig.5.

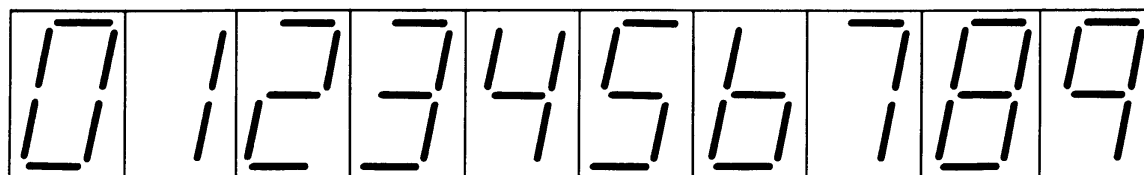
FUNCTION TABLE

INPUTS							OUTPUTS							
\overline{EL}	\overline{BI}	\overline{LT}	D_D	D_C	D_B	D_A	O_a	O_b	O_c	O_d	O_e	O_f	O_g	DISPLAY
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	blank
H	H	H	X	X	X	X				*				*

Note

- H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
* Depends upon the BCD code applied during the LOW to HIGH transition of \overline{EL} .

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Fig.7 Display.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).

Output (source) current HIGH $-I_{OH}$ max. 25 mA

For other RATINGS see Family Specifications.

Note

1. A destructive high current mode may occur if V_I and V_O are not constrained to the range $V_{SS} \leq V_I$ or $V_O \leq V_{DD}$.

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DC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$

HEF	V_{DD} V	I_{OH} mA	SYMBOL	T_{amb} (°C)					
				-40		+ 25		+ 85	
				MIN.	MAX.	MIN.	TYP.	MIN.	MAX.
Output voltage HIGH	5	0	V_{OH}	4,10		4,10	4,40	4,10	V
	10	0		9,10		9,10	9,40	9,10	V
	15	0		14,10		14,10	14,40	14,10	V
Output voltage HIGH	5	5	V_{OH}				4,20		V
	10	5					9,20		V
	15	5					14,20		V
Output voltage HIGH	5	10	V_{OH}	3,60		3,60	4,05	3,30	V
	10	10		8,75		8,75	9,10	8,45	V
	15	10		13,75		13,75	14,10	13,45	V
Output voltage HIGH	5	15	V_{OH}				4,00		V
	10	15					9,00		V
	15	15					14,00		V
Output voltage HIGH	5	20	V_{OH}	2,80		2,80	3,80	2,50	V
	10	20		8,10		8,10	9,00	7,80	V
	15	20		13,10		13,10	14,00	12,80	V
Output voltage HIGH	5	25	V_{OH}				3,70		V
	10	25					8,90		V
	15	25					14,00		V

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HEC	V _{DD} V	I _{OH} mA	SYMBOL	T _{amb} (°C)					
				-55		+ 25		+ 125	
				MIN.	MAX.	MIN.	TYP.	MIN.	MAX.
Output voltage HIGH	5	0	V _{OH}	4,10		4,10	4,40	4,10	V
	10	0		9,10		9,10	9,90	9,10	V
	15	0		14,10		14,10	14,40	14,40	V
Output voltage HIGH	5	5	V _{OH}				4,30		V
	10	5					9,30		V
	15	5					14,30		V
Output voltage HIGH	5	10	V _{OH}	3,60		3,60	4,25	3,20	V
	10	10		8,75		8,75	9,25	8,35	V
	15	10		13,75		13,75	14,25	13,35	V
Output voltage HIGH	5	15	V _{OH}				4,20		V
	10	15					9,20		V
	15	15					14,20		V
Output voltage HIGH	5	20	V _{OH}	2,80		2,80	4,20	2,30	V
	10	20		8,10		8,10	9,20	7,60	V
	15	20		13,10		13,10	14,20	12,60	V
Output voltage HIGH	5	25	V _{OH}				4,15		V
	10	25					9,20		V
	15	25					14,20		V

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	1 000 f _i + ∑ (f _o C _L) × V _{DD} ² 4 000 f _i + ∑ (f _o C _L) × V _{DD} ² 10 000 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)

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AC CHARACTERISTICS

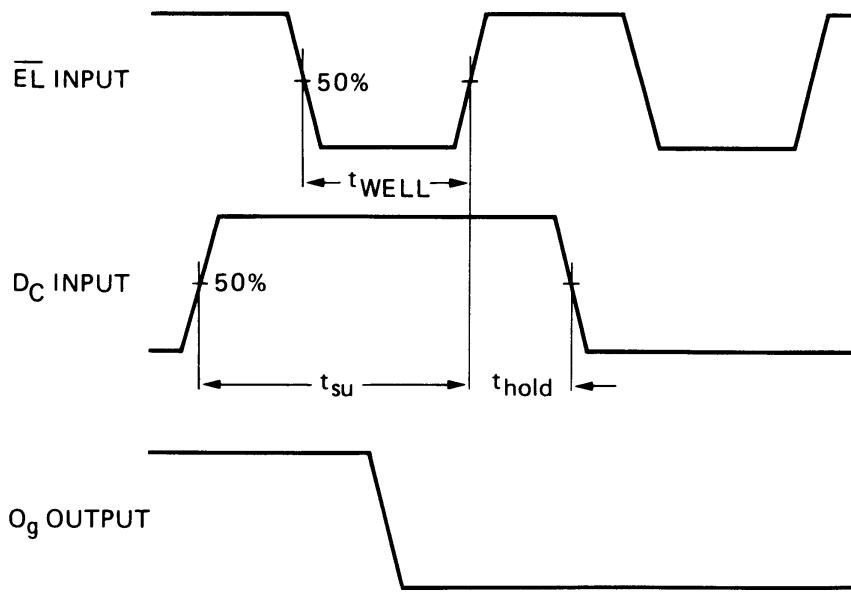
 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA							
Propagation delays	5	t_{PHL}											
							10	HIGH to LOW	155	310	ns	$128\text{ ns} + (0,55\text{ ns/pF}) C_L$	
									60	120	ns	$49\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	40								80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$		
	15						LOW to HIGH	135	270	ns	$108\text{ ns} + (0,55\text{ ns/pF}) C_L$		
								55	110	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$		
								40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$		
	5						t_{PHL}						
													10
		60	120	ns	$49\text{ ns} + (0,23\text{ ns/pF}) C_L$								
	45	90	ns	$37\text{ ns} + (0,16\text{ ns/pF}) C_L$									
	15	LOW to HIGH	160	320	ns	$133\text{ ns} + (0,55\text{ ns/pF}) C_L$							
			70	140	ns	$59\text{ ns} + (0,23\text{ ns/pF}) C_L$							
			50	100	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$							
	5	t_{PHL}											
							50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$			
	35						70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$				
	15						LOW to HIGH	105	210	ns	$78\text{ ns} + (0,55\text{ ns/pF}) C_L$		
								40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$		
								30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$		
	5						t_{PHL}						
		30	60	ns	$19\text{ ns} + (0,23\text{ ns/pF}) C_L$								
20	40	ns	$12\text{ ns} + (0,16\text{ ns/pF}) C_L$										
15	LOW to HIGH	60	120	ns	$33\text{ ns} + (0,55\text{ ns/pF}) C_L$								
		30	60	ns	$19\text{ ns} + (0,23\text{ ns/pF}) C_L$								
		25	50	ns	$17\text{ ns} + (0,16\text{ ns/pF}) C_L$								
Output transition times	5	t_{THL}											
													10
							30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$			
	20						40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$				
	15						LOW to HIGH	25	50	ns	$20\text{ ns} + (1,0\text{ ns/pF}) C_L$		
								16	32	ns	$13\text{ ns} + (0,06\text{ ns/pF}) C_L$		
13		26	ns	$10\text{ ns} + (0,06\text{ ns/pF}) C_L$									

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	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Minimum \overline{EL} pulse width; LOW	5	t_{WELL}	80	40	ns	see also waveforms Fig.8
	10		40	20	ns	
	15		35	17	ns	
Set-up time $D_n \rightarrow \overline{EL}$	5	t_{su}	50	25	ns	
	10		25	12	ns	
	15		20	9	ns	
Hold-time $D_n \rightarrow \overline{EL}$	5	t_{hold}	60	30	ns	
	10		30	15	ns	
	15		25	12	ns	



Conditions:
 $D_D = \text{LOW}$
 $D_A = D_B = \overline{B}_1 = \overline{L}\overline{T} = \text{HIGH}$

Fig.8 Waveforms showing minimum \overline{EL} pulse width, set-up and hold time for D_C to \overline{EL} .

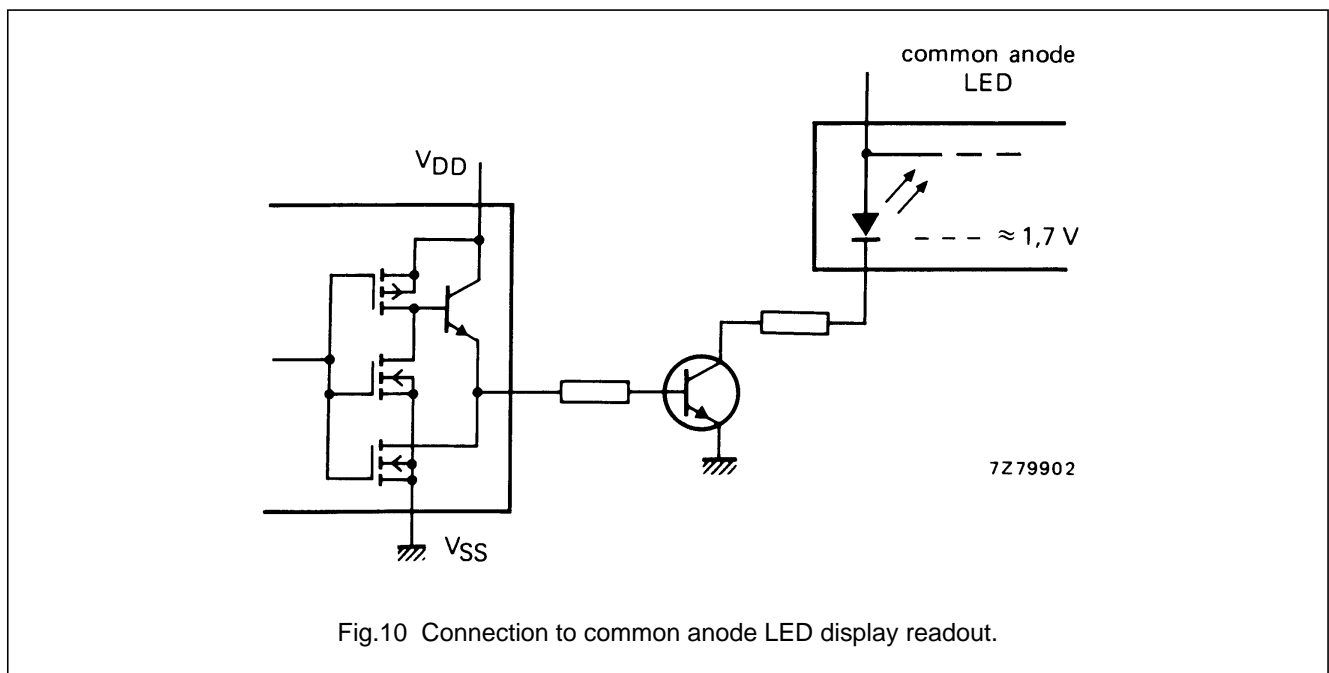
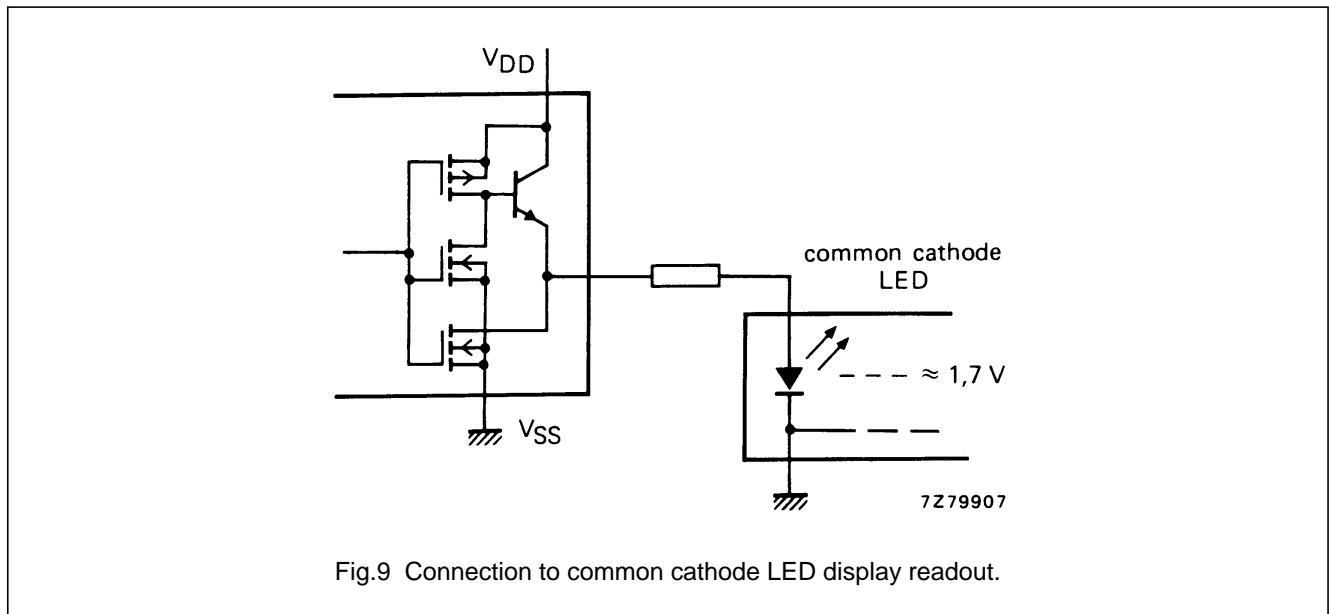
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APPLICATION INFORMATION

Some examples of applications for the HEF4511B are:

- Driving LED displays.
- Driving incandescent displays.
- Driving fluorescent displays.
- Driving LCD displays.
- Driving gas discharge displays.



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