Shock Sensor Signal Processor
BU3892FV

The BU3892FV is an IC that processes the signals from shock sensors like those used in HDD and CD-ROM drives. This IC receives the faint signals output by shock sensors in response to vibration, and output a shock detection signal when they exceed a certain level.

●Applications
HDD and CD-ROM drives

●Features
1) Single 5V power supply
2) Low-input bias current (CMOS)
3) Low power consumption mode
4) SSOP-B 16 pin package

●Absolute maximum ratings (Ta=25℃)

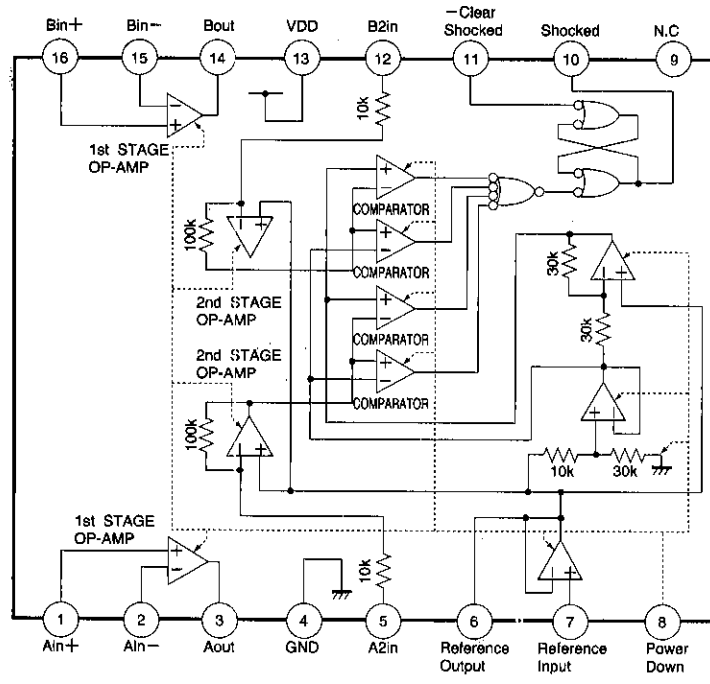
Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	−0.3~7.0	V
Power dissipation	P_D	300*	mW
Storage temperature	T_{STG}	−55~125	℃
Input voltage	V_{IN}	−0.3~V_{DD}+0.3	V
Output voltage	V_{OUT}	−0.3~V_{DD}+0.3	V

* Reduced by 3mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta=25℃)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	4.5~5.5	V
Input voltage, LOW level	V_{IL}	−0.3~1.5	V
Iutput voltage, HIGH level	V_{IH}	3.5~V_{DD}+0.3	V
Operating temperature	T_{OPR}	0~70	℃

●Block diagram



●Pin descriptions

Pin No.	Name	Function
1	Ain+	Forward input of 1st stage operational amplifier A
2	Ain−	Reverse input of 1st stage operational amplifier A
3	Aout	Output of 1st stage operational amplifier A
4	GND	Ground
5	A2in	Input of 2nd stage reversing amplifier
6	Reference Output	Reference voltage output (typically 2 V)
7	Reference Input	Reference voltage input (typically 2 V)
8	Power Down	Power-down signal input (The IC enters the power-down mode when the high-level signal is input.)
9	N.C	Not connected inside the IC.
10	Shocked	Shock detection output. Outputs the high level when a shock is detected. (The high level is maintained until pin 11 input changes to the low level.)
11	−Clear Shocked	Shocked clear input Shocked output is cleared when the level changes to low.
12	B2in	2nd stage reversing amplifier input
13	V_{DD}	Power supply
14	Bout	1st stage operational amplifier B output
15	Bin−	1st stage operational amplifier B reverse input
16	Bin+	1st stage operational amplifier B forward input

●Electrical characteristics (unless otherwise noted, Ta=25℃, V_{DD}=4.5 ~ 5.5V)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
〈1st STAGE〉								
Input bias current	Ta=25℃	IIB_{1ST}	—	1	20	pA	Measured at Ain+, Ain-, Bin+, Bin- and GND*2	Fig.1
	Ta=75℃		—	—	2000			
Maximum output current		IO_{1ST}	0.5	—	—	mA		Fig.1
Supply voltage rejection ratio		SVR_{1ST}	65	—	—	dB	*2	Fig.1
Voltage gain bandwidth		GB_{1ST}	—	1.4	—	MHz		Fig.1
High-amplitude voltage gain		AV_{1ST}	10	—	—	V/mV		Fig.1
〈REFERENCE INPUT〉								
Input current		I_{REF}	—	—	10	μA	Reference Input=2V	Fig.1
Output impedance		RO_{REF}	—	—	30	Ω	Reference Input=2V	Fig.1
〈2nd STAGE〉								
Input current (A2in, B2in)		I_{I2nd}	−11	−16	−22	μA	Reference Input=2V A2in, B2in=1.8V	Fig.1
Threshold voltage, high level (A2in, B2in)		DVH_{2nd}	+0.04	+0.05	+0.06	V	Reference Input=2V −Clear Shocked=0V Value relative to reference input	Fig.1
Threshold voltage, low level (A2in, B2in)		DVH_{2nd}	−0.06	−0.05	−0.04			
〈TOTAL〉								
Recovery time from power down		T_{RCVRY}	—	—	1	mS	Time required for operation within specifications*2,3	Fig.2
Supply current		I_{DD}	—	4	6.5	mA	Input at power down low level	Fig.1
			—	15	100	μA	Input at power down high level	Fig.1

*2 Guaranteed performance

*3 Shocked: The high level is output during transition in the power down low level.

●Measurement circuit

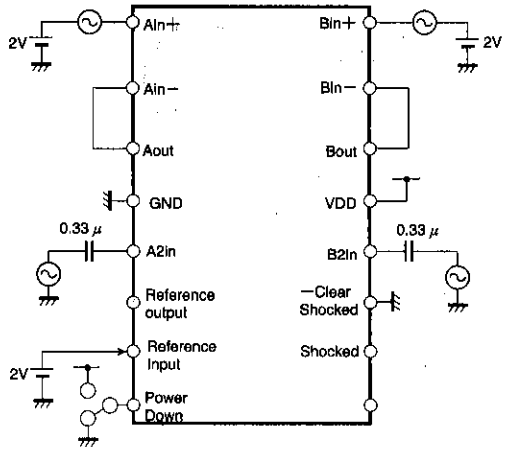


Fig. 1

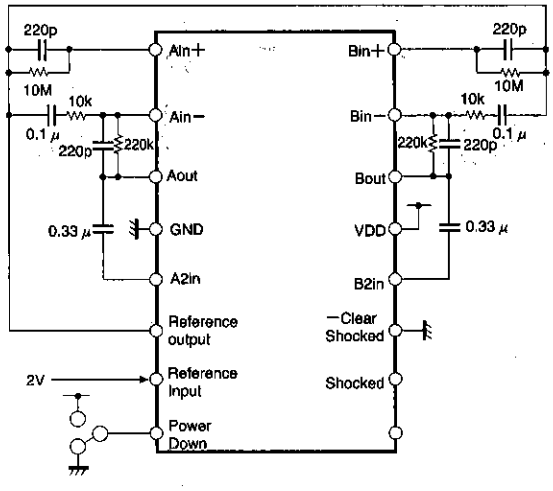
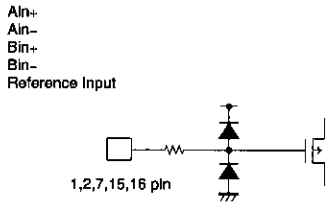
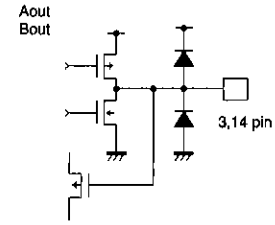
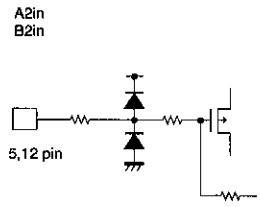


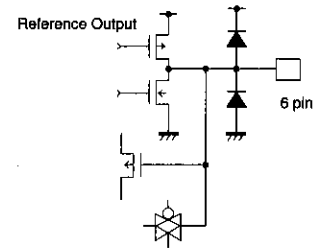
Fig. 2

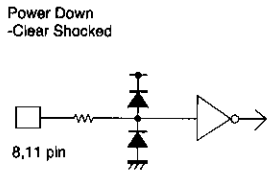
●Input/output circuits

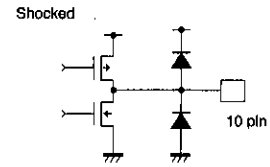












●Circuit operation

Broadly speaking, the BU3892FV comprises 1st and 2nd stage operational amplifiers, which amplify the shock sensor signal; a comparator, which monitors the output level; and a latch circuit, which outputs and retains the shock detection signal.

(1) The 1st stage operational amplifier amplifies the shock sensor signal; gain and frequency characteristic can be set with external components. The 2nd stage operational amplifier also amplifies the shock sensor signal, but its gain is internally fixed at 20dB. The capacitor between the 1st and 2nd stage operational amplifier cuts the DC level to prevent adverse effects on the application device.

(2) The comparator receives the signal from the 2nd stage operational amplifier and compares it to the comparator level, which depends on the DC level input from the reference input pin (the higher the DC level, the lower sensitivity becomes).

(3) Signals detected by the comparator are latched by the latch circuit and output via the SHOCKED pin until reset input is received from the Clear Shocked pin.

●Operation notes

(1) Because the high impedance around the shock sensor makes it susceptible to noise (which can cause malfunctioning), design patterns carefully.

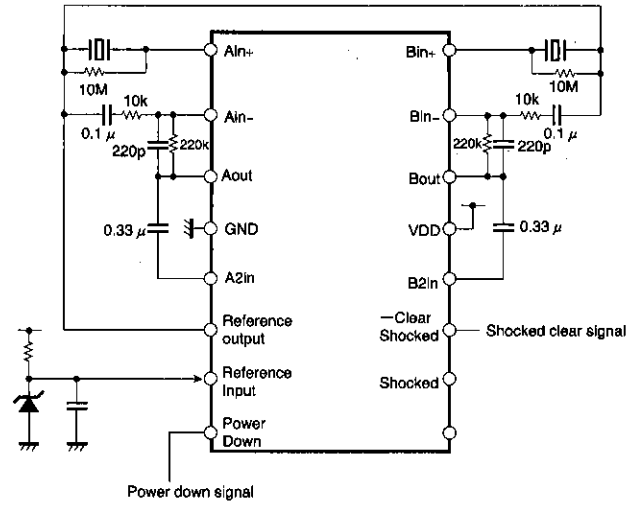
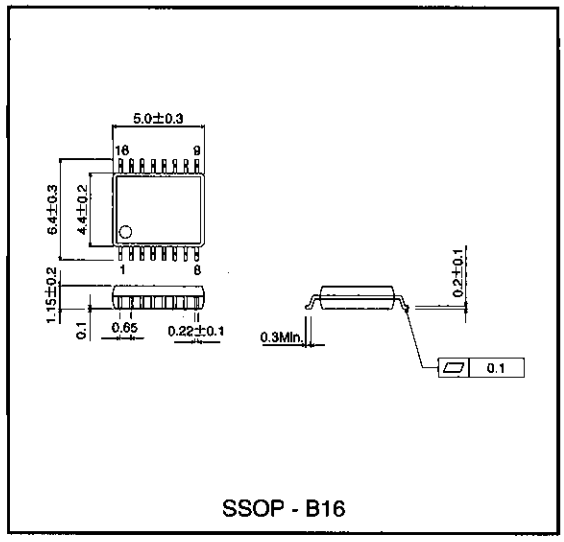


Fig. 3

●External dimensions (Units: mm)



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