

Micro controller servo

BU38905

The BU38905 is a servo controller for VCRs. It has a high-speed, 8-bit CPU and performs the processing required for the drum, capstan, FV and PV completely in software, allowing a large reduction in the number of external components required. It also has a high-performance linear amplifier so an interface IC is not required. Specialized hardware is included for items that require high-speed processing, to allow efficient utilization of the CPU. Timer and tuner functions are also built-in. The VCR control system can be performed by 1 chip.

●Applications

VHS VCRs and camcorders.

●Features

- 1)CPU
 - 499 commands (69 types)
 - Memory-mapped I/O.
 - Minimum command execution time: 250ns (8MHz)
- 2)ROM capacity: 48152×8 bit.
- 3)RAM capacity: 896×8 bit.
- 4)Interrupts
 - Pattern generator: 2
 - Watchdog timer: 1
 - External interrupts: 2
 - FG interrupts: 5
 - Internal interrupts: 10
 - Two timers, one interval timer, two 0.5sec serial, VISS, linear time counter, two PTGs
 - ※ Multi-layer interrupts possible.
- 5)Free-running counter: 19 bit
 - With 8-bit capture for remote control.
- 6)PWM output: 12 bit×2
 - For tuner: 14 bit×1
- 7)Pattern generator
 - 16 bits from FRC MSB used.
 - Output
 - Internal: 4 bit
 - External (PO): 4 bit
 - External (special purpose): 4 bit
- 8)Programmable pre-scaler
 - For CFG: 7 bit
- 9)Head amplifier/chroma rotary
 - Generated from pattern generator output.
- 10) Built-in AGC. Five-bits used to switch the gain control registers for the CTL amplifier.
- 11)CTL counter: 1/30 or 1/25
- 12)Multiplication and division
 - 24 bit×16 bit = 40 bit
 - 16 bit ÷ 16 bit = 16 bit
- 13)Timer: 8 bit×2
- 14)Serial input/output: 8 bit×2
 - SIO2 has automatic transmission buffer.
- 15)VH PULSE
 - VSYNC separated from composite synchronous signal. Pseudo V generated from pattern generator output. Superimposed pseudo H synchronized with the composite synchronous signal.
- 16)VISS/VASS
 - VASS 0/1 discrimination
 - VISS discrimination: every 8 bits
 - Aspect discrimination: done in software
 - D/A CTL switching
- 17)Standard I/O
 - Parallel I/O (PIO): 32 bits
 - Parallel output (PO): 3 bits
 - Tri-state input (PI): 4 bits
 - Tri-state output (PO): 4 bits
- 18)A/D converter: 8 bits×12 channels
 - Automatic scanning.
- 19)Watchdog timer
 - Setting period: 4
- 20)Time counter
 - Interrupt generated every 0.5msec by dividing the 32.7kHz sub-clock.

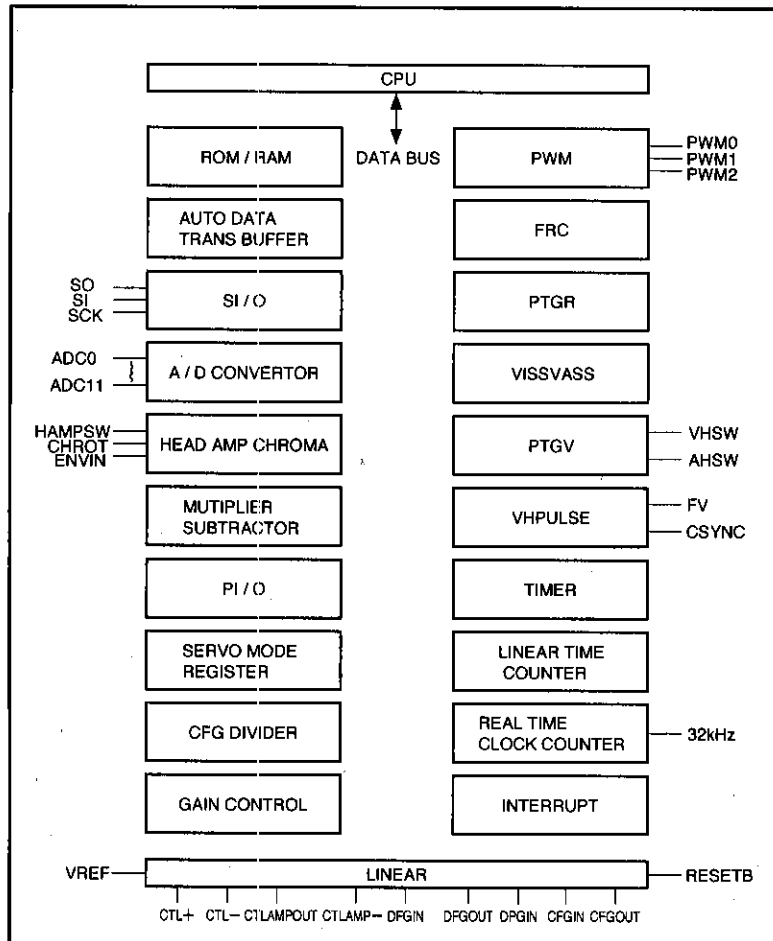
21) Power save

Switch to sub-clock by external interrupt (etc.). Low-power mode.

22) Linear circuits

- DFG : amplifier/comparator
- CFG : amplifier/comparator
- CTL : differential amplifier/comparator
- DPG : comparator

● Block diagram



● Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Applied voltage	V _{DD} , V _{DDA} , V _{DDB}	0.3~7.0*2	V
Input voltage	V _{IN}	V _{SS} -0.3~V _{DD} +0.3	V
Power dissipation	P _d	500*1	mW
Storage temperature	T _{stg}	-55~125	°C

* 1 Reduced by 5mW for each increase in Ta of 1°C over 25°C.

* 2 Use with V_{SS}=V_{SSA}=V_{SSB}, and V_{DD}=V_{DDA}=V_{DDB}.

● Recommended operating conditions

Parameter	Symbol	Limits	Unit
Power supply voltage	V _{DD} , V _{DDA} , V _{DDB}	4.5~5.5	V
Clock frequency	F _{CK}	8	MHz
Operating temperature	T _{opr}	-25~75	°C

●Pin description

Pin No.	Pin name		Function	Pin No.	Pin name		Function	
1	Vss		Logic circuit GND	36	ADC2		A/D converter	
2	PO0*2	PTGVD0	Parallel output and pattern output	37	ADC3			
3	PO1*2	PTGVD1			38	ADC4		
4	PO2*2	PTGRD0			39	ADC5		
5	PO3*2	PTGRD1			40	ADC6		
6	PO4*2	FRC10	Parallel output and FRC output	41	ADC7			
7	PO5*2	PBCTL	Parallel output and PBCTL output	42	V _{DDP}			PWM circuit power supply
8	PO6*2	CS2	Parallel output and serial 2 chip select	43	V _{SSP}		PWM circuit power GND	
9	SO2		Serial I/O2 data I/O	44	RESETB		Reset B	
10	SCK2		Serial I/O2 clock I/O	45	TEST		TEST mode input (normally GND)	
11	SI1		Serial I/O1 data input	46	PWM0		PWM output	
12	SO1*1	PIO28	Serial I/O1 data I/O	47	PWM1			
13	SCK1		Serial I/O1 clock I/O	48	PWM2			
14	AHSW*2	PO7	Parallel output and AHSW output	49	PIO36		Parallel I/O	
15	HAMPSW		Head amplifier switch output	50	PIO37			
16	CHROT		Chroma rotary switch output	51	PIO38			
17	CSYNC		Composite signal logic input	52	PIO39			
18	FV		Pseudo Vsync output	53	PIO8	ENVIN	Parallel I/O and ENVIN input	
19	EXT1	PI4	Parallel input and external interrupt 1	54	PIO9		Parallel I/O	
20	EXT2 (REM)		External interrupt 2	55	PIO10			
21	VHSW		VHSW output	56	PIO11			
22	VDDA		Linear, A/D circuit power supply	57	PIO19			
23	DPGIN		Drum PG (PFG) comparator input	58	PIO20			
24	DFGIN		Drum FG amplifier input	59	PIO16			
25	DFGOUT		Drum FG amplifier output	60	VDD		Logic circuit power supply	
26	CFGOUT		Capstan FG amplifier output	61	PIO17		Parallel I/O	
27	CFGIN		Capstan FG amplifier input	62	PIO18			
28	VREF		Internal bias and power-on reset	63	PIO21			
29	CTLAMP-		CTL amplifier - input	64	PIO22			
30	CTLAMPOUT		CTL amplifier output	65	PIO23			
31	CTL-		CTL coil - connection	66	PIO24			
32	CTL+		CTL coil + connection	67	PIO25			
33	V _{SSA}		Linear, A/D circuit GND	68	PIO26			
34	ADC0		A/D converter	69	PIO27			
35	ADC1				70	PIO29		

Pin No.	Pin name	Function
71	PIO30	Parallel I/O
72	PIO31	
73	PIO32	
74	PIO33	
75	PIO34	
76	PIO35	
77	CLOCKO1	For connection of main oscillator
78	CLOCKI1	
79	CLOCKI2	For connection of sub oscillator
80	CLOCKO2	

* 1 Output signal is xor. Does not become HI-z even if there is PIO Input.

* 2 Output is or.

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●Electrical characteristics (Unless otherwise specified: Ta=25°C, V_{DD}=5V and fosc=8MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
[Logic block]							
Circuit current	I _{DD}	—	10.0	25.0	mA	No load, when reset	Fig.1
<Logic I/O>							
Output "H" voltage	V _H	4.0	4.5	—	V	I=2mA	Fig.3
Output "L" voltage	V _L	—	0.5	1.0	V	I=2mA	Fig.3
Input "H" voltage	V _{IH}	4.0	—	—	V		—
Input "L" voltage	V _{IL}	—	—	1.0	V		—
Input "H" current	I _H	—	0	1.0	μA	V _{in} =V _{DD}	Fig.4
Input "L" current	I _L	-1.0	0	—	μA	V _{in} =0	Fig.4
<Serial I/O>							
Input data hold	T _{SH}	0.16	—	—	μS		—
Input data setup	T _{SS}	0.16	—	—	μS		—
Output data delay	T _D	—	—	0.3	μS	Between clock and data	—
[Linear block]							
Circuit current	I _{LI}	—	12.0	35.0	mA	No load	Fig.5
<DFG>							
Amplifier gain setting range	G _{DFG}	—	—	50	dB		—
Comparator threshold	V _{DFG}	±80	±200	±360	mV _{PP}		Fig.6
<DPG>							
Comparator threshold +	V _{DPG}	+40	+100	+180	mV _{OP}	When positive polarity selected	Fig.7
Comparator threshold -	V _{DPG}	-40	-100	-180	mV _{OP}	When negative polarity selected	Fig.7
<CFG>							
Amplifier gain setting range	G _{CFG}	—	—	50	dB		—
Comparator threshold	V _{CFG}	±55	±135	±250	mV _{PP}		Fig.8
<CTL>							
Comparator threshold	V _{CTL}	±250	±480	±850	mV _{OP}		Fig.10
AGC H threshold	V _{AGCH}	920	1470	2000	mV _{OP}		Fig.10
AGC L threshold	V _{AGCL}	500	930	1480	mV _{OP}		Fig.10
<VREF>							
VREF pin voltage	V _{REF}	2.3	2.5	2.7	V	No load	Fig.9
[A/D block]							
Linearity error	E _L	-3	0	3	LSB		Fig.11
[Power-save mode block]						Stop mode	
Circuit current 1	I _{DD1}	—	10	25	μA	No load, 32kHz oscillation, V _{DD} =3.0V	Fig.2
Circuit current 2	I _{DD2}	—	0	10	μA	No load, 32kHz oscillation stopped	Fig.12

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● Measurement circuit

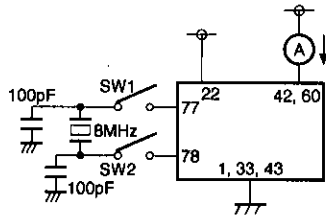


Fig. 1

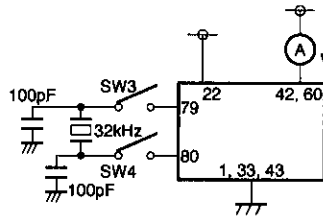


Fig. 2

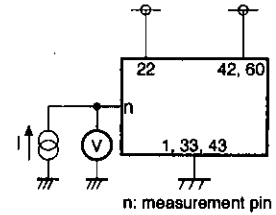


Fig. 3

n: measurement pin

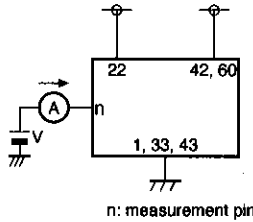


Fig. 4

n: measurement pin

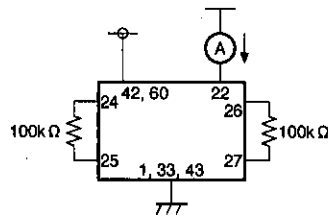


Fig. 5

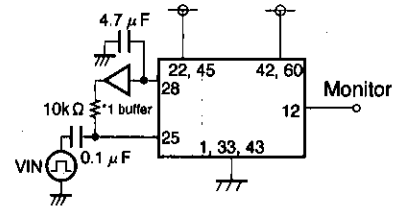


Fig. 6

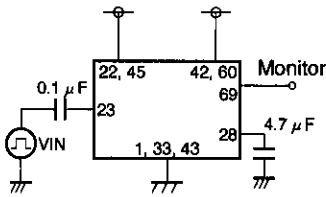


Fig. 7

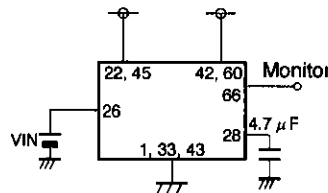


Fig. 8

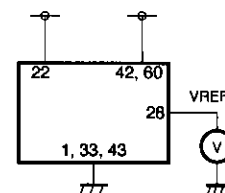


Fig. 9

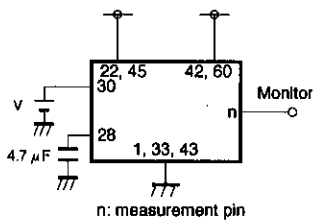


Fig. 10

n: measurement pin

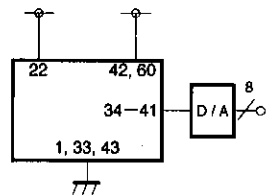


Fig. 11

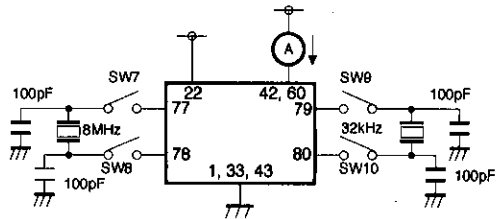


Fig. 12

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●Application example

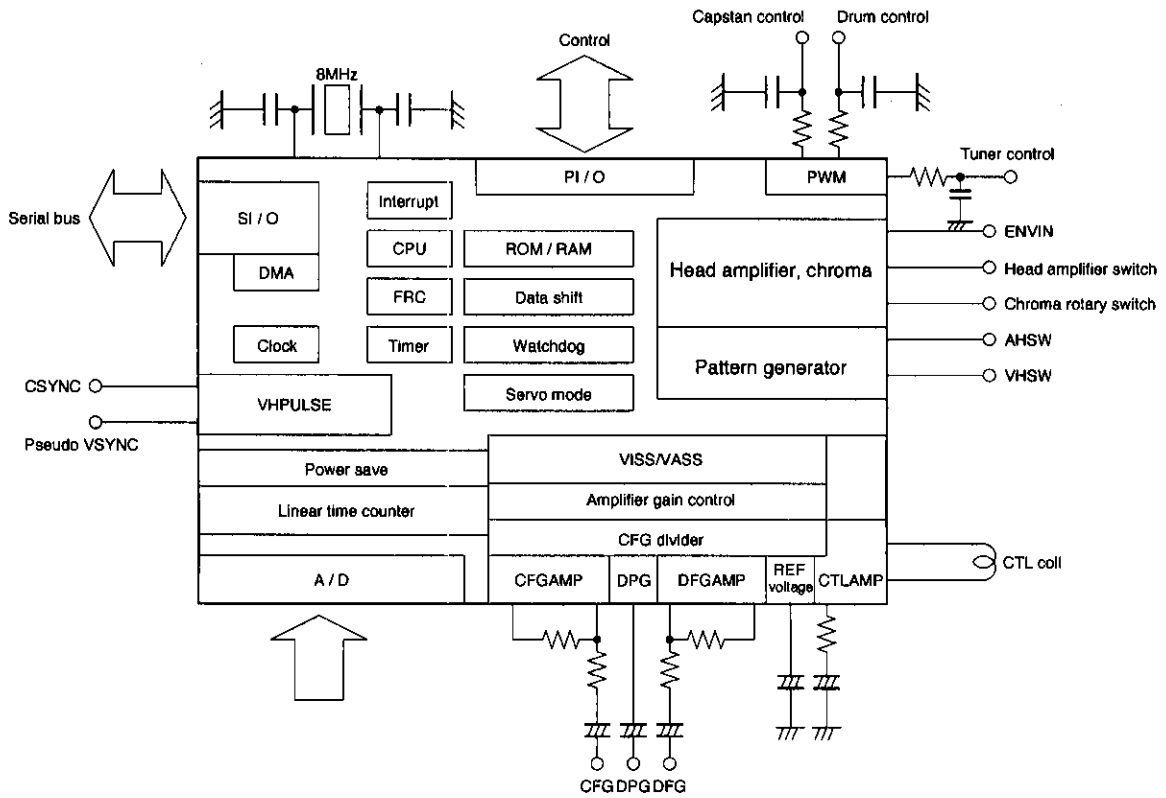


Fig.13

● Electrical characteristic curves

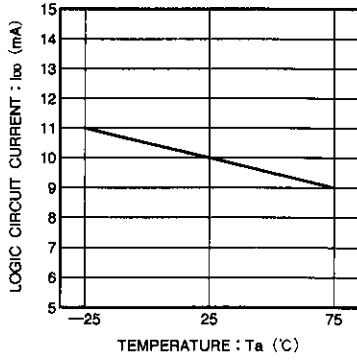


Fig. 14 Logic circuit current vs. temperature.

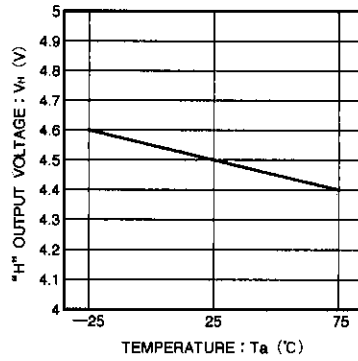


Fig. 15 Logic "H" output voltage vs. temperature.

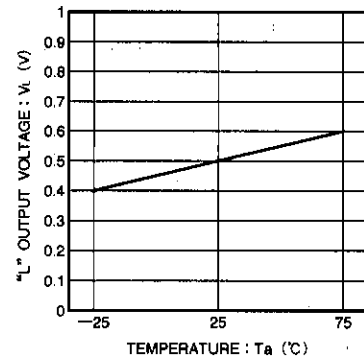


Fig. 16 Logic "L" output voltage vs. temperature.

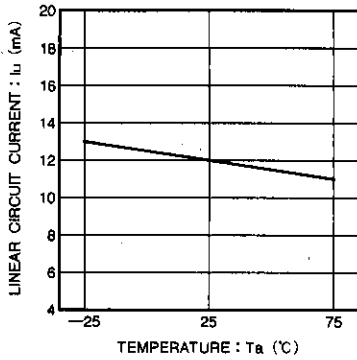
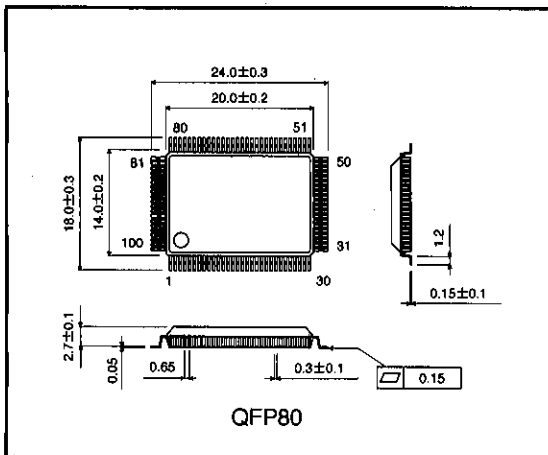


Fig. 17 Linear circuit current vs. temperature.

● External dimensions (Units: mm)



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