NTSC / PAL digital RGB encoder
BU1424K

The BU1424K is an IC that converts digital RGB / YUV input to composite (NTSC / PAL / PAL60), luminance (Y), and chrominance (C) signals, and outputs the results.

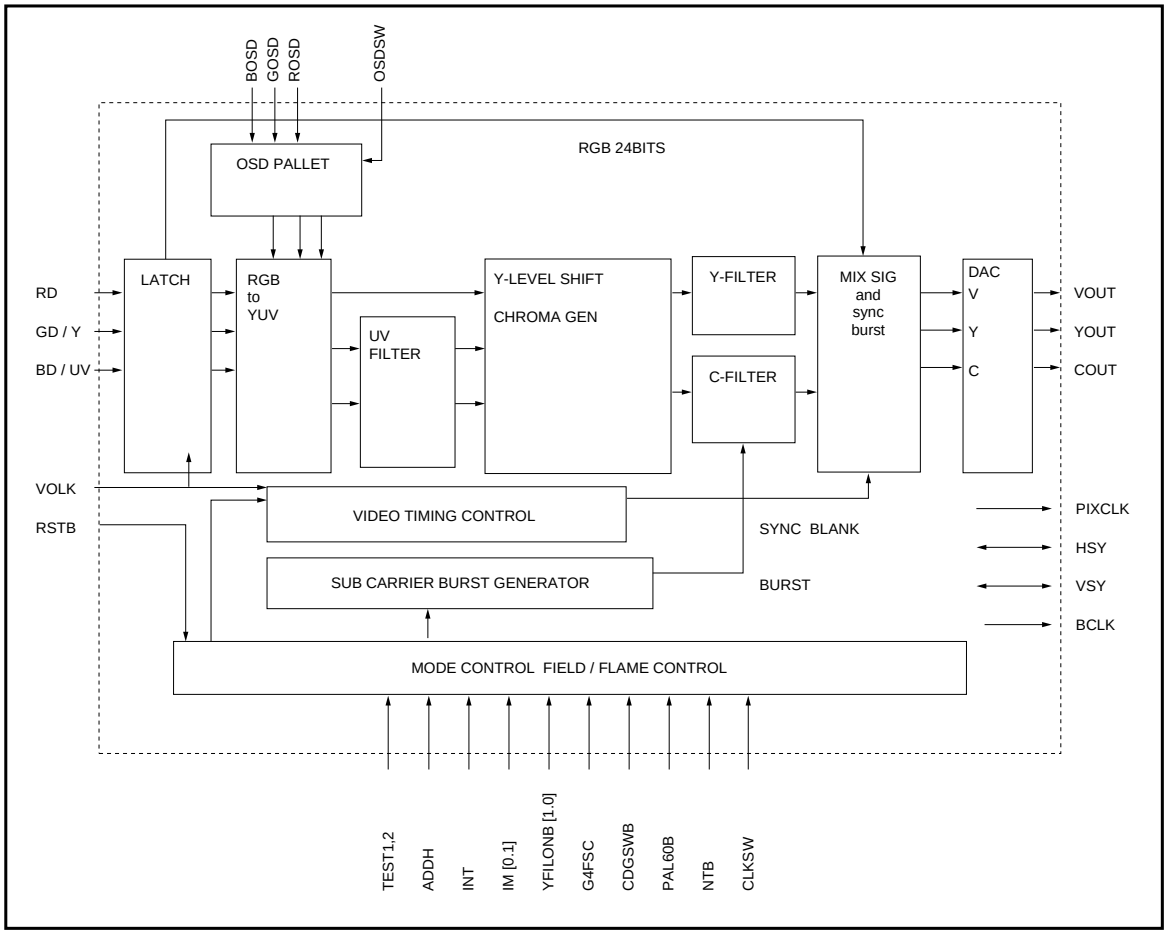
●Applications

Video interfaces for VIDEO-CDs and CD-G decoders

●Features

1) Input clocks supported.
   27.0 / 13.5MHz
   28.636 / 14.318MHz
   28.375 / 14.1875MHz
   35.4695 / 17.73475MHz
2) 24-bit RGB and 16-bit YUV input signals are supported.
3) Both master and slave systems are supported.
4) 9-bit high-speed DAC is used for DAC output of composite VIDEO, Y, and C signals.
5) Internal 8-color OSD output function is provided.
6) FSC-TRAP on the Y channel can be turned on and off.
7) C channel is equipped with an internal chrominance band-pass filter in addition to the U,V. low-pass filter.
8) 5V single power supply, low power consumption. (0.4W typ.)
9) Y and C output can be turned off (the power consumption with Y and C off is 0.25W typ.).

●Block diagram



●Pin descriptions

Pin No.	Pin name	Function		Pin No.	Pin name	Function	
1	BOSD	OSD BLUE DATA INPUT	∗1	33	SLABEB	SELECT MASTER / SLAVE	∗1
2	GD0 / Y0	GREEN DATA Bit0 (LSB)		34	ADDH	+ 0.5 / – 0.5LINE at NON-INTER	∗1
3	GD1 / Y1	GREEN DATA Bit1		35	VREF-C	DAC BIAS	
4	GD2 / Y2	GREEN DATA Bit2		36	CGND	CHROMA OUTPUT GROUND	
5	GD3 / Y3	GREEN DATA Bit3		37	COUT	CHROMA OUTPUT	
6	GD4 / Y4	GREEN DATA Bit4		38	VGND	Composite Output Ground	
7	GD5 / Y5	GREEN DATA Bit5		39	VOUT	COMPOSITE OUTPUT	
8	GD6 / Y6	GREEN DATA Bit6		40	AV_{SS}	Analog Ground (DAC. VREF)	
9	GND	DIGITAL GROUND		41	AV_{DD}	ANALOG (DAC) V_{DD}	
10	GD7 / Y7	GREEN DATA Bit7 (MSB)		42	IR	REFERENCE RESISTOR	
11	BD0 / UV0	BLUE DATA Bit0 (LSB)		43	AV_{DD}	ANALOG (VREF) V_{DD}	
12	BD1 / UV1	BLUE DATA Bit1		44	YGND	Luminance Output Ground	
13	BD2 / UV2	BLUE DATA Bit2		45	YOUT	Luminance Output	
14	BD3 / UV3	BLUE DATA Bit3		46	C4FSC	4FSC / 3.2FSC at PALCD-G	∗1
15	OSDSW	OSD ENABLE / DISABLE	∗1	47	YFILON2B	Y-FILSEL THROU / FILON2	∗2
16	CDGSWB	SELECT Video-CD / CD-G		48	YCOFF	DAC (YOUT. COUT) OFF	∗
17	BD4 / UV4	BLUE DATA Bit4		49	YFILON1B	Y-FILSEL THROU / FILON1	∗2
18	BD5 / UV5	BLUE DATA Bit5		50	PAL60B	NORMAL / PAL60 at PALMODE	∗2
19	BD6 / UV6	BLUE DATA Bit6		51	VCLK	Video Clock Input	
20	BD7 / UV7	BLUE DATA Bit7 (MSB)		52	RSTB	NORMAL / RESET	∗2
21	GND	DIGITAL GROUND		53	CLKSW	SEL × 1CLK / × 2CLK	
22	NTB	SELECT NTSC / PAL MODE		54	RD0	RED DATA Bit0 (LSB)	∗1
23	IM0	SELECT YUV / RGB	∗1	55	RD1	RED DATA Bit1	∗1
24	IM1	SELECT DAC / NORMAL	∗1	56	RD2	RED DATA Bit2	∗1
25	TEST1	Normally pull down to GND	∗1	57	ROSD	OSD RED DATA INPUT	∗1
26	TEST2	SELECT U / V TIMING	∗1	58	RD3	RED DATA Bit3	∗1
27	VSY	V-SYNC INPUT or OUTPUT		59	RD4	RED DATA Bit4	∗1
28	HSY	H-SYNC INPUT or OUTPUT		60	RD5	RED DATA Bit5	∗1
29	PIXCLK	1 / 2freq. of BCLK		61	V_{DD}	DIGITAL V_{DD}	
30	BCLK	INTERNAL CLOCK OUTPUT		62	RD6	RED DATA Bit6	∗1
31	V_{DD}	DIGITAL V_{DD}		63	RD7	RED DATA Bit7	∗1
32	INT	Interlace / Non-Interlace		64	GOSD	OSD GREEN DATA INPUT	∗1

∗1 Internal pull-down resistor
∗2 Internal pull-up resistor

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Applied voltage	V_{DD}, AV_{DD}	– 0.5 ~ + 7.0	V
Input voltage	V_{IN}	– 0.5 ~ V_{DD} + 0.5	V
Storage temperature	Tstg	– 55 ~ + 150	°C
Power dissipation	Pd	1350*1	mW

*1 Reduced by 11mW for each increase in Ta of 1°C over 25°C.
When mounted on a 120mm × 140mm × 1.0mm glass epoxy board.
* Operation is not guaranteed at this value.
○ Not designed for radiation resistance.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD} = AV_{DD}*	+ 4.75 ~ + 5.25	V
Input high level voltage	V_{IH}	+ 2.1 ~ V_{DD}	V
Input low level voltage	V_{IL}	0 ~ + 0.8	V
Analog input voltage	V_{AIN}	0 ~ AV_{DD}	V
Operating temperature	Topr	– 25 ~ + 60	°C

* Should be used at V_{DD} = AV_{DD}.

●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = AV_{DD} = 5.0V, GND = AV_{SS} = VGND = CGND = YGND)

Digital block

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Burst frequency 1	fBST1	—	3.57954	—	MHz	—
Burst frequency 2	fBST2	—	4.43361	—	MHz	—
Burst cycle	CBST	—	9	—	CYC	—
Operating circuit current 1	Idd1	—	80	—	mA	27MHz color bar
Operating circuit current 2	Idd2	—	40	—	mA	27MHz color bar PD mode
Output high level voltage	V_{OH}	4.0	4.5	—	V	I_{OH} = – 2.0mA
Output low level voltage	V_{OL}	—	0.5	1.0	V	I_{OH} = 2.0mA
Input high level voltage	V_{IH}	2.1	—	—	V	—
Input low level voltage	V_{IL}	—	—	0.8	V	—
Input high level current	I_{IH}	– 10	0.0	10.0	µA	—
Input low level current	I_{IL}	– 10	0.0	10.0	µA	—

DAC block

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
DAC resolution	RES	—	9	—	BITS	—
Linearity error	EL	—	± 0.5	± 3.0	LSB	IR = 1.2kΩ
Y white level current	IYW	—	25.14	—	mA	—
Y black level current	IYB	—	7.24	—	mA	—
Y zero level current	IYZ	– 10	0.0	10.0	µA	—
V white level current	IYW	—	25.14	—	mA	—
V black level current	IYB	—	7.24	—	mA	—
V zero level current	IYZ	– 10	0.0	10.0	µA	—

●Application example

(1) Example in Master mode: Doubled clock is input and 24-bit RGB input is used

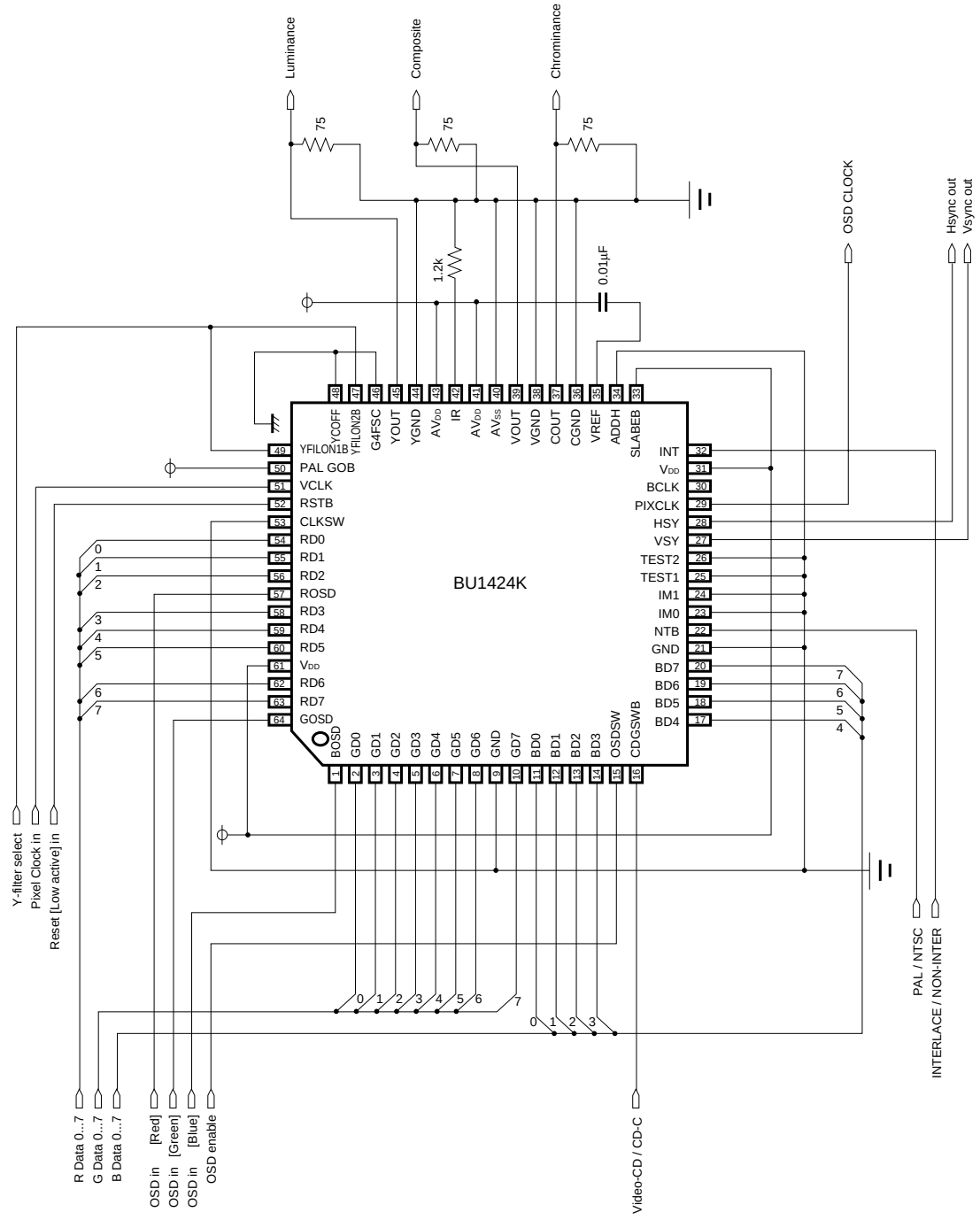


Fig.1

(2) Example in Slave mode: Doubled clock is input and 16-bit YUV input is used

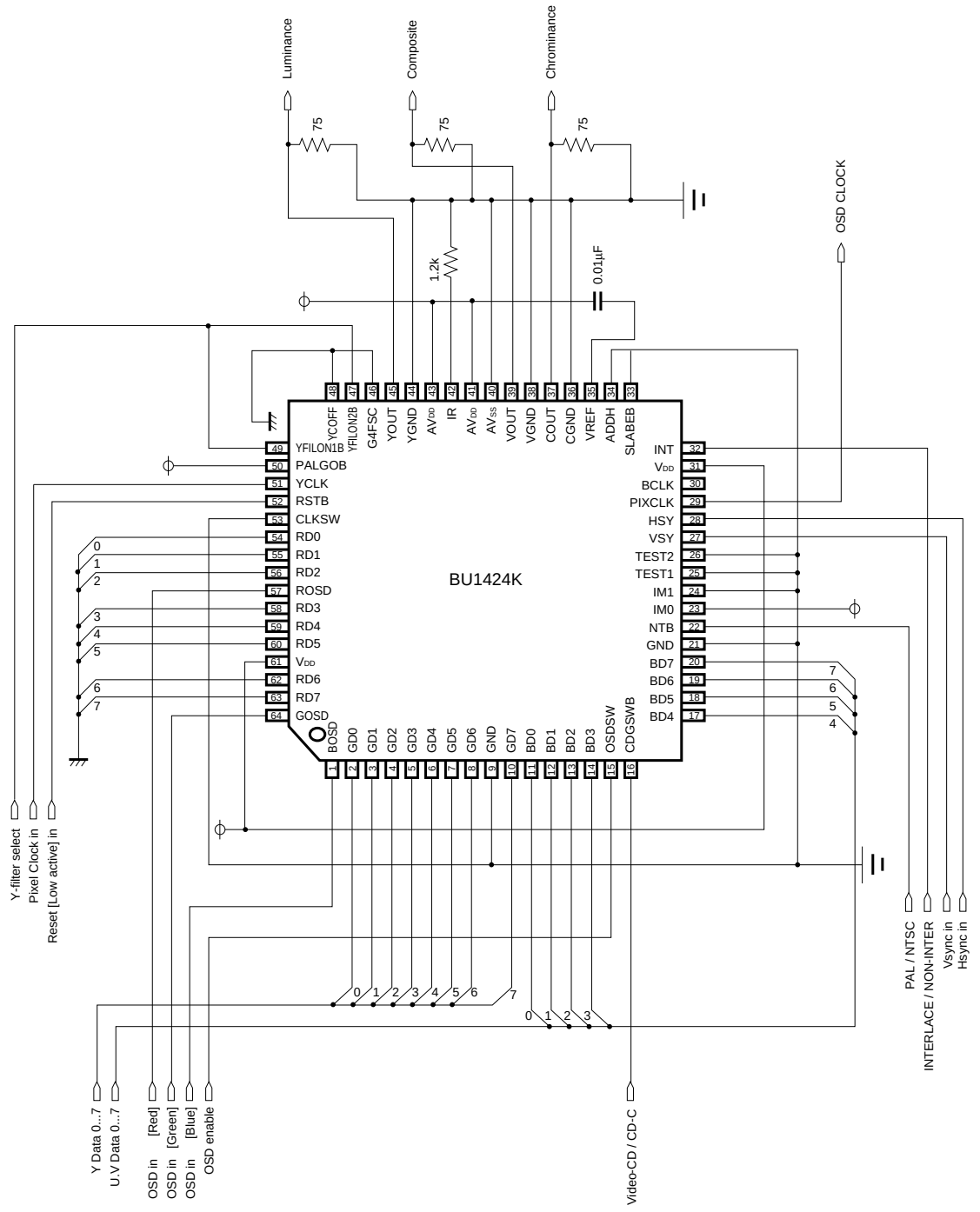
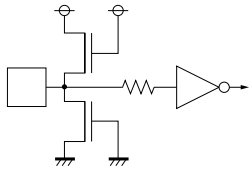
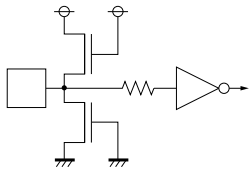
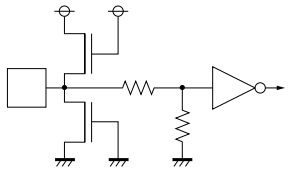
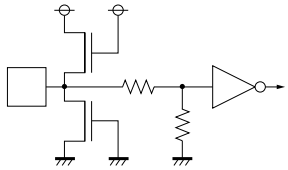
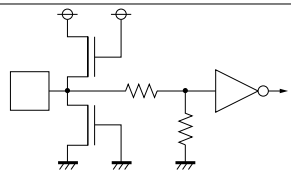
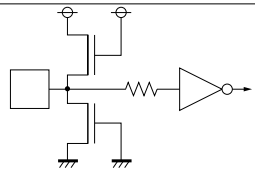
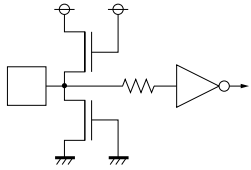
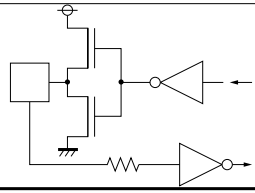
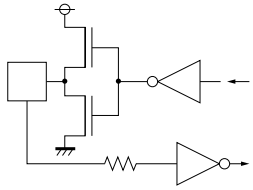
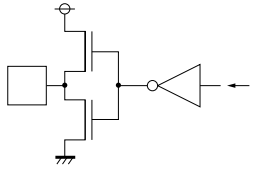
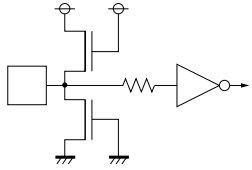
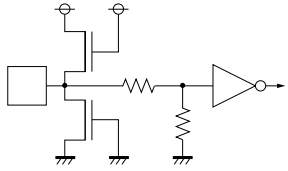
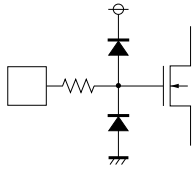
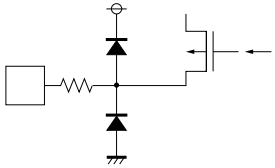
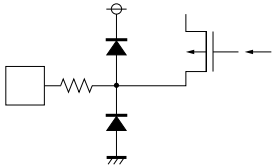
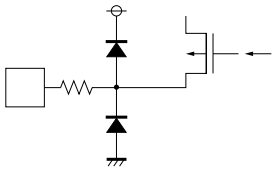
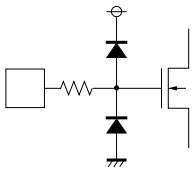
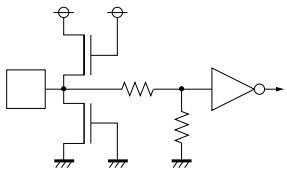
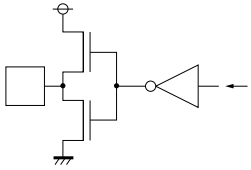


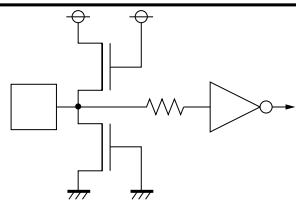
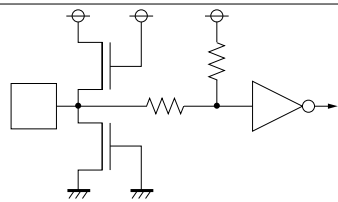
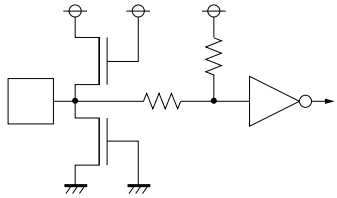
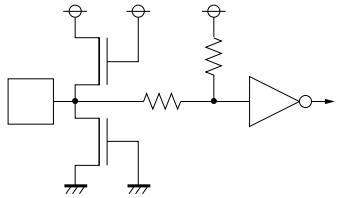
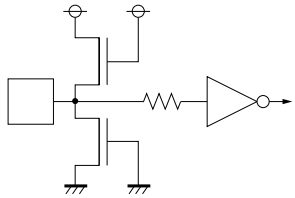
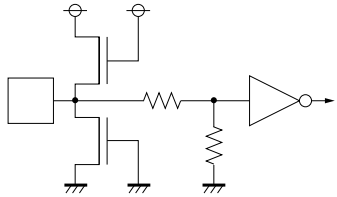
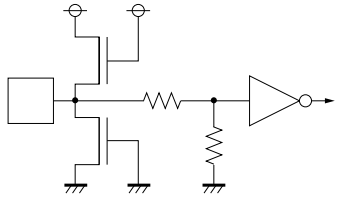
Fig.2

●Equivalent circuits

Pin No.	Pin name	I / O	Equivalent circuit	Function
2 ~ 8 10	GD (7: 0)	I		G data input pin for 24-bit RGB input. Y data input pin for 16-bit YUV input.
11 ~ 14 17 ~ 20	BD (7: 0)	I		B data input pin for 24-bit RGB input. U, V data input pins for 16-bit YUV input.
54 ~ 56 58 ~ 60 62.63	RD (7: 0)	I		R data input pin for 24-bit RGB input.
1 57 64 15	ROSD GOSD BOSD OSDSW	I		OSD data input pin when using the OSD function. When the OSDSW pin is HIGH, input to the ROSD, GOSD, and BOSD pins takes precedence over RGB, and the data is converted.
23 24	IM0 IM1	I		Control pins used to select RGB (24-bit), YUV (16-bit) or DAC Through as the input mode.
16	CDGSWB	I		Switches the mode between Video-CD (HIGH) and CD-G (LOW).
22	NTB	I		Switches the mode between NTSC (LOW) and PAL (HIGH).
28	HSY	I / O		This is the horizontal synchronization signal pin. Negative polarity HSYNC signals are input (when SLABEB = LOW) or output (when SLABEB = HIGH) here. This is also used as the synchronization signal for fixing the PIXCLK output phase.

Pin No.	Pin name	I / O	Equivalent circuit	Function
27	VSY	I		Vertical synchronization signals (VSYNC) are input (when SLABEB = LOW) or output (when SLABEB = HIGH) here.
29	PIXCLK	O		The internal processing clock is divided in half and then output. Data is read at the point at which the edge of this clock changes. This can also be used as the clock for the OSD IC.
32	INT	I		This pin switches between interlace (when HIGH) and non-interlace (when LOW) modes. This pin is effective in both the VIDEO-CD and CD-G modes.
33 34	SLABEB ADDH	I I		This pin switches between the Master (when HIGH) and Slave (when LOW) modes. It is effective in the non-interlace mode, and it switches between – 0.5 lines (when LOW) and + 0.5 lines (when HIGH) for the number of lines in an interlace field.
35	Vref-C	I		This is the reference voltage generator circuit monitoring pin which determines the output amplitude (output current for 1 LSB) of the DAC.

Pin No.	Pin name	I / O	Equivalent circuit	Function
37	COUT	O		This is the chrominance output pin for the S pin.
39	VOUT	O		Composite output pin.
45	YOUT	O		Luminance output pin for the S pin.
42	IR	I		The output amplitude (output current for 1 LSB) of the DAC is specified using an external resistor, and this pin controls the value of the current flowing per bit.
48	YCOFF	I		When there is HIGH input at the signal input pin, which switches to and from the low power consumption mode, this turns off the output from the YOUT and COUT pins.
30	BCLK	O		Output for the internal clock. When CLKSW is HIGH, the VCLK buffer output. When CLKSW is LOW, the VCLK 1 / 2 cycle output.

Pin No.	Pin name	I / O	Equivalent circuit	Function
51	VCLK	I		Input pin for the reference clock in the Video-CD mode.
52	RSTB	I		Reset input pin which initializes the system.
49	YFILON1B YFILON2B	I		Selects the F characteristic of the Y-FILTER. However, this is only effective when OSDSW is LOW.
50	PAL60B	I		Switches between the PAL and PAL60 modes. This is effective only when the NTB pin is HIGH. (PAL mode only).
53	CLKSW	I		This switches between dividing the VCLK input in half and using it as an internal clock (when LOW), and using it as an internal clock without dividing it in half (when HIGH).
46	G4FSC	I		Switching pin for CDG mode input frequency 14.1875 / 4fsc.
25 26	TEST1 TEST2	I		Normally, this is connected to the GND pin. However, when 16-bit YUV input is used, the TEST2 pin can be used as the U and V timing control pins.

Pin No.	Pin name	I / O	Equivalent circuit	Function
31 61 41 43	V_{DD} AV_{DD}	—	—	Power supply pin for the digital, the analog and blocks.
9 21 36 38 40 44	GND CGND VGND AV_{SS} YGND	—	—	Ground for digital and analog blocks.

●Circuit operation

(1) Overview

The BU1424K converts digital images and video data with an 8-bit configuration to 9-bit composite signals (VOUT), luminance signals (YOUT), and chrominance signals (COUT) for the NTSC, PAL, and PAL60 formats, and outputs the converted data as analog TV signals.

The user may select whether VOUT consists of chrominance signals that have passed through a chrominance band pass and luminance signals that have been mixed, or luminance signals that have passed through a chrominance trap and luminance signals that have not passed through a chrominance trap. The F characteristic of this chrominance trap may be selected from among three available types. Since YOUT normally does not pass through the trap, it is optimum for the S pin. COUT normally passes through the chrominance band pass, and is thus highly resistance to dot interference. In addition, when used in the doubled clock mode, it passes through an interpolator filter, and for that reason is able to reproduce even cleaner image quality.

A correspondence can be set up between input digital image data and Video-CD and CD-G decoder output. Output TV signals, in addition to switching among the NTSC, PAL, and PAL60 modes, can be switched between the interlace and non-interlace modes.

The data clock input to the VCLK pin can also be input as a doubled clock for the data rate (in doubled clock modes). In doubled clock modes, data is read and processed at the rising edge of an internal clock that has been divided in half. In ordinary clock modes, data is read and processed at the rising edge of the clock that has the same phase as the input clock. Two input data formats are supported: 24-bit RGB (4: 4: 4) and 16-bit YUV (4: 2: 2). These are input to RD0 to 7, GD0 to 7, and BD0 to 7, respectively. The selected input format can be switched using the IM0 and IM1 pin input. When the OSDSW pin is set to the "Enabled" (H) state, data input to the ROSD, GOSD, and BOSD pins becomes effective, making it possible to input 7-color (8 including black) chrominance data. At the same time, a clock with a frequency half that of the internal clock is output from the PIXCLK pin. As a result, the PIXCLK pin can easily be directly connected to the OSD IC clock input pin, and the OSDSW pin can be directly connected to the BLK output pin. Thus, the BU1424K and the OSD IC can be synchronized, and OSD text with a burster trimmer stacker feature can be used.

If the input data is in the RGB format, it is converted to YUV. If it is in the YUV format, it is converted from the CCIR-601 format to level-shifted YUV data. The YUV data is then adjusted to the 100IRE level in the NTSC, PAL, and PAL60 modes, and U and V data is phase-adjusted by a sub-carrier generated internally, and is modulated to chrominance signals.

Ultimately, elements such as the necessary synchronization level, the color blanking level, and burst signals are mixed, and pass through the 9-bit DAC to be output as NTSC or PAL composite signals, luminance signals, and chrominance signals (conforming to RS-170A). At this point, the DAC is operating at twice the internal clock, making it possible to reduce the number of attachments.

Furthermore, luminance signal output and chrominance signal output can be turned off. At this point, it is possible to reduce the level of power consumption.

The DAC output is current output. If a resistor of a specified value is connected to the IR pin, $2.0V_{P-P}$ output can be obtained by connecting 75Ω to the VOUT pin as an external resistor. As a result, normally, when a video input pin (75Ω terminus) is connected, the output is approximately $1.0V_{P-P}$ voltage output at a white 100% level.

(2) Specifying the mode

1) Power saving mode

With the BU1424K, setting the YCOFF pin to HIGH turns off the output from the YOUT and COUT pins of the DAC output, enabling use in the low power consumption mode.

Table 1: Low power consumption mode with the YCOFF pin

Pin No.	Pin name	Output mode and power consumption			
	YCOFF	VOUT pin	YOUT pin	COUT pin	Power consumption (Typ.)
48	LOW	Composite signal	Luminance signal	Chrominance signal	0.45W
	HIGH	Composite signal	No output (0V)	No output (0V)	0.25W

2) Output modes

The "Video-CD" and "CD-G" modes can be supported by both digital image and video data, with the mode being switched by the CDGSWB pin input. When the CDGSWB pin input is LOW, the CD-G mode is set, and when HIGH, the Video-CD mode is set. Also, the "NTSC", "PAL", and "PAL60" modes may be selected as the output TV modes. The output TV mode is switched using the NTB and PAL60 pin input. Setting the NTB pin input to LOW sets the NTSC mode, and setting it HIGH with the PAL60 pin also HIGH sets the PAL mode. Setting the NTB pin HIGH and the PAL60 pin LOW, sets the PAL60 mode.

Table 2: Specifying modes

NTB	PAL60	GDGSWB	Decoder mode	TV mode
0	*	0	CD-G	NTSC
0	*	1	Video-CD	NTSC
1	0	0	CD-G	PAL60
1	0	1	Video-CD	PAL60
1	1	0	CD-G	PAL
1	1	1	Video-CD	PAL

Also, INT pin input can be used to switch between "interlace output" and "non-interlace output."

Setting the input to LOW enables non-interlace output, and setting it to HIGH enables interlace output. When non-interlace output is used, the number of lines in one field can be controlled using the ADDH pin. If the ADDH pin is LOW, the number of lines in one field is set to the number of interlace output lines minus 0.5 lines, and when HIGH, the number of lines in one field is set to the number of interlace output lines plus 0.5 lines.

Table 3: Pin settings for interlace / non-interlace modes

INT	ADDH	Scan Mode	No. of Lines / Field	
			NTSC / PAL60	PAL
0	0	Non-interlace	262	312
0	1	Non-interlace	263	313
1	*	Interlace	262.5	312.5

3) Input formats

The digital data input format can be set as shown in the table below, using the IM1 and IM0 pins. Both 24-bit RGB (4: 4: 4) and 16-bit YUV (4: 2: 2) are supported. In addition, digital RGB input can be output as analog RGB output (RGB Through mode).

Table 4: Input format settings

IM1	IM0	Input format	Output signal
0	0	R (8 bits), G (8 bits), B (8 bits)	TV signals (9-bit resolution)
0	1	YUV16bit (4: 2: 2)	TV signals (9-bit resolution)
1	0	—	—
1	1	ROSD, GOSD, BOSD expanded to RGB input	RGB analog signals (9 bits)

Table 5: Bit assignments in RGB Through mode

Output Pin	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
YOUT (45)	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	ROSD
VOUT (39)	GD7	GD6	GD5	GD4	GD3	GD2	GD1	GD0	GOSD
COUT (37)	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	BOSD

The BU1424K has an internal OSD switch and chrominance data generating function. Consequently, joint usage of an OSD-IC with blanking and R, G, and B output can be easily supported by the OSD. Moreover, a clock with half the internal processing frequency of the BU1424K is output from the PIXCLK pin, and can be connected to the OSD-IC clock input, enabling the timing to be captured.

ROSD, GOSD, and BOSD pin input is effective as long as the OSDSW pin input is HIGH. The relationship between OSD data and chrominance data is as shown in Table 6 below.

Table 6: Correspondence between OSD function, input data and chrominance output

OSDSW	ROSD	GOSD	BOSD	Output chrominance signal
1	0	0	0	Black (blanking)
1	0	0	1	Blue
1	0	1	0	Green
1	0	1	1	Cyan
1	1	0	0	Red
1	1	0	1	Magenta
1	1	1	0	Yellow
1	1	1	1	White
0	*	*	*	Based on input specified by IM0 and IM1

4) Clock modes

With the BU1424K, clock input is available at the VCLK pin.

Clocks supplied from an external source should basically be input at a frequency double that of clocks used internally (basic clock: BCLK) (when the CLKSW pin is LOW). The phase relationship between the internal clock and the external clock at this time is as shown in Fig. 3, with the HSY pin input serving as a reference. In the Master mode, in which data from the HSY pin is output and used, HSY is output at the timing shown in Fig. 3. With the BU1424K, data (RD, GD, BD, etc.) is read at the rising edge of the internal clock (BCLK), so data should be input to the BU1424K as shown in Fig. 3.

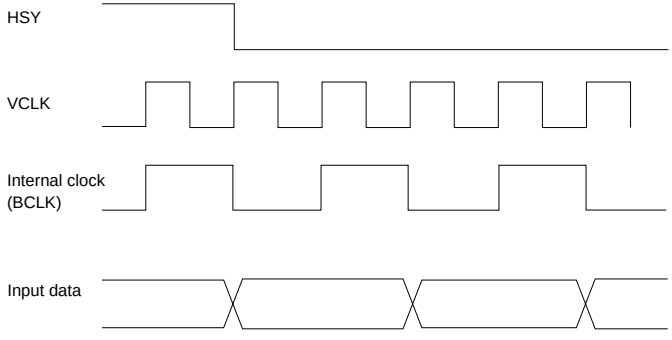


Fig.3 Illustration of clock timing (CLKSW is LOW)

Also, setting the CLKSW pin to HIGH enables the frequency of the external clock to be used as BCLK, the internal clock, just as it is. Since the data is read to the BU1424K at the rising edge of BCLK at this time as well, data should be input as shown in Fig. 4. The relationship with HSY is also as shown in Fig. 4.

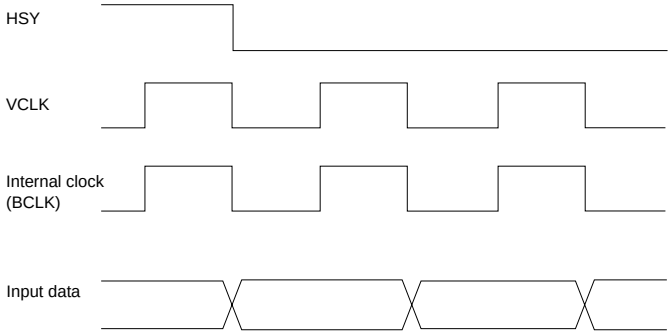


Fig.4 Illustration of clock timing (CLKSW is HIGH)

With the BU1424K, the sub-carrier (burst) frequency is generated using the internal clock. For this reason, the frequencies used in the various modes are limited, so those frequencies should be input (see Table 7 below).

Table 7: BU1424K clock input frequency settings

CLKSW pin	G4FSC pin	Video-CD mode	CD-G mode	
		Same for NTSC / PAL / PAL60	NTSC	PAL / PAL60
0	0	27.000MHz	28.636MHz	28.3750MHz
0	1	27.000MHz	28.636MHz	35.4695MHz
1	0	13.500MHz	14.318MHz	14.1875MHz
1	1	13.500MHz	14.318MHz	17.73475MHz

5) Synchronization signals

The BU1424K has an "Encoder Master" mode in which synchronization signals are output, and an "Encoder Slave" mode in which synchronization signals are input from an external source and used to achieve synchronization. These modes are switched at the SLABEB pin. When the SLABEB pin is LOW, the Slave mode is in effect, and when HIGH, the Master mode is in effect.

In the Master mode, the HSY and VSY pins serve as output, with horizontal synchronization signals (HSYNC) being output from the HSY pin and vertical synchronization signals (VSYNC) from the VSY pin. At this time, the reference timing for synchronization signal output is determined at the rising edge of the RSTB pin. Output is obtained in accordance with the specified mode (NTSC, PAL, or PAL60, interlace or non-interlace). Output in the non-interlace mode, however, is output only under "Odd" field conditions (the falling edges of HSY and VSY are the same).

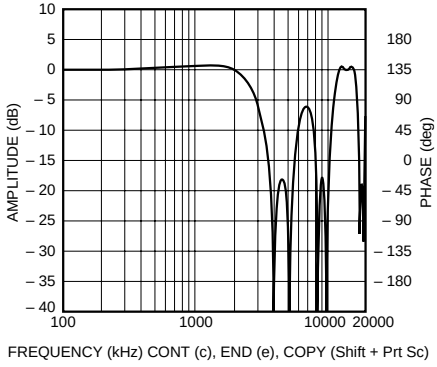
In the Slave mode, the HSY and VSY pins serve as input, and horizontal synchronization signals (HSYNC) should be input to the HSY pin and vertical synchronization signals (VSYNC) to the VSY pin. The input synchronization signals at this time should be input in accordance with the specified mode. With the BU1424K, field distinction between odd and even fields is made automatically for each field when interlace input is used. With the BU1424K, all synchronization signals are treated as negative polarity signals (signals for which the sync interval goes LOW). When using the non-interlace mode, operation is normally carried out under odd field conditions (the falling edges of HSY and VSY are simultaneous).

6) Y filter

With the BU1424K, the frequency characteristic of Y, which is mixed with the VOUT pin output, is set so that it can be selected using the YFILON1 and 2 pins. A through filter is normally used on the YOUT pin output, so that it is not limited to this method.

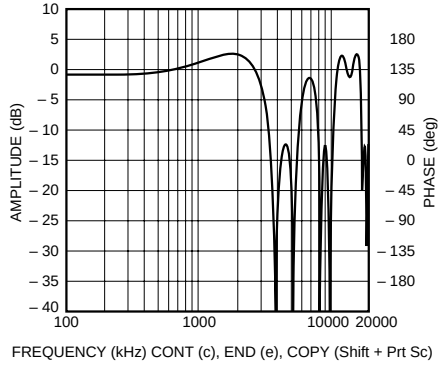
Table 8: Frequency characteristic of the Y channel

YFILON2B	YFILON1B	Frequency characteristic of the Y channel
H	H	TRAP filter through (same signal as YOUT pin output is mixed with VOUT)
L	H	chart1
H	L	chart2
L	L	chart3



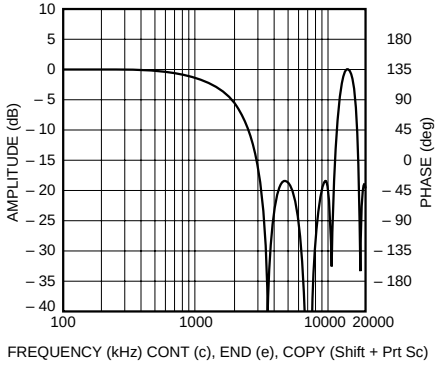
Gain-Phase Graphic

Fig.5 Chart1 (BCLK = 13.5MHz)



Gain-Phase Graphic

Fig.6 Chart2 (BCLK = 13.5MHz)



Gain-Phase Graphic

Fig.7 Chart3 (BCLK = 14.318MHz)

(3) Output level

Figures 8 to 10 indicate the digital data values for the DAC output when the color bars from the various pins are reproduced.

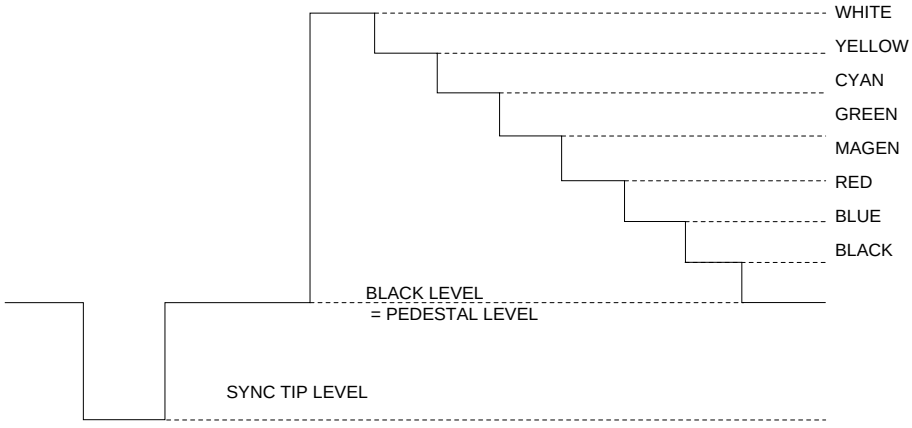


Fig.8 YOUT output

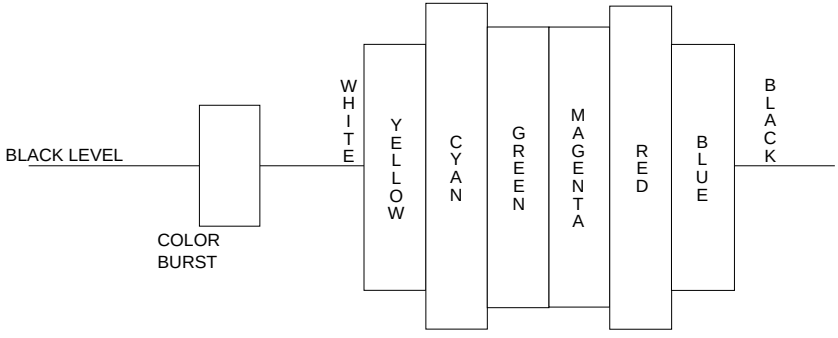


Fig.9 COUT output

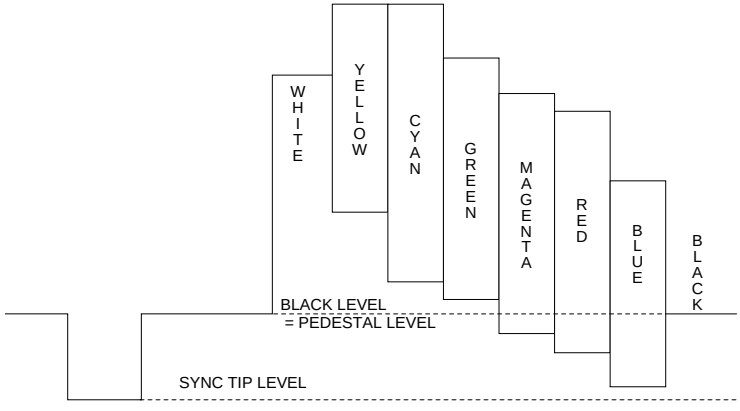


Fig.10 VOUT output

Table 9: BU1424K color bar input / output data

Input (8-bit hexadecimal for each)						Output (9-bit hexadecimal for each)			
RGB24bit			YUV (4: 2: 2)			NAME&COLOR	YOUT	COUT	VOUT
RD	GD	BD	YD	UD	VD				
—	—	—	—	—	—	SYNC TIP	000	—	000
—	—	—	—	—	—	Color Burst NTSC	—	± 039	± 039
—	—	—	—	—	—	Color Burst PAL	—	± 03D	± 03D
—	—	—	—	—	—	BLANK LEVEL	—	100	—
00	00	00	10	80	80	BLACK (Pedestal)	072	000	072
00	00	FF	28	F1	6D	BLUE	092	± 064	± 064
00	FF	00	90	36	22	GREEN	117	± 085	± 085
00	FF	FF	A9	A5	10	CYAN	138	± 08E	± 08E
FF	00	00	51	5A	F0	RED	0C6	± 08E	± 08E
FF	00	FF	6A	C9	DD	MAGENTA	0E6	± 085	± 085
FF	FF	00	D2	0E	92	YELLOW	16C	± 064	± 064
FF	FF	FF	EB	80	80	WHITE	18C	000	000

∗ COUT and VOUT display the chrominance amplitude. COUT is 100H ± XXXH.
VOUT is YOUT ± XXXH.

(4) Timing

Table 10 below shows the input and output pins related to timing.

Table 10: BU1424K timing-related input / output pins

Pin No.	Pin name	I / O	Function
52	RSTB	I	System reset input pin
51	VCLK	I	Clock input pin
53	CLKSW	I	Clock input mode setting pin
27	VSY	I / O	Vertical synchronization signal I / O pin
28	HSY	I / O	Horizontal synchronization signal I / O pin
16	CDGSWB	I	Video-CD / CD-G mode switching pin
22	NTB	I	NTSC / PAL mode switching pin
50	PAL60B	I	PAL / PAL60 mode switching pin
32	INT	I	Interlace / Non-interlace mode switching pin
33	SLABEB	I	Master / Slave mode switching pin
34	ADDH	I	Pin which adds 1 line in non-interlace mode
29	PIXCLK	O	1 / 2 divider output for internal clock (OSD clock)

1) Input clocks and input data timings in the various operation modes

There are slight differences in the input data and the clock timing, depending on which mode is being used. What is shared by all modes is that, with the BU1424K, data is read and discharged at the rising edge of the internal clock. The illustration below shows the input conditions in the various modes.

1. Master mode, ∗ clock mode
Encoder master (pin 33 = H)
Internal clock = input clock (pin 53 = H)

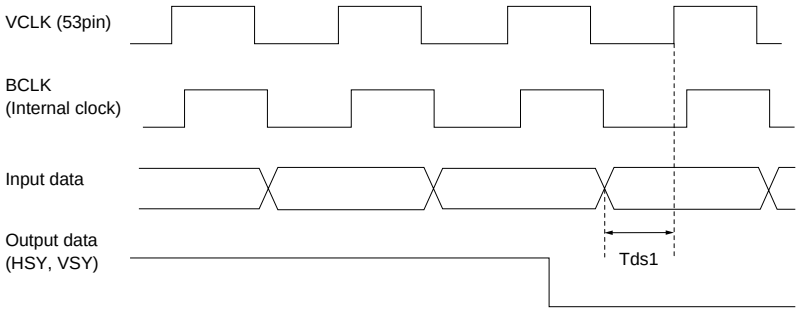


Fig.11

∗ In this mode, the internal clock (BCLK) begins to operate at the same phase as the VCLK input, following the rise of the RSTB pin (pin 52).

Table 11

Parameter	Symbol	Min.	Typ.	Max.
Data setup time 1	Tds1	10	—	—

2. Master mode, doubled clock mode
Encoder master (pin 33 = H)
Internal clock = 2 ∗ input clock (pin 53 = H)

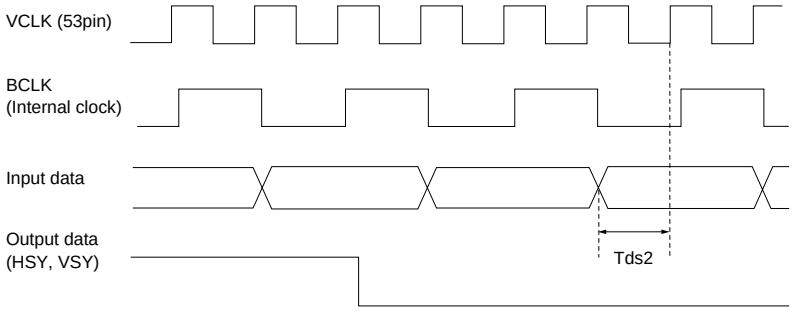


Fig.12

∗ In this mode, the internal clock (BCLK) begins to operate at a halved frequency at the rise of the VCLK input, following the rise of the RSTB pin (pin 52).

Table 12

Parameter	Symbol	Min.	Typ.	Max.
Data setup time 2	Tds2	10	—	—

3. Slave mode, single clock mode
Encoder slave (pin 33 = L)
Internal clock = input clock (pin 53 = L)

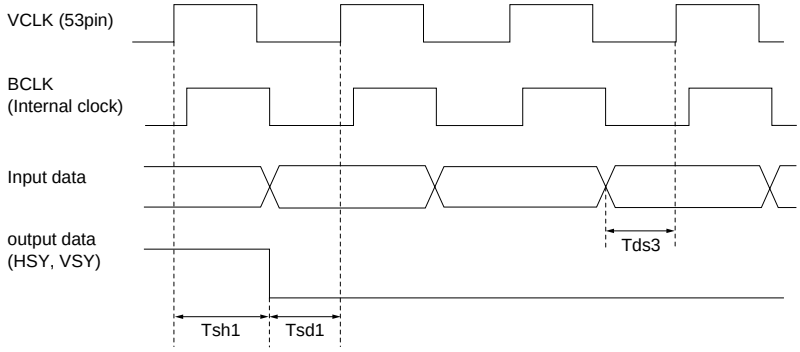


Fig.13

∗ In this mode, the internal clock (BCLK) begins to operate at the same phase as the VCLK input, following the rise of the RSTB pin (pin 52).

Table 13

Parameter	Symbol	Min.	Typ.	Max.
Data setup time 3	Tds3	10	—	—
Sync signal hold time	Tsh1	10	—	—
Sync signal hold time	Tsd1	10	—	—

4. Slave mode, doubled clock mode
Encoder slave (pin 33 = L)
Internal clock = 2 ∗ input clock (pin 53 = L)

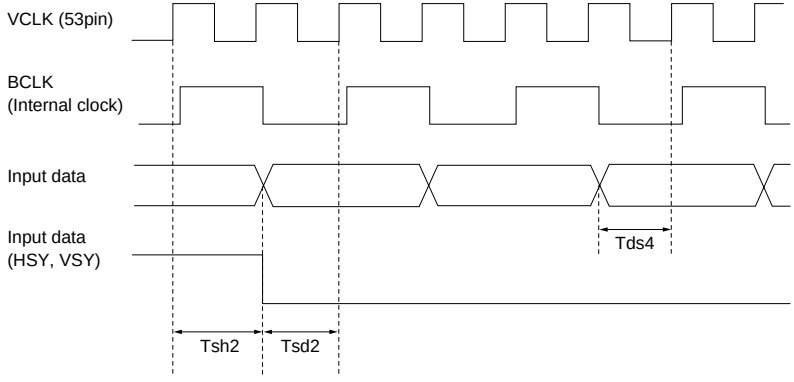


Fig.14

∗ In this mode, the internal clock (BCLK) begins to operate at a halved frequency at the rise of the VCLK input, following the rise of the RSTB pin (pin 52). When HSY is input, phase correction is carried out at the falling edge, as shown in Fig. 14. (In other words, the phase of the internal clock (BCLK) is not determined until HSY is input.)

Table 14

Parameter	Symbol	Min.	Typ.	Max.
Data setup time 4	Tds4	10	—	—
Sync signal hold time 2	Tsh2	10	—	—
Sync signal setup time 2	Tsd2	10	—	—

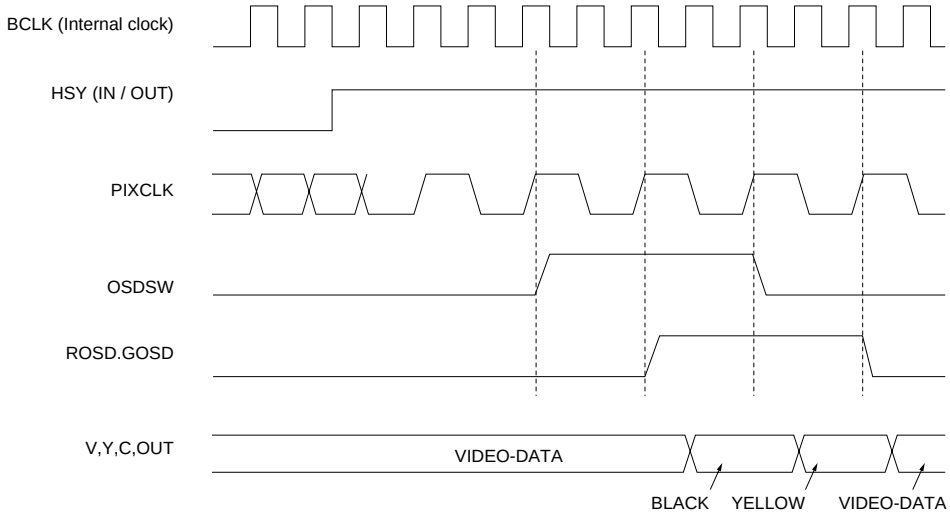


Fig.15 Clock timing with the OSD function

∗ The frequency of the PIXCLK pin output is one-half that of the internal clock. This phase is determined at the rising edge of HSY, as shown in Fig. 15. (In the Encoder Master mode, phase correction is implemented using the HSY output of the BU1424K itself.) The OSD function is effective only during the time that video output is enabled.

2) Output timing

1. Master mode, doubled clock mode

Encoder master (pin 33 = H)

Internal clock = input clock ∗ 1 / 2 (pin 53 = L)

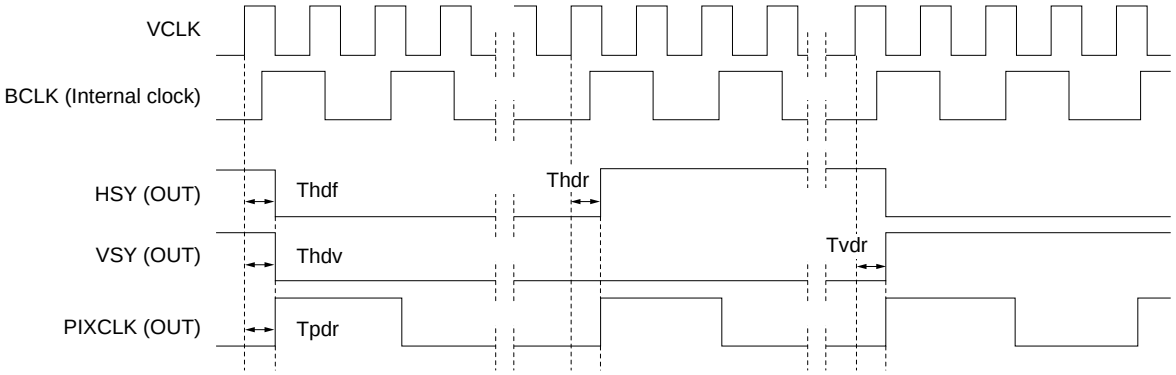


Fig.16 Output timing with a doubled clock

Table 15

Parameter	Symbol	Min.	Typ.	Max.
HSY output delay	Thdr Thdf	—	14	—
VSY output delay	Tvdr Tvdf	—	14	—
PIXCLK output delay	Tpdr Tpdf	—	14	—

2. Master mode, regular clock mode

Encoder master (pin 33 = H)

Internal clock = input clock (pin 53 = L)

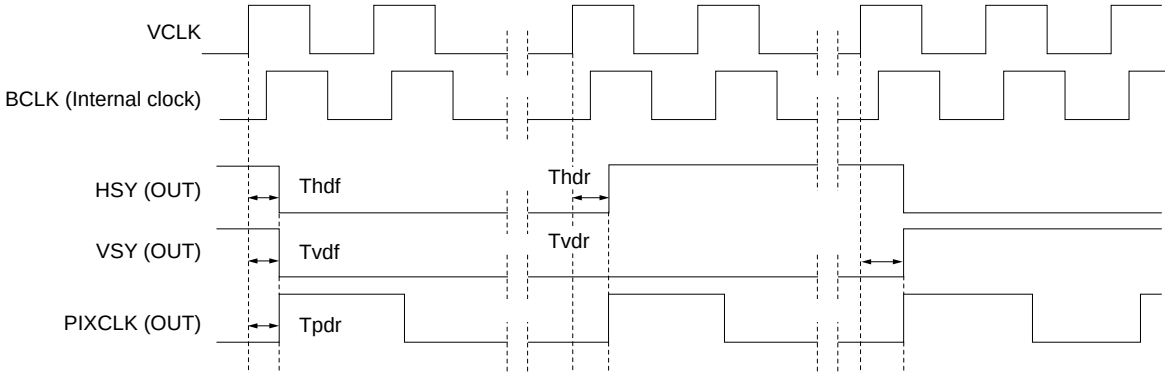


Fig.17 Output timing with a clock at the regular frequency

Table 16

Parameter	Symbol	Min.	Typ.	Max.
HSY output delay	Thdr Thdf	—	10	—
VSY output delay	Tvdr Tvdf	—	10	—
PIXCLK output delay	Tpdr Tpdf	—	10	—

3) Odd / even recognition timing in Slave mode

The BU1424K distinguishes whether the conditions of each field (each time that VSY is input) are odd or otherwise, and internal operation is carried out based on that recognition after the data is input. As a result, HSY and VSY are input under input conditions appropriate to the specified mode, enabling regulated output for the first time. Odd input conditions are indicated below. Timing that does not match these conditions is recognized as an even field.

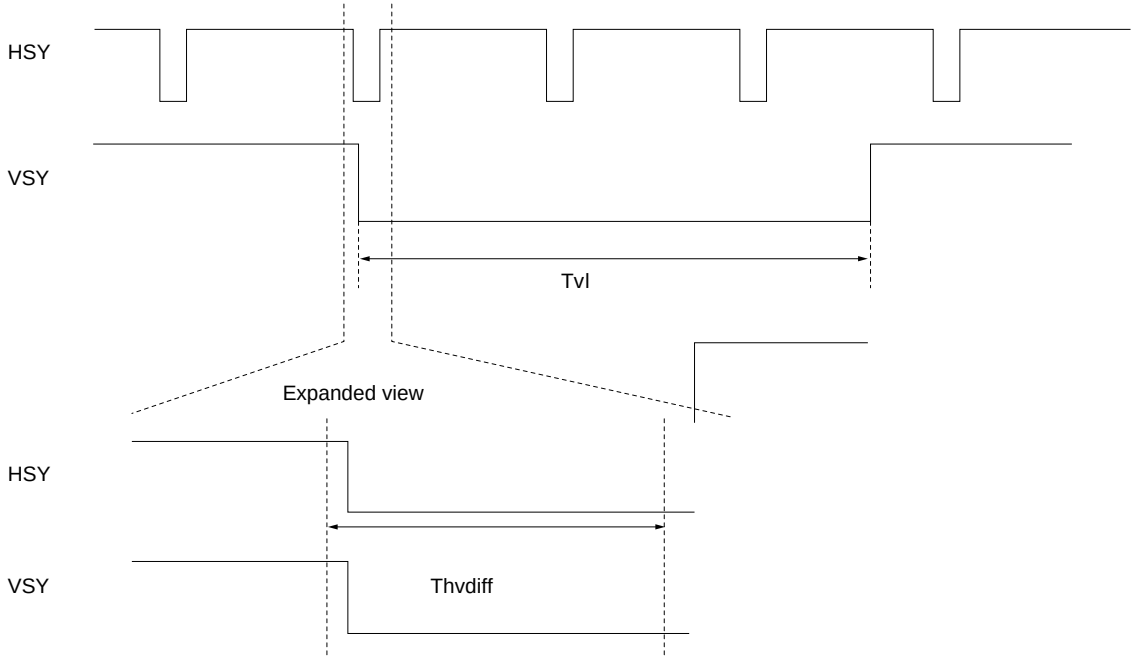


Fig.18 ODD recognition conditions

Table 17: Odd recognition conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
VSY input L interval	Tvl	128	—	—	BCLK
VSY Delay from HSY	Thvdiff	HSY falling edge – 1clk	—	HSY Rising edge – 2clk	BCLK

∗ BCLK = One cycle of internal clock

4) TV signal timing diagram

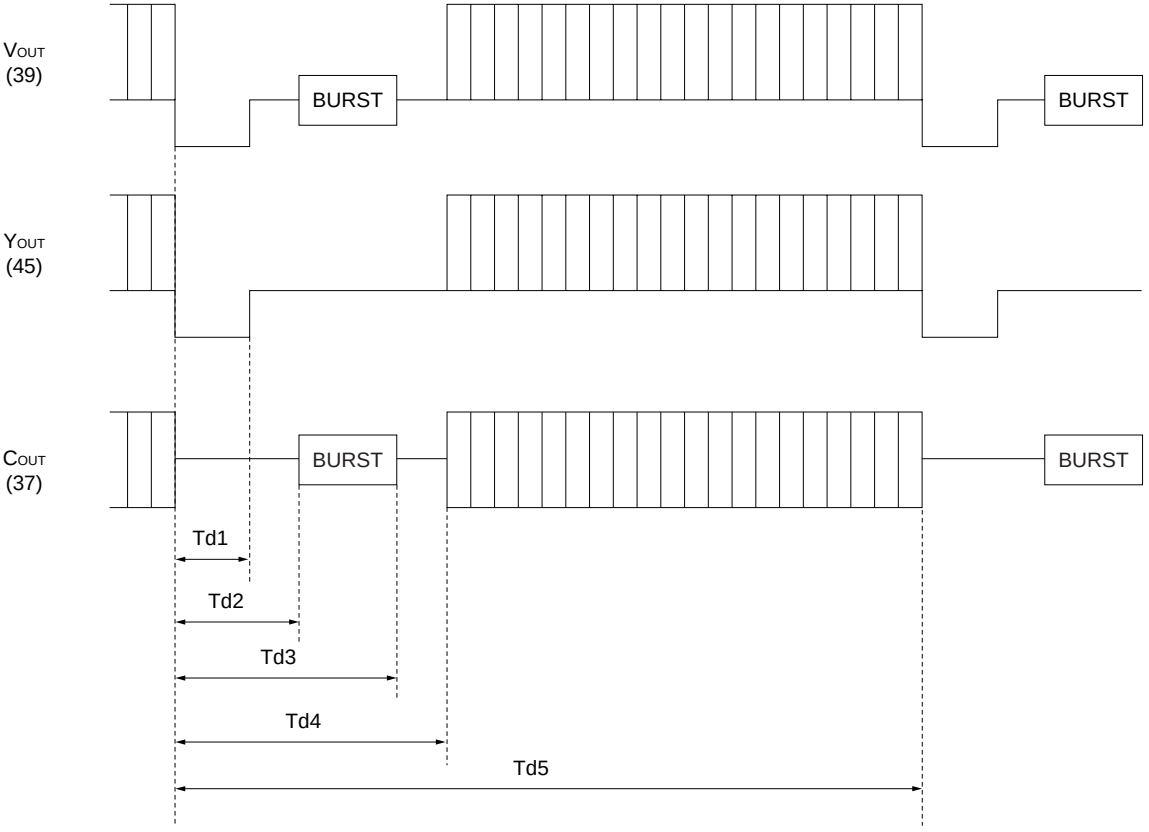


Fig.19

Table 18

Parameter	Symbol	Unit	NTSC		PAL			PAL60		
			V-CD	CD-G	V-CD	CDG2	CDG1	V-CD	CDG2	CDG1
SYNC rise	Td1	BCLK	64	67	64	83	67	64	83	67
Burst start	Td2	BCLK	71	76	76	100	79	71	94	75
Burst end	Td3	BCLK	106	112	106	140	112	106	139	111
Data start	Td4	BCLK	128	135	142	186	149	128	166	135
1-line interval	Td5	BCLK	858	910	864	1135	908	858	1127	902

Frame timing in Video-CD mode
(NTSC / PAL60: Interlace)

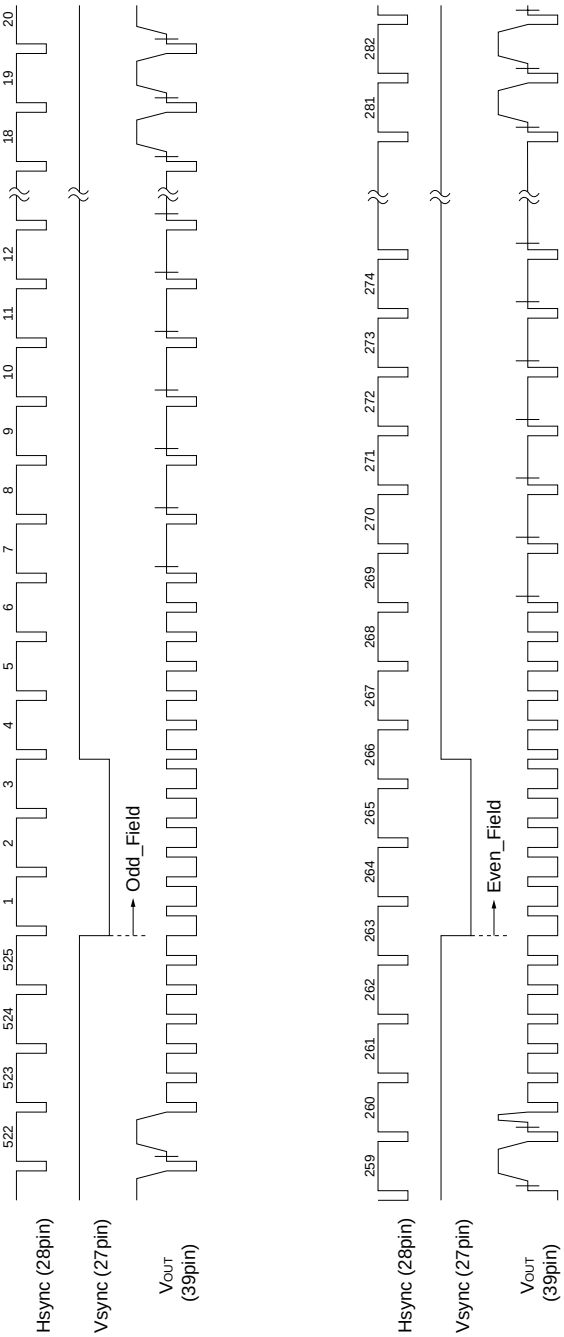


Fig.20

Frame timing in Video-CD mode
(PAL: Interlace)

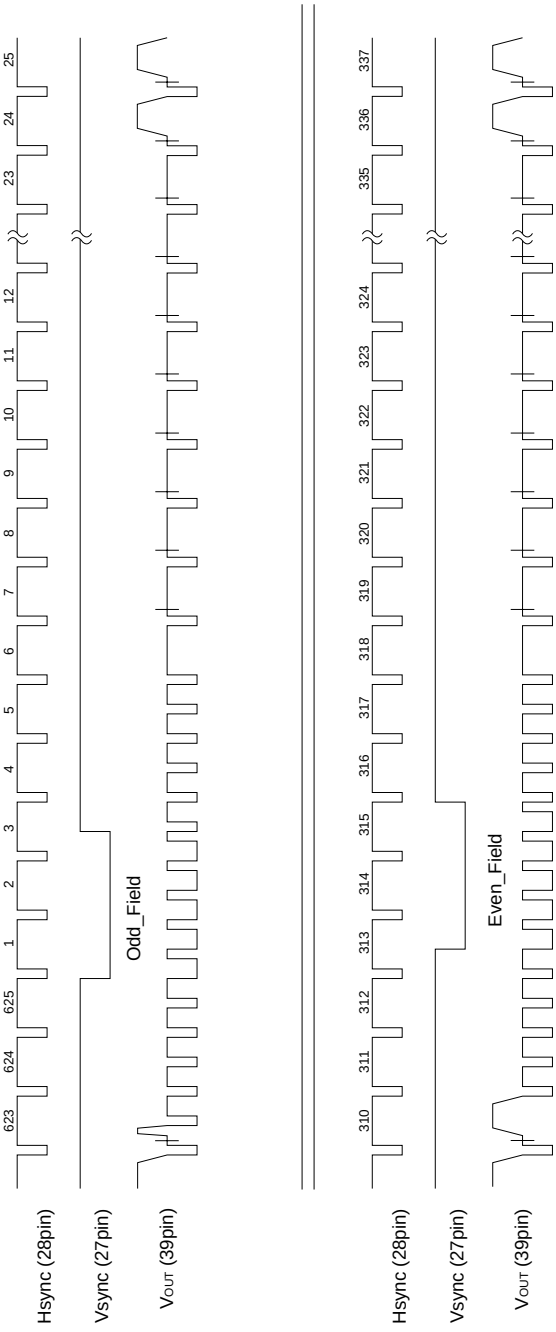


Fig.21

Frame timing in CD-G mode
(NTSC / PAL60: Non-interlace)

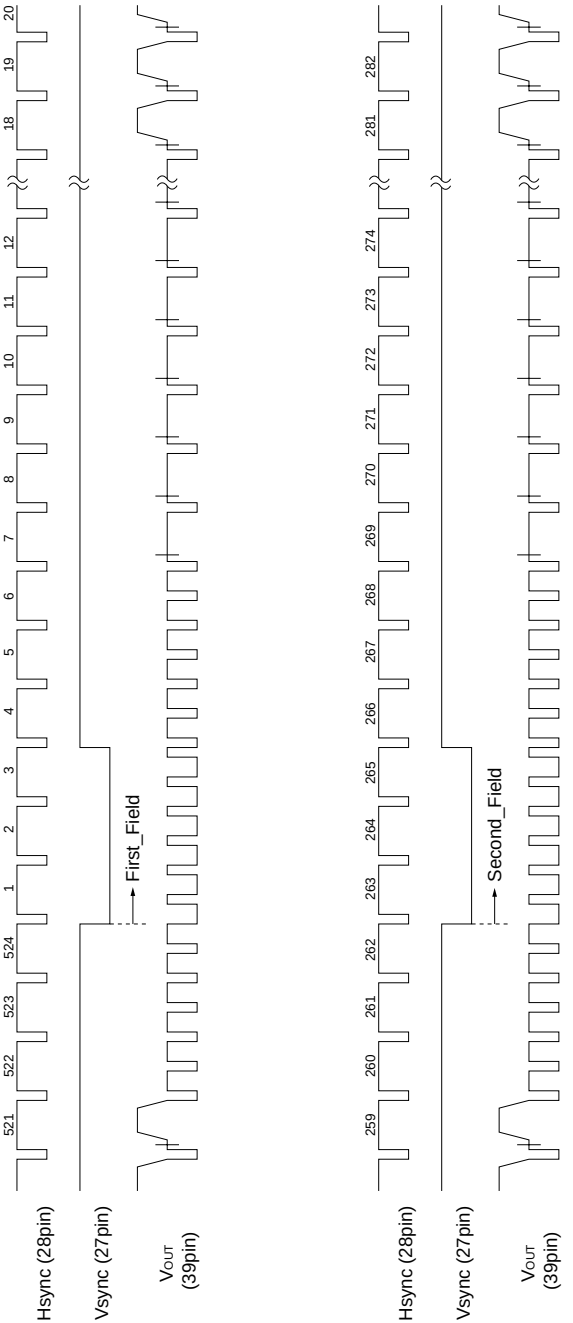


Fig.22

Frame timing in CD-G mode
(PAL: Non-interlace)

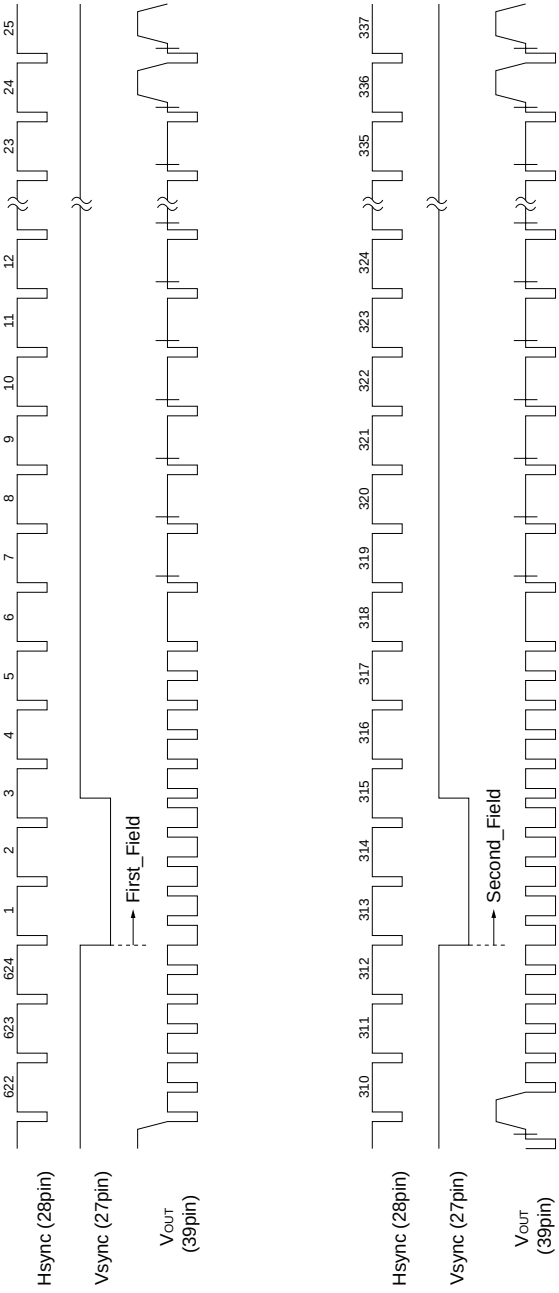


Fig.23

(5) Adjustment of the DAC output level

The voltage level of the DAC output is determined by the DAC internal output current and the DAC output external resistor. The output current per 1 DAC bit is determined by the external resistor of the IR pin (pin 42), as shown below.

I (1LSB) = VVREF / RIR ∗ 1 / 16 [A]····· (equation 6-1)

VREF·····Voltage generated by the regulator circuit in the BU1424K [V]

RIR·····External resistor for the IR pin 1200Ω]

Consequently, when VREF = 1.3V and RIR = 1200Ω, a current of 67.71μA per 1LSB is output. Because the white level of Y is a digital value of 396 (decimal value), the following results:

V (Y white) = 0.0677 × 396 = 26.81[mA]

At this point, if the DAC output external resistance is 37.5Ω, an amplitude of 1.005[V_{P-P}] is obtained.

(6) YUV input mode

With the BU1424K, setting the IM0 pin (pin 23) to HIGH enables a 16-bit YUV input format to be supported. At that time, the timing of U and V can be reversed when data is input, using the H / L state of the Test2 pin. The input conditions for this mode are shown below.

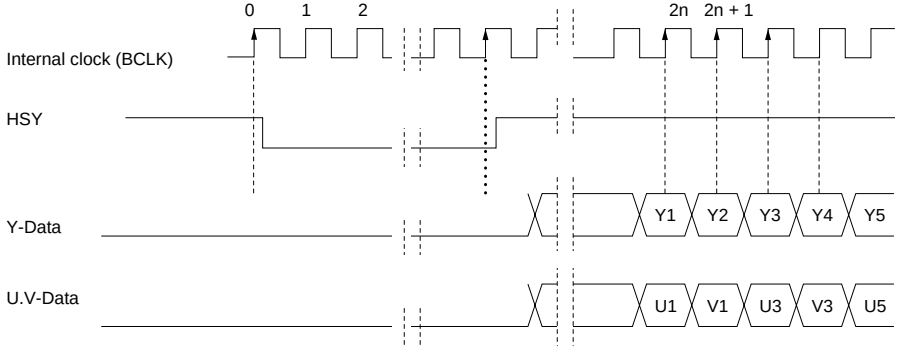


Fig.24 YUV input timing when TEST [2] = L

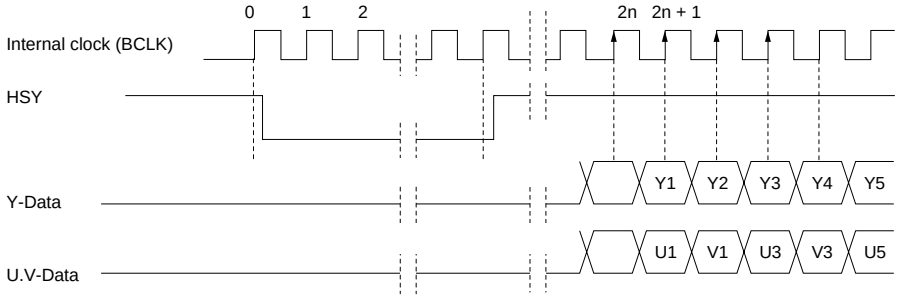


Fig.25 YUV input timing when TEST [2] = H

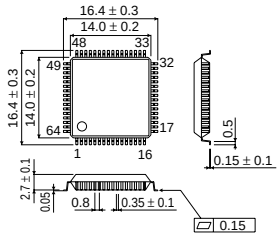
Reversal of the U and V timing using the H / L state of TEST[2] can be controlled regardless of whether CLKSW is HIGH or LOW (the input clock is a doubled clock or not).

∗ When using the RGB input mode, TEST[2] should be fixed at LOW.
∗ In the Master mode, HSYNC is output at the timing shown on the previous page. For that reason, the timing of U and V should be determined by counting from that falling edge. In the Slave mode, the HSY, U, and V data should be input at the timing shown on the previous page.

Table 19

TEST2 (26pin)	CLKSW (53pin)	
0	0	In a doubled clock mode, the timing of U and V is as shown in Fig. 24
0	1	In a regular clock mode, the timing of U and V is as shown in Fig. 24
1	0	In a doubled clock mode, the timing of U and V is as shown in Fig. 25
1	1	In a regular clock mode, the timing of U and V is as shown in Fig. 25

●External dimensions (Units: mm)



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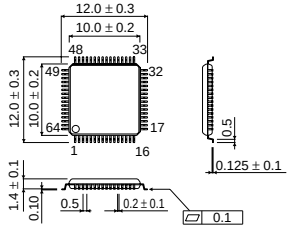

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