

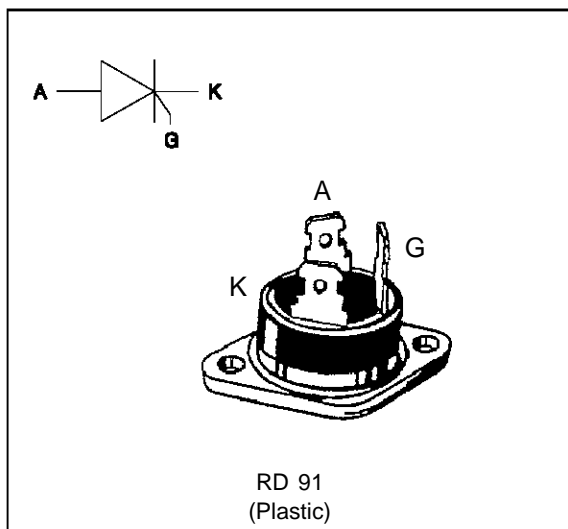
**FEATURES**

- HIGH SURGE CAPABILITY
- HIGH ON-STATE CURRENT
- HIGH STABILITY AND RELIABILITY
- ISOLATED PACKAGE :  
INSULATED VOLTAGE = 2500V<sub>(RMS)</sub>  
(UL RECOGNIZED : E81734)

**DESCRIPTION**

The BTW 66 and BTW 67 Family Silicon Controlled Rectifiers are high performance glass passivated chips technology.

This general purpose Family Silicon Controlled Rectifiers is designed for power supply up to 400Hz on resistive or inductive load.



**ABSOLUTE RATINGS** (limiting values)

Symbol	Parameter			Value	Unit
I <sub>T(RMS)</sub>	RMS on-state current (180° conduction angle)	BTW 66	T <sub>c</sub> =75°C	30	A
		BTW 67	T <sub>c</sub> =75°C	40	
I <sub>T(AV)</sub>	Average on-state current (180° conduction angle, single phase circuit)	BTW 66	T <sub>c</sub> =75°C	20	A
		BTW 67	T <sub>c</sub> =75°C	25	
I <sub>TSM</sub>	Non repetitive surge peak on-state current ( T <sub>j</sub> initial = 25°C )	BTW 66	tp=8.3 ms	420	A
		BTW 67	tp=8.3 ms	525	
I <sup>2</sup> t	I <sup>2</sup> t value	BTW 66	tp=10 ms	400	A <sup>2</sup> s
		BTW 67	tp=10 ms	500	
dI/dt	Critical rate of rise of on-state current Gate supply : I <sub>G</sub> = 100 mA di <sub>G</sub> /dt = 1 A/μs			100	A/μs
T <sub>stg</sub> T <sub>j</sub>	Storage and operating junction temperature range			- 40 to + 150 - 40 to + 125	°C °C
TI	Maximum lead temperature for soldering during 10 s at 4.5 mm from case			230	°C

Symbol	Parameter	BTW 66- / BTW 67-						Unit
		200	400	600	800	1000	1200	
V <sub>DRM</sub> V <sub>RRM</sub>	Repetitive peak off-state voltage T <sub>j</sub> = 125 °C	200	400	600	800	1000	1200	V

**THERMAL RESISTANCES**

Symbol	Parameter		Value	Unit	
Rth (c-h)	Contact (case to heatsink)		0.10	°C/W	
Rth (j-c) DC	Junction to case for DC		BTW 66	1.2	°C/W
			BTW 67	1.0	

**GATE CHARACTERISTICS** (maximum values)

 $P_G (AV) = 1W$     $P_{GM} = 40W$  (tp = 20  $\mu s$ )    $I_{FGM} = 8A$  (tp = 20  $\mu s$ )    $V_{RGM} = 5V$ .

**ELECTRICAL CHARACTERISTICS**

Symbol	Test Conditions			Value		Unit
				BTW 66	BTW 67	
I <sub>GT</sub>	V <sub>D</sub> =12V (DC) R <sub>L</sub> =33 $\Omega$	T <sub>j</sub> =25°C	MAX	50	80	mA
V <sub>GT</sub>	V <sub>D</sub> =12V (DC) R <sub>L</sub> =33 $\Omega$	T <sub>j</sub> =25°C	MAX	1.5		V
V <sub>GD</sub>	V <sub>D</sub> =V <sub>DRM</sub> R <sub>L</sub> =3.3k $\Omega$	T <sub>j</sub> = 125°C	MIN	0.2		V
t <sub>gt</sub>	V <sub>D</sub> =V <sub>DRM</sub> I <sub>G</sub> = 200mA dI <sub>G</sub> /dt = 1.5A/ $\mu s$	T <sub>j</sub> =25°C	TYP	2		$\mu s$
I <sub>L</sub>	I <sub>G</sub> = 1.2 I <sub>GT</sub>	T <sub>j</sub> =25°C	TYP	50		mA
I <sub>H</sub>	I <sub>T</sub> = 500mA gate open	T <sub>j</sub> =25°C	MAX	75	150	mA
V <sub>TM</sub>	BTW 66 I <sub>TM</sub> = 60A BTW 67 I <sub>TM</sub> = 80A tp= 380 $\mu s$	T <sub>j</sub> =25°C	MAX	2.2	2.0	V
I <sub>DRM</sub> I <sub>RRM</sub>	V <sub>DRM</sub> Rated V <sub>RRM</sub> Rated	T <sub>j</sub> =25°C	MAX	0.02		mA
		T <sub>j</sub> = 125°C		6		
dV/dt	Linear slope up to V <sub>D</sub> =67%V <sub>DRM</sub> gate open	V <sub>DRM</sub> ≤ 800V V <sub>DRM</sub> ≥ 1000V	T <sub>j</sub> = 125°C	MIN	500 250	V/ $\mu s$
t <sub>q</sub>	V <sub>D</sub> =67%V <sub>DRM</sub> dI <sub>TM</sub> /dt=30 A/ $\mu s$	I <sub>TM</sub> = 60A V <sub>R</sub> = 75V dV <sub>D</sub> /dt= 20V/ $\mu s$	T <sub>j</sub> = 125°C	TYP	100	$\mu s$

Package	$I_{T(RMS)}$	$V_{DRM} / V_{RRM}$	Sensitivity Specification
	A	V	BTW
BTW 66 (Insulated)	30	200	X
		400	X
		600	X
		800	X
		1000	X
		1200	X
BTW 67 (Insulated)	40	200	X
		400	X
		600	X
		800	X
		1000	X
		1200	X

Fig.1 : Maximum average power dissipation versus average on-state current (BTW 66).

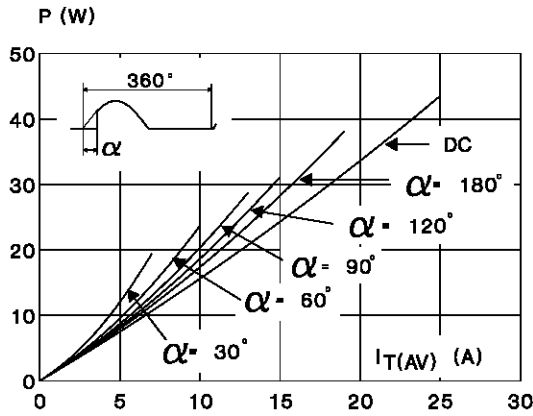


Fig.3 : Maximum average power dissipation versus average on-state current (BTW 67).

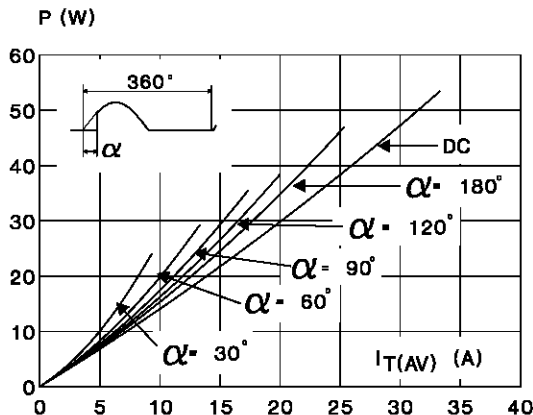


Fig.2 : Correlation between maximum average power dissipation and maximum allowable temperatures ( $T_{amb}$  and  $T_{case}$ ) for different thermal resistances heatsink + contact (BTW 66).

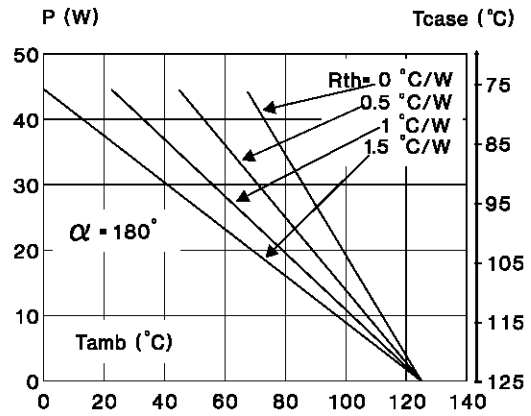
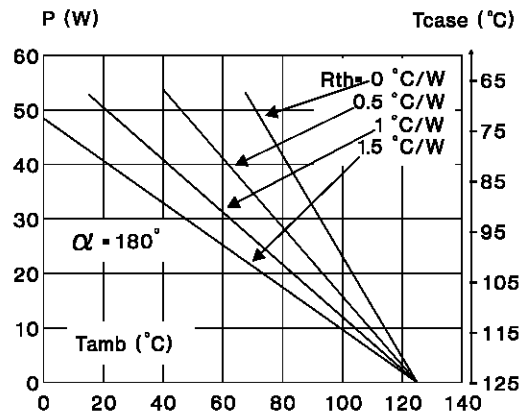
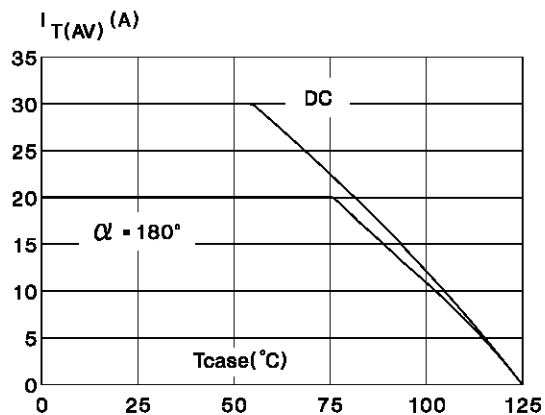


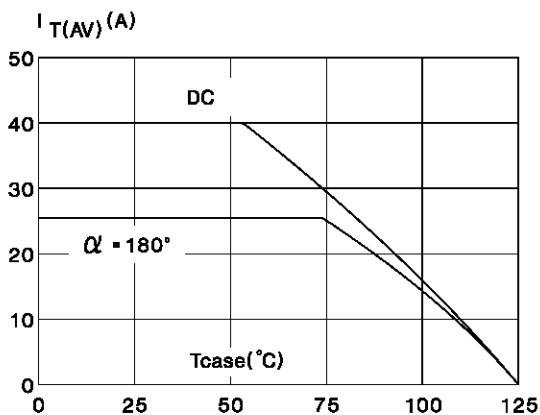
Fig.4 : Correlation between maximum average power dissipation and maximum allowable temperatures ( $T_{amb}$  and  $T_{case}$ ) for different thermal resistances heatsink + contact (BTW 67).



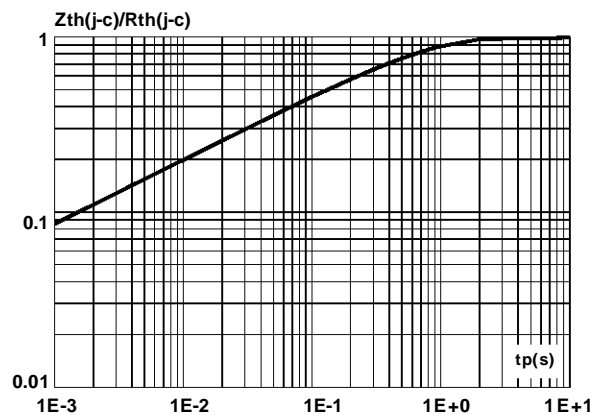
**Fig.5** : Average on-state current versus case temperature (BTW 66).



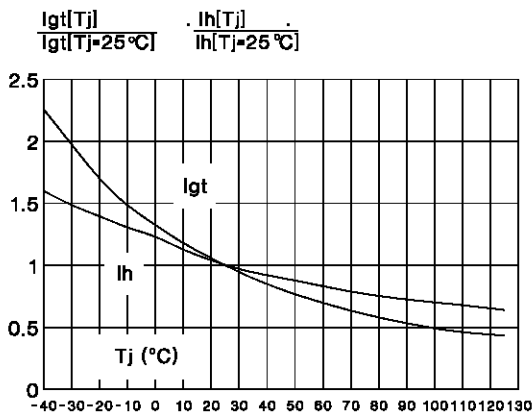
**Fig.6** : Average on-state current versus case temperature (BTW 67).



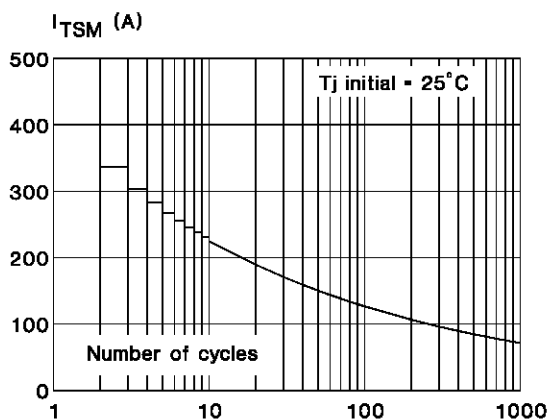
**Fig.7** : Relative variation of thermal impedance junction to case versus pulse duration.



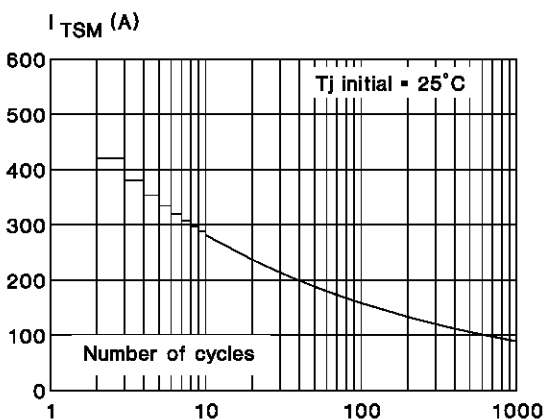
**Fig.8** : Relative variation of gate trigger current versus junction temperature.



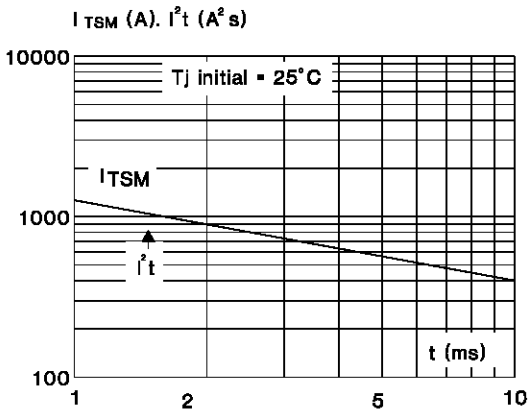
**Fig.9** : Non repetitive surge peak on-state current versus number of cycles (BTW 66).



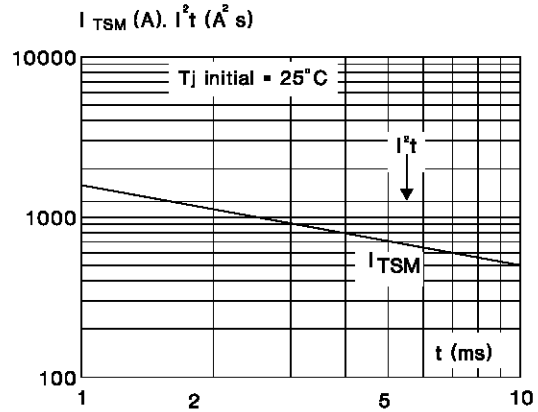
**Fig.10** : Non repetitive surge peak on-state current versus number of cycles (BTW 67).



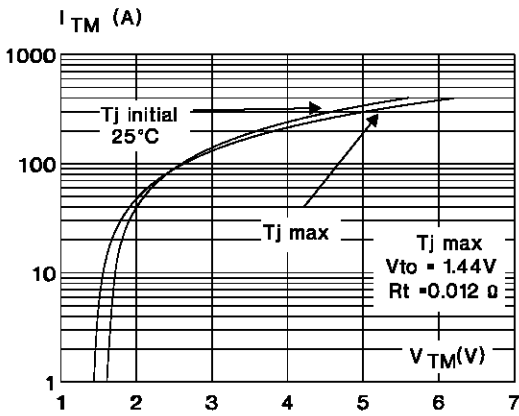
**Fig.11** : Non repetitive surge peak on-state current for a sinusoidal pulse with width :  $t \leq 10$  ms, and corresponding value of  $I^2t$  (BTW 66).



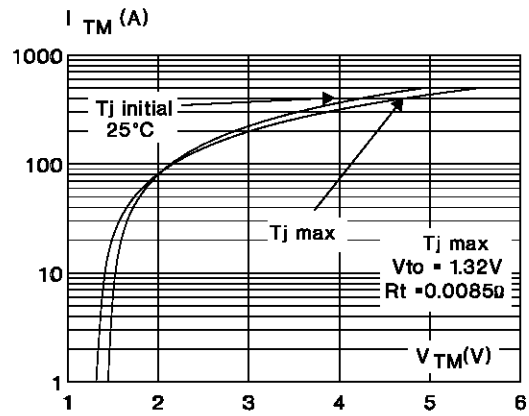
**Fig.12** : Non repetitive surge peak on-state current for a sinusoidal pulse with width :  $t \leq 10$  ms, and corresponding value of  $I^2t$  (BTW 67).



**Fig.13** : On-state characteristics (maximum values) (BTW 66).

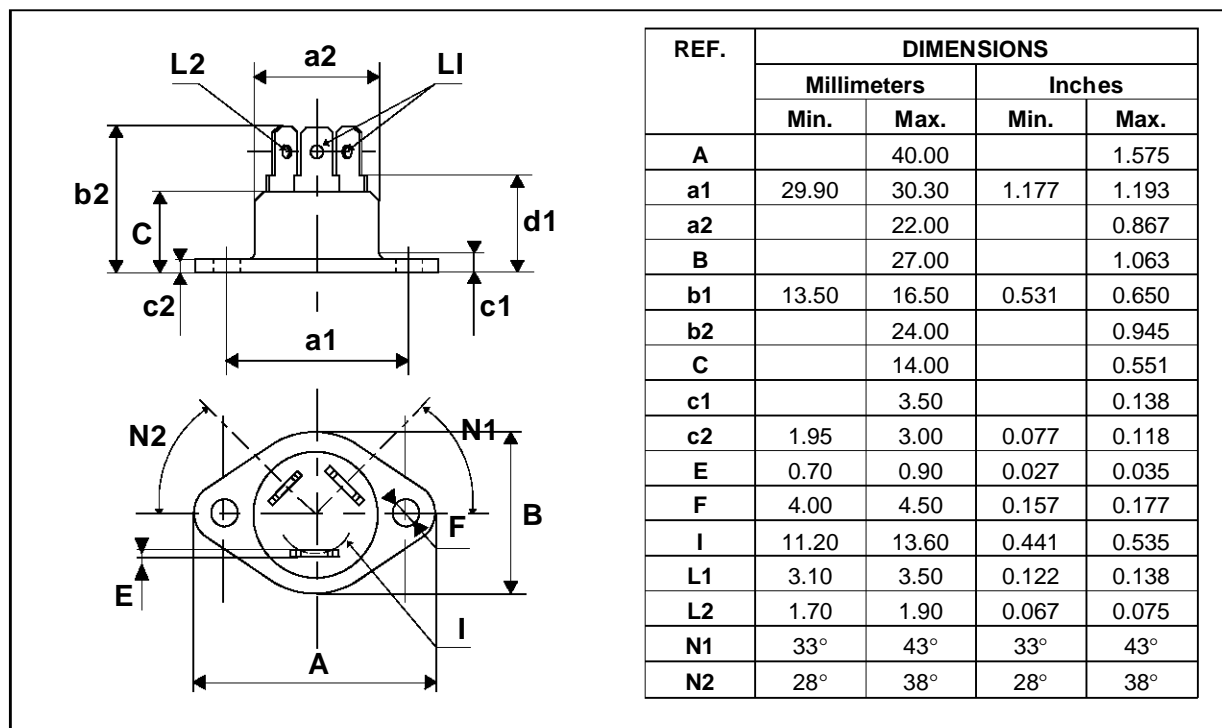


**Fig.14** : On-state characteristics (maximum values) (BTW 67).



**PACKAGE MECHANICAL DATA**

RD 91 Plastic



Marking : type number  
Weight : 20 g

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