Depletion-Mode MOSFETs Expand Circuit Opportunities

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Introduction

A principal advantage of the depletion-mode MOSFET is its ability to perform at higher operating voltages than its JFET counterpart. As a depletion-mode structure, the MOSFET permits the added flexibility of allowing the gate potential not only to be higher but to be of either polarity. Earlier, small-signal MOSFETs were classed as being quite sensitive to ESD. With the introduction of the ND2012 and ND2406 series, with BV > 200 V and > 240 V respectively, sensitivity to ESD has been greatly reduced.

Depletion-Mode vs. Enhancement-Mode

Three Classes of FETs

Perhaps the simplest definition of depletion-mode operation is shown by the transfer characteristic (biasing) curves (Figure 1b). Drain current is reduced to zero when the gate voltage reaches a critical cutoff voltage, opposite in polarity to that of the drain voltage. The n-channel JFET (depletion-mode), (Figure 1a) has a positive-polarity drain voltage and is controlled by a negative-polarity gate voltage. The depletion-mode MOSFET may also perform in the enhancement-mode. The n-channel enhancement-mode MOSFET (Figure 1c), requires a positive-polarity gate voltage referenced to the source to provide current conduction.

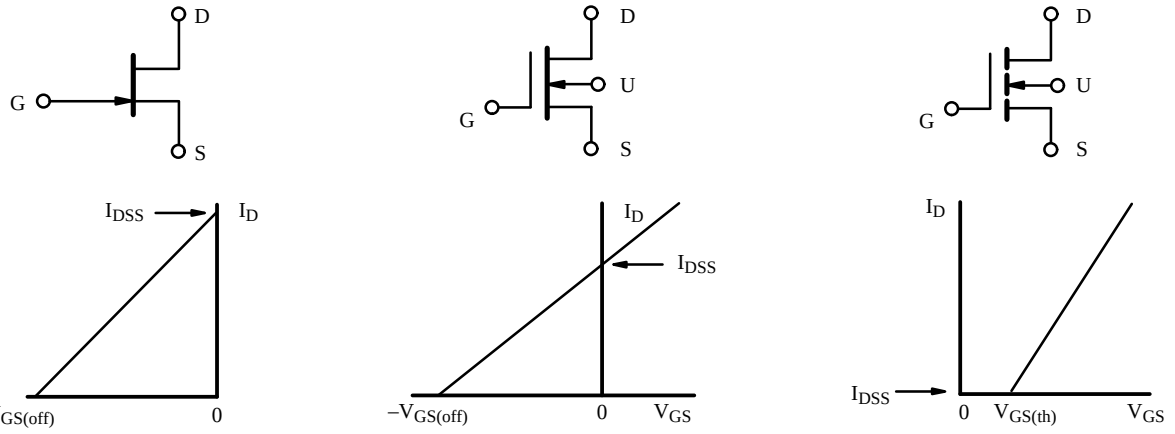
The Structure of MOSFETs

All MOSFETs are classified as either depletion-mode or enhancement-mode. Although they can be fabricated as n- or p-channel, generally we find n-channel MOSFETs in either mode and p-channel MOSFETs available only as enhancement-mode devices.

There are, however, three fundamental styles of MOSFETs regardless of mode. The classic planar MOSFET, shown in cross-section (Figure 2), the short-channel double-diffused MOSFET (DMOS FET), and the vertical power MOSFET (Figure 3). The features of each style are distinguished by performance.

When viewing the cross section, the distinguishing feature that quickly identifies the mode is whether a diffused channel spans the gap from source to drain. The absence of a visible channel (Figures 2a and 3a) identify the enhancement-mode MOSFET.

N-Channel Devices*



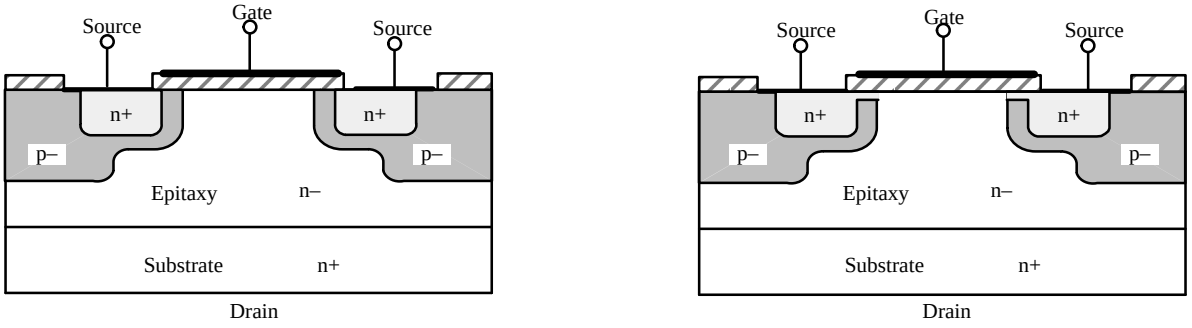
1a) Depletion-Mode JFET **1b)** Depletion-Mode MOSFET **1c)** Enhancement-Mode MOSFET

*P-channel devices have opposite arrows (⍰) and polarities versus n-channel devices.

Figure 1. Classification of FETs

2a) Enhancement-Mode **2b)** Depletion-Mode

Figure 2. Classic Planar MOSFETs



3a) Enhancement-Mode **3b)** Depletion-Mode

Figure 3. Vertical Power MOSFET

The Performance of a Depletion-Mode MOSFET

Regardless of whether or not a MOSFET is an n- or p-channel device, there are fundamental performance differences between depletion-mode and enhancement-mode MOSFETs. There are also important, though secondary, differences between styles of MOSFET: planar, DMOS, or vertical. The principle differences will be clarified by studying the transfer characteristics (biasing), (Figure 1).

The transfer characteristic of the n-channel, depletion-mode MOSFET (Figure 1b). Because the gate is isolated (see Figure 2b), V_{GS} can be reversed without creating a gate current. The gate may be made either positive or negative with respect to the source. By allowing the gate-to-source potential to go positive and increasing the magnitude of gate voltage, additional free electrons will be attracted beneath the gate oxide. This further enhances the diffused channel and allows I_D to become greater than I_{DSS}!

This mode of operation results in a unique series of output characteristics where, for the n-channel depletion-mode MOSFET, we see near-linear performance in what appears as the enhancement region (Figure 4). The foregoing establishes that the depletion- mode MOSFET is a “normally-on” device; that is, when $V_{GS} = 0$, $I_D = I_{DSS}$. When a normally-off device is needed, the enhancement-mode MOSFET is selected.

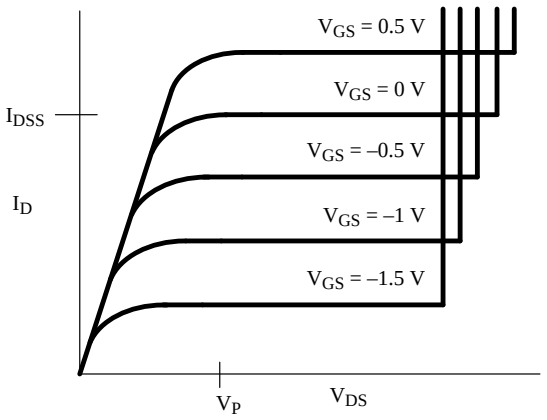


Figure 4. Output Characteristics N-Channel Depletion-Mode MOSFET

Applications For Depletion-Mode MOSFETs

As a Current Regulator

An ideal current source supplies a fixed current to a load independent of the impressed voltage. Such a source would exhibit zero output conductance. Aside from the fact that depletion-mode MOSFETs can handle higher voltages and greater currents than most JFETs, they exhibit two characteristics which make them near-ideal current regulators. First, when the V_{DS} voltage exceeds pinch-off V_P, the saturation characteristics, exhibit near-constant current (low output conductance) over a wide voltage range (Figure 4). Second, performance as a depletion-mode transistor allows for simplified biasing to achieve the desired results.

Basic Regulator Circuit

For a given device where I_{DSS} and $V_{GS(off)}$ are both known, the value of bias required to establish the regulating current may be approximated by

$$V_{GS} = V_{GS(off)}\left[1-\left(\frac{I_D}{I_{DSS}}\right)^{1/2}\right] \quad (1)$$

The biasing resistor, R_S, required in the source of the MOSFET is

$$R_S = \frac{V_{GS}}{I_D} \simeq \frac{V_{GS(off)}}{I_D}\left[1-\left(\frac{I_D}{I_{DSS}}\right)^{1/2}\right] \quad (2)$$

A change in either supply voltage or load impedance will change the regulating current in proportion to the magnitude of the output conductance of the MOSFET.

$$dI_D = dV_{DS}\ g_{os} \quad (3)$$

Table 1

I_D/I_{DSS}	% Regulation
0.02	0.5
0.05	1.0
0.10	1.5
0.20	2.5
0.30	3.5

A typical constant-current regulator circuit that employs a depletion-mode MOSFET (Figure 5). As with any depletion-mode FET, the lower the ratio between I_D and I_{DSS} the better the regulation (Figure 6 and Table 1).

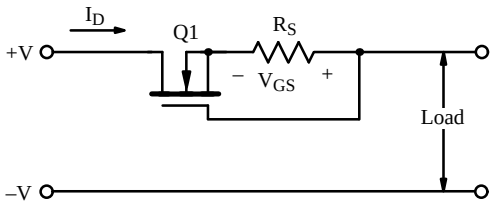


Figure 5. Basic Regulator Circuit

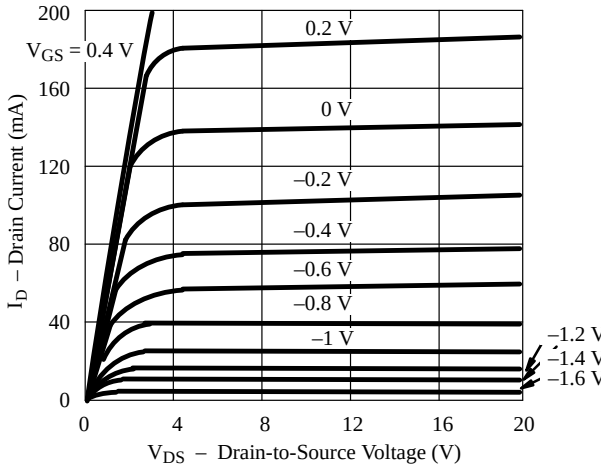


Figure 6. Output Characteristics of a Depletion-Mode MOSFET (ND2020L)

Extending Power Level Using MOSPOWER

The n-channel, depletion-mode MOSFET can be used in conjunction with an enhancement-mode power device to give an appreciable boost to the power handling capability of a current regulator (Figure 7). Both the operating voltage and regulating current are set by the selection of the power FET, Q2. Regulation may suffer somewhat when using large power FETs due to the higher g_{os} typical of large power FETs. Q2, operating in the linear mode, will, in all likelihood, require a heatsink. The basic regulator circuit, Q1 and R_S, is used to establish a small bias current that, in conjunction with R1, sets the bias level for the enhancement-mode power FET.

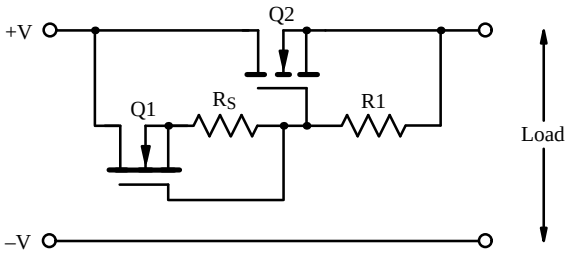


Figure 7. Extended-Range Current Limiter

A Simple Regulator for Telecom

Modern telephone handsets are steadily increasing their electronic content. Useful features, such as the ability to retain the last number dialed, require constant voltage to retain the information in memory. Typically, small memory ICs require only a few microamperes at 3 to 4 V to perform. This sustaining voltage must be available at all times, even when the phone is inactive or “on hook.” Some handsets use a small battery cell to fill this need, while other designs use the –48-V power supply which is available from the telephone line.

To utilize the incoming line, one needs to reduce the voltage and loosely regulate it, without consuming much power. In most systems, current drain in excess of 10 to 15 µA will alert the central office to an “off hook” condition and the subscriber’s phone is presumed “busy.” A simple depletion-mode regulator using the ND2410 can satisfy these requirements very economically. The depletion-mode MOSFET is used in a current-regulator mode to supply 10 µA to a 500-kΩ load (Figure 8). This establishes a voltage of 5-V to power the memory circuit. If the memory requires 2 µA, only 8 µA will flow through the resistor, and the voltage drops to 4 V, which is sufficient to sustain the memory. Should the telecom line rise to 60 V, the current regulator continues to supply a fixed 10 µA to the load; the surplus voltage is dropped by the MOSFET. The regulation is not precise, but more than sufficient to provide a simple and reliable solution. Alternatives such as 3-terminal bipolar regulators require high bias currents (over 1 mA) and are not readily available to sustain the high voltages necessary for use on telephone lines.

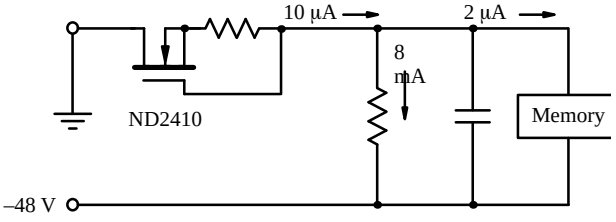


Figure 8. Telecom Voltage Regulator for Memory—Resident Redialing

As a Switch

When considering a switch, we usually select one whose natural, quiescent state is either normally-on or normally-off. With no applied power (or voltage), the depletion-mode MOSFET is normally-on.

Improving the dv/dt of Thyristors

The ND2410 can be used very effectively in power SCR circuits to improve the critical dv/dt rating. Spurious turn-on of an SCR caused by dv/dt can result in permanent damage to an SCR or an out-of-sequence turn-on that can have disastrous effects in high-powered phase-control equipment.

Traditionally, SCRs fired by pulse transformers have used a resistor from gate to cathode to shunt false gate signals caused by dv/dt (Figure 9). This method requires a large wattage resistor, since the normal gate trigger signal is also applied across the resistor. The resistor, therefore, shunts part of the normal gate current, thus reducing the signal available for adequate turn-on of the SCR. The ideal solution would be a shunting resistor that seems to disappear when a normal gate signal is applied.

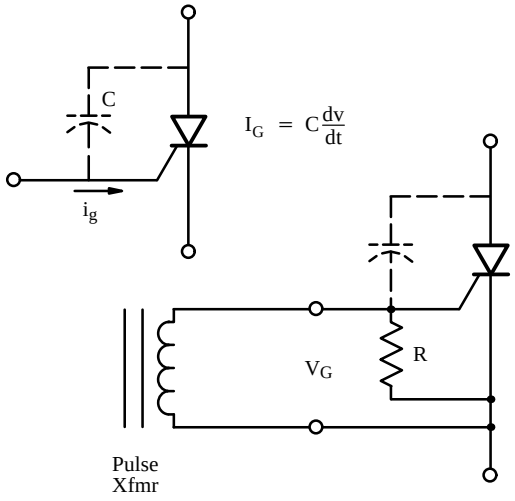


Figure 9. dv/dt Triggering of SCRs

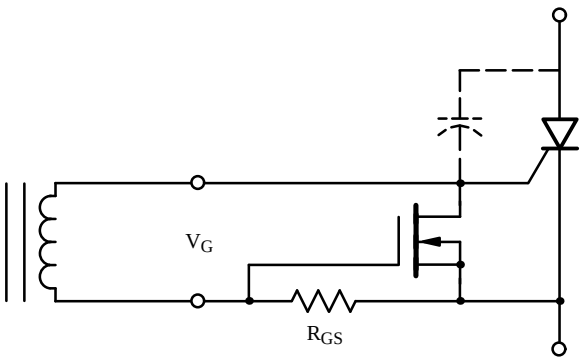


Figure 10. Depletion-Mode Active Shunt

Just such an effect can be achieved using the normally-on feature of the ND2410 (Figure 10). With no gate pulse applied, the depletion-mode transistor is “on” with an equivalent resistance of about 10 Ω. When the gate current is applied, the voltage drop across R_{GS} turns the transistor off, allowing all of the gate current to flow through the SCR gate.

Since the MOSFET turns off in a few nanoseconds, it has very little effect on normal SCR operation. In an actual experiment, the dv/dt of a 25-A SCR (similar to a 2N692) was improved from 300 V/µs (with no gate shunt network) to 2000 V/µs with the depletion-mode shunt.

Some suggestions for effective operation:

1. Use a fast-rising gate pulse: $I_G > 3 \times I_{gt}$
2. The shunt should be located as physically close to the SCR gate terminal as possible to reduce the winding inductance and noise pick-up from long gate wires.
3. $R_{GS} \geq \frac{V_{GS(off)}}{I_G}$
4. Do not use with non-isolated gate drive circuits; a pulse transformer should be used.