Thermal Characteristics of Siliconix's LITTLE FOOT® Family of Surface-Mount MOSFETs

Jim Harnden

Although a wide selection of digital and linear ICs have been available in surface-mount packages for some time, circuits that require power devices have, for the most part, required "mixed-technology" assembly processes. Several versions of DPAK and SOT packages evolved in an attempt to provide compatible discrete solutions. Both, however, have limitations. The DPAK provides, at best, tolerable compatibility with other surface-mount components, and it offers little density advantage over "through-hole" technologies. SOT packages are more compatible with standard SOIC (small outline IC) packaging but have severely limited thermal transfer capabilities. And they accommodate only the smallest power MOSFET die.

Siliconix's LITTLE FOOT family of surface-mount power MOSFETs provide a true surface-mount alternative that boasts greatly improved thermal transfer characteristics, high current handling capability, and low on-resistance. The LITTLE FOOT family includes dual and single power MOSFETs in 8-pin and 16-pin SO packages. High current handling capability and low on-resistance are possible because of Siliconix's industry-leading SiMOS 2.5 MOSFET technology, combined with a custom copper leadframe that allows tiny SO-8 packages to achieve 2 W of internal power dissipation.

While standard small-outline (SO-8) surface-mount packages offer limited potential for direct heat dissipation, the copper leadframes designed for the LITTLE FOOT family maximize heat transfer to the PC board. This reduced thermal impedance, combined with very low on-resistance MOSFETs, greatly extends the range of surface-mount technology in power applications.

The copper leadframes are designed to bring the die bond pad in thermal contact with PC board traces through as many pins as possible. In SOIC packaging, the close proximity of the silicon die to the PC board contributes to efficient thermal transfer. Because its mass is considerably greater than that of the die, the copper leadframe also serves as a very efficient heat spreader.

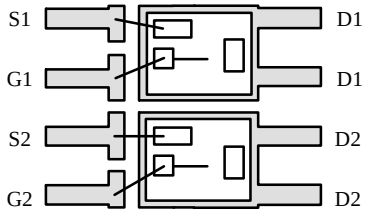

Figure 1a. Dual MOSFET SO-8 Leadframe

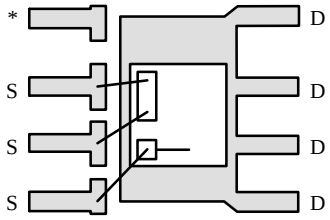

Figure 1b. Single MOSFET SO-8 Leadframe

*All parts except Si9400, Si9405, Si9410 and Si9420 have additional source connections on Pin 1.

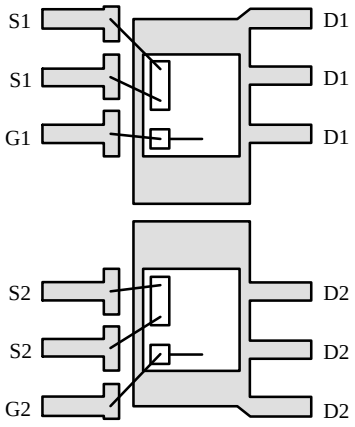

Figure 1c. Dual MOSFET SO-16 Leadframe

The SO-8 package is available in single or dual die versions with the die substrate brought out on four or two pins respectively. The SO-16 is available as a dual only, with the die substrates available on three pins each.

The common multi-layer PC board and its printed copper conductors can play a significant role in dissipating heat from electrical components. Unfortunately, the extent of the effect on a working circuit board is almost impossible to calculate with any precision. While the thermal conductivity of various weights of copper-clad and PC board material are well characterized and available (see references), the proximity of neighboring components on densely populated surface-mount boards, the effects of multi-layer board construction, solder masks, etc., dominate the equations. The references at the end of this application note are offered for those attempting a thermal model; but, to date, significant data has come only from characterization of best- and worst-case prototypes.

Thermal Transfer Characterization

The data presented here was obtained using the MOSFET's intrinsic diode to measure the die junction temperature. The thermal characteristics of each MOSFET's intrinsic diode have been determined; thus, the diode provides a predictable thermal sensor located precisely at the junction in question. At the beginning of each thermal dissipation test, the diode was first measured to determine the die's "ambient" starting temperature (Figure 2a). The device was then forced to dissipate a controlled power level (Figure 2b) for a precise amount of time, and the diode was immediately remeasured to determine the resulting junction temperature increase (Figure 2c). During step two (Figure 2b), the power level was regulated by applying a drain voltage (5 V) and varying the MOSFET's gate voltage to yield a programmed drain current, consistent with the desired power level of each test. (The power level was increased proportionally for shorter pulse durations to increase resolution.) The complete series of tests was performed for each die on each lead frame connected to thermally best- and worst-case PC board layouts. The PC board layouts tested are reproduced (1:1) next to each set of results in Figure 3. Actually, the layout representing the best case is more correctly a single-sided, maximum-copper, one-inch square board that is easily surpassed by the thermal dissipation of the larger, multi-layered boards used in most applications. The worst-case example employs the "standard" spacing and trace width used for non-power devices. The worst-case example was coated with a solder mask and the best-case example was left uncoated.

Pulsed Power Capability

The characteristics shown in Figure 3a and 3b are presented as the power level that a room temperature device can absorb for a given amount of time without exceeding $T_{j(max)}$ = 150°C (the absolute maximum junction temperature rating). An approximation of the pulse duration or power level for a junction temperature increase from an elevated ambient to $T_{j(max)}$ can be obtained by multiplying the indicated power by the ratio $\Delta T/125°C$.

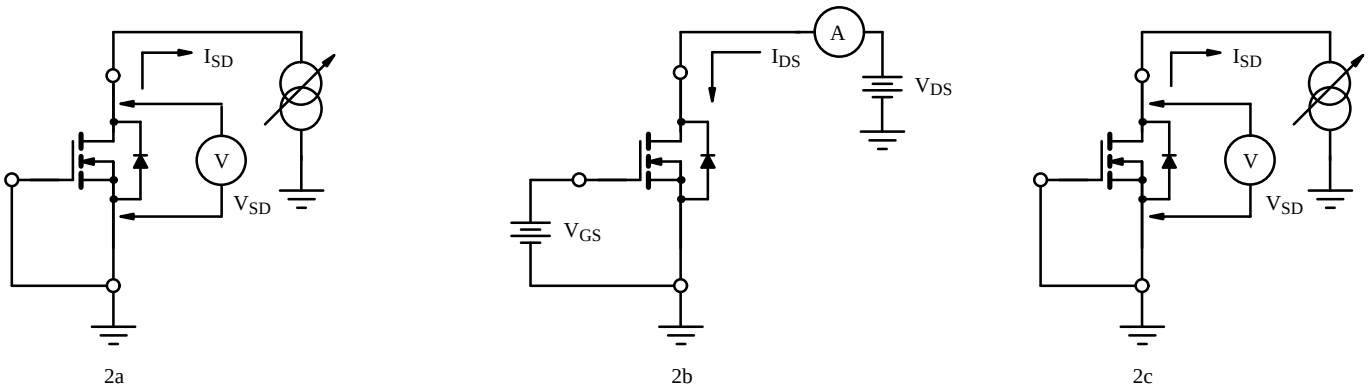

Figure 2. Thermal Impedance Test Sequence

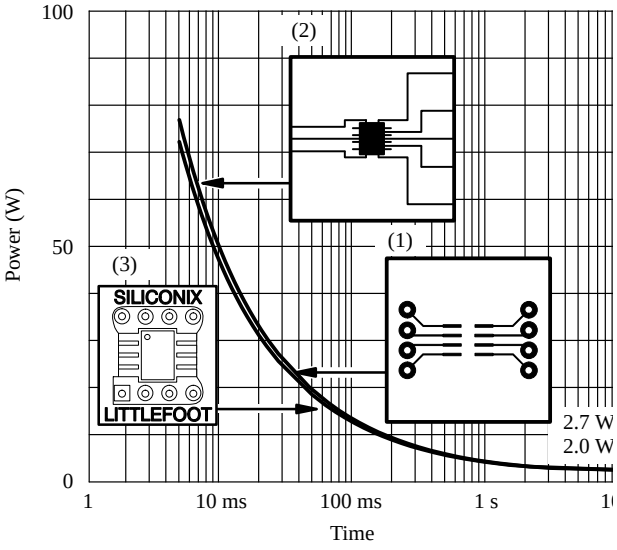

Figure 3a. Power vs. Pulse Duration for Typical Devices in the Dual SO-8 Package (as shown in Figure 1a)

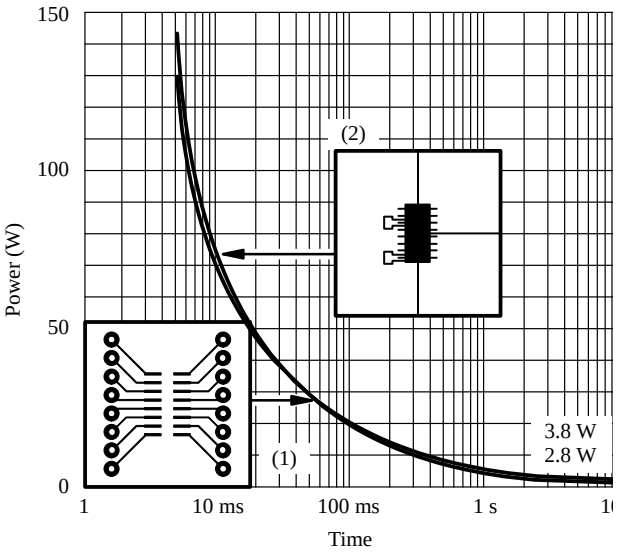

Figure 3b. Power vs. Pulse Duration for the Single Die SO-8 Package or a Dual Die SO-16 Package (as shown in Figures 1b and 1c)

Note:

The test PC board layout (1) is 1-inch square with minimum trace wid typical of those used for digital layouts. Test PC board layout (2) is als 1-inch square but with maximum copperclad area left on the board. Als for comparison, layout (3) is our standard SO-8/DIP adapter which thermally very much like the worst-case example (1) above.

Conclusion

The thermal dissipation of the worst-case, minimum-trace-width layout was made even worse by covering all but the soldered portion of the traces with a solder mask. The standard LITTLE FOOT SO-8/DIP adaptor board was also tested and found to have very similar thermal characteristics to that of the worst-case example. The thermal results of a typical device on each board is shown in Figures 3a and 3b. The thermal characteristics of the single die SO-8 are identical to those of each die in the dual SO-16 (see Figure 3b).

Although hard to resolve from the curves, the maximum size copper traces increased the steady-state (defined as greater than 10 seconds) power dissipation approximately 25% in each case. At shorter pulse widths, the copper area on the PC board has less effect, since the heat does not have time to transfer from the leadframe to the board before the measurement is taken.

With the selection of $r_{DS(on)}$ available in the LITTLE FOOT product line, the option often exists to choose a device with sufficiently low internal dissipation so as to allow the entire board to be evenly populated and connected with the same line widths without regard to the components' analog, power, or digital function.

References

1. A. J. Chapman, "Heat Transfer", Second Edition, Macmillan 1967.
2. R. H. Norris, et al., "Heat Transfer Data Book", General Electric Corporate Research and Development, Schenectady, N.Y.
3. Fredric Wenthen, "The Heat Sink Effect of Printed Conductors", IEEE Transactions on Parts, Hybrids and Packaging, Vol. PHP-12, No. 2, June 1976.