Unclamped Inductive Switching Rugged MOSFETs for Rugged Environments

Ed Oxner and Philip A. Dunning

The evolution of the power MOSFET has resulted in a very rugged transistor. The semiconductor industry defines this ruggedness as the capability to withstand avalanche currents when subjected to unclamped inductive switching. Historically, MOSFET manufacturers chose to quantify ruggedness, not based principally on individual performance, but rather on comparative performance with other manufacturers. Siliconix has optimized the cell structure of power MOSFETs, resulting in a new class of extremely rugged devices. Today's avalanche-rated MOSPOWER FET exhibits a ruggedness that far exceeds the performance of any power MOSFET of earlier years.

This application note reviews the history of unclamped inductive switching (UIS) and examines various theories pertaining to failure. It further identifies what appears to be two related mechanisms — thermal and bipolar — believed to be responsible for failure during unclamped inductive switching and concludes by recommending how a power MOSFET should be qualified for ruggedness in the data sheet.

Two failure modes exist when MOSFETs are subjected to UIS. In this article, these failure mechanisms are labelled as either *active* or *passive*. The first, or active mode, results when the avalanche current forces the parasitic bipolar transistor into conduction. The second, or passive mode, results when the instantaneous chip temperature reaches a critical value.[1] At this elevated temperature, a "mesoplasma"* forms within the parasitic npn bipolar transistor and causes catastrophic thermal runaway. In either case, the MOSFET is destroyed. The passive mechanism is, therefore, identified as that failure mode not directly attributed to avalanche currents.

Symbols and Definitions

Whenever possible, symbols and definitions established by the JEDEC Committee, JC-25, are used in this article. To clear up any discrepancies, however, the following list describes symbols used frequently in this article.

I_O	the peak current reached during avalanche
t_{AV}	the time duration of the avalanche phenomenon
L	the value of inductance
$V_{(BR)eff}$	the breakdown voltage in avalanche

What is Unclamped Inductive Switching?

Whenever current through an inductance is quickly turned off, the magnetic field induces a counter electromagnetic force (EMF) that can build up surprisingly high potentials across the switch. Mechanical switches often have spark-suppression circuits to reduce these harmful effects that result when current is suddenly interrupted. However, when transistors are used as the switches, the full buildup of this induced potential may far exceed the rated breakdown ($V_{(BR)DSS}$) of the transistor, thus resulting in catastrophic failure.

If we know the size of the inductor, the amount of current being switched, and the speed of the switch, the expected potential may be easily calculated as

$$V = L\,di/dt + V_{DD} \quad (1)$$

where

L = the inductance (H)

di/dt = rate of change of current (A/s)

V_{DD} = the supply voltage (V)

* A "mesoplasma," according to Ghandhi, takes the form of a glowing red spot having an average temperature in excess of 650°C and a peak core temperature in excess of 1000°C. This mesoplasma is a result of regenerative thermal runaway.

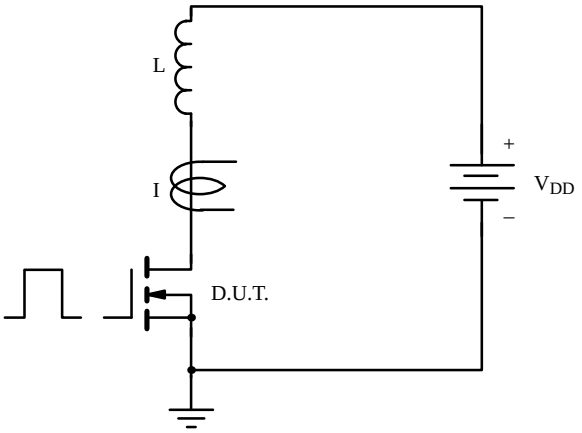

Figure 1. UIS Test Circuit

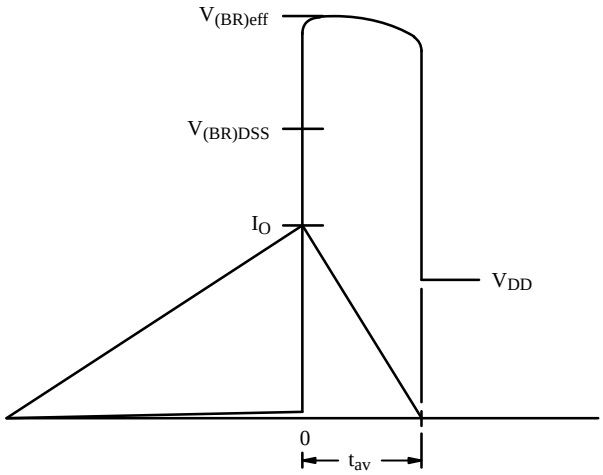

Figure 2. UIS Waveform during Switching

The classic UIS test circuit in widespread use* is shown in Figure 1. Using this circuit, the energy absorbed by the power MOSFET may be calculated using

$$E = 1/2\ I_O^2 L \left[\frac{V_{(BR)\,eff}}{V_{(BR)\,eff} - V_{DD}} \right] \qquad (2)$$

An alternate circuit removes V_{DD} (i.e., $V_{DD} = 0$) just prior to switching the device off, thus eliminating the last term in equation (2).

Reviewing the switching waveform shown in Figure 2, the gate remains on long enough to ramp the current to I_O, at which time the gate switches off, resulting in an abrupt break in the drain current. Since the magnetic field of the inductor cannot instantaneously collapse, a voltage is induced on the drain of the MOSFET in accordance with equation (1). This induced potential may easily exceed the (avalanche) breakdown voltage shown on the data sheet.** During avalanche, the voltage is clamped at a value of $V_{(BR)eff}$, and the current stored in the inductor decays linearly from I_O to zero. This decay time may be determined by rearranging equation (1).

$$t_{AV} = \frac{L\ I_O}{V_{(BR)\,eff}} \qquad (3)$$

Theories Pertaining to Stress Failures

The Bipolar Excitation Effect — The "Active" Mode. The classic reason for failure when a MOSFET is stressed focuses on the activation and subsequent secondary breakdown of the parasitic bipolar transistor. The intrinsic diode of a DMOS FET is actually the collector-base junction of this parasitic transistor. Whether the stress is a form of dv/dt[2,3] or UIS, current cascading laterally through the p^+ region is considered responsible for transistor failure when the voltage drop, $I_O R_{p+}$, activates this bipolar transistor.[4,5,6] The accepted model representing this failure mode in the vertical MOSFET structure is offered in Figure 3.

The initial avalanche current at breakdown is heavily concentrated within the MOSFET's inherent Zener diode (afforded by the deep p^+ well situated centrally in each cell, as shown in Figure 3). However, as the avalanche current continues to increase, it also spreads across the p/n barrier. The lateral resistance (R_p) is much greater than the "vertical" resistance (R_B) of the heavily-doped p^+ region. Avalanche current concentrated in the p^+ (Zener) region does not normally initiate bipolar action. As the avalanche current increases in intensity, it spreads along the p/n barrier, and the scenario follows the classic reasoning. If the avalanche currents cascading laterally through the p-doped region (pseudobase region) develop sufficient forward bias across R_p to offset V_{BE}, the normal forward base current, $+I_B$, in conjunction with the beta of the parasitic npn bipolar transistor, will result in a local

* Recommended by JEDEC Committee JC–25.

** Avalanche breakdown, $V_{(BR)DSS}$, offered in the typical data sheet is generally rated at the zero gate voltage drain current (I_{DSS}) of the MOSFET. Avalanche breakdown during UIS ($V_{(BR)eff}$) is, as shown in Figure 2, at substantially higher drain currents. $V_{(BR)eff}$ is much greater than $V_{(BR)DSS}$.

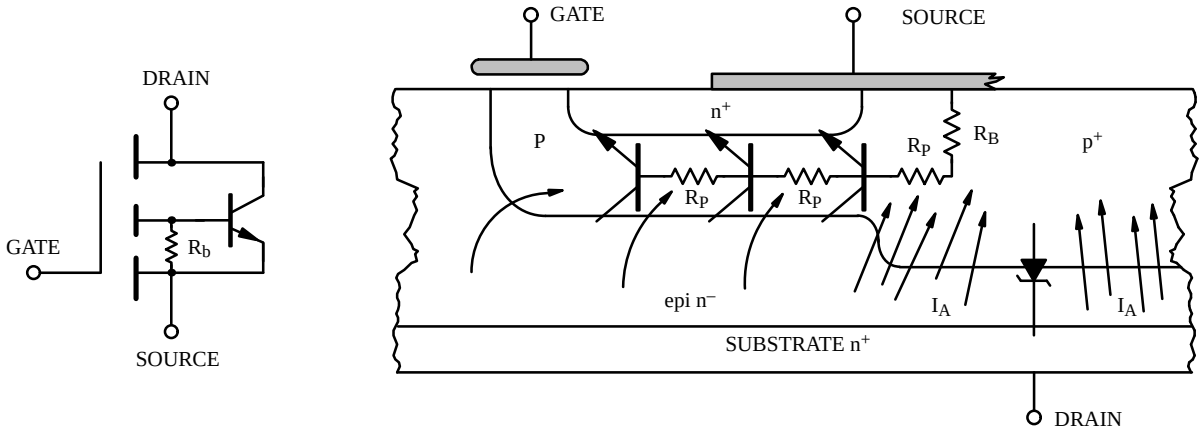

Figure 3. Equivalent Circuit and Cross Section

breakdown voltage equal to BV_{CEO} (which is approximately half of $V_{(BR)DSS}$). The resulting mesoplasma causes thermal runaway and the destruction of the power MOSFET.

Examination of Figure 3 suggests that the current necessary to trigger this series of events might be closely approximated if both the V_{BE} of the parasitic npn bipolar transistor and R_p were known.[7] Test patterns available on the semiconductor wafer during manufacture make it possible to examine such parameters of the parasitic npn bipolar transistor. Measurement results of V_{BE}, beta, and $R_p{}^+$ from the test pattern are shown in Figure 4. Because of the deep p^+ diffusion that forms the Zener structure, the region beneath the n^+ diffusion — where R_p is critical—resembles a graded junction. This—in concert with the dramatic temperature rise that together reduces V_{BE}, raises R_p, and increases beta—com- complicates any effort to calculate the critical avalanche current required to excite the parasitic bipolar transistor. Blackburn[8] derived a worst-case calculation; however, the actual performance is substantially better than predicted due to second-order effects.

Today's MOSPOWER devices can safely withstand over two times the 25°C rated current even at junction temperatures approaching 150°C. The "active" form of failure is no longer the prevalent mode under normal operating conditions. The limiting mechanism is now usually a thermal failure caused by the large temperature increase during avalanche.

The Thermal Effect — The "Passive" Mode. During UIS, as the MOSFET is subjected to increasing energy, the internal chip temperature rises dramatically (equation 4) and is thought to generate a mesoplasma. Such mesoplasmas (regenerative heating) lead to the irreversible damage generally associated with thermal runaway.[1] * The swiftness of this temperature rise, see equation (3), tends to make heat sinks irrelevant for UIS testing.

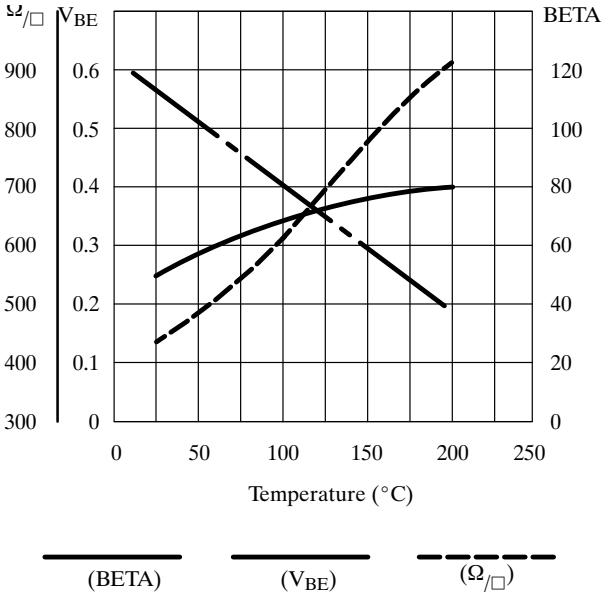

Figure 4. Parasitic Bipolar Transistor Characteristics

* The increasing temperature during mesoplasma formation results in a decreasing thermal conductivity of silicon (see Figure 5a) which, in turn, results in a further increase in the localized temperature. Thermal runaway is thus encouraged.

During this avalanche period, as defined by equation (3), energy is dissipated in the device equation (2), resulting in a dramatic increase in chip temperature. Blackburn[8]

derived the following one-dimensional thermal model to calculate the maximum temperature rise, ΔT_M.

$$\Delta T_M = \frac{\sqrt{2}}{3} P_o K \sqrt{t_{AV}} \quad (4)$$

where

$$K = \frac{2}{A\sqrt{(r \pi k c)}} = 2\sqrt{\frac{R}{\pi C}}$$

$$P_o = I_O V_{(BR)eff}$$

DT_M = maximum instantaneous temperature rise (_C)

and

A = the active chip area (where heat originates)

ϱ = the density of silicon

k = the thermal conductivity (very temperature dependent (see Figure 5a)

c = the specific heat of silicon (also temperature dependent (see Figure 5b)

R = effective thermal resistance of chip (°C/W)

C = effective thermal capacitance of chip (J/°C)

Equation (4) can be further manipulated to relate the temperature rise, ΔT_M, to

$$\Delta T_M = \frac{\sqrt{2}}{3} K\, l_o V_{(BR)eff} \sqrt{\frac{L l_o}{V_{(BR)eff}}} \quad (5)$$

Although $V_{(BR)eff}$ is temperature sensitive, for simplicity we assume it is a constant. Therefore,

$$\Delta T_M \alpha\ l_o \sqrt{L\ l_o} \quad (6)$$

or

$$\Delta T_M \alpha\ l_o^{3/2} \sqrt{L} \quad (7)$$

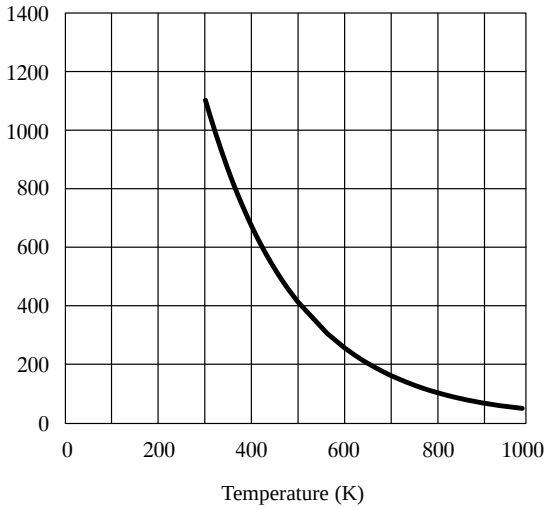

Figure 5a. Conductivity of Silicon vs. Temperature ([Physics Review, Vol. 130 (6/'63)] (Ω/cm_)

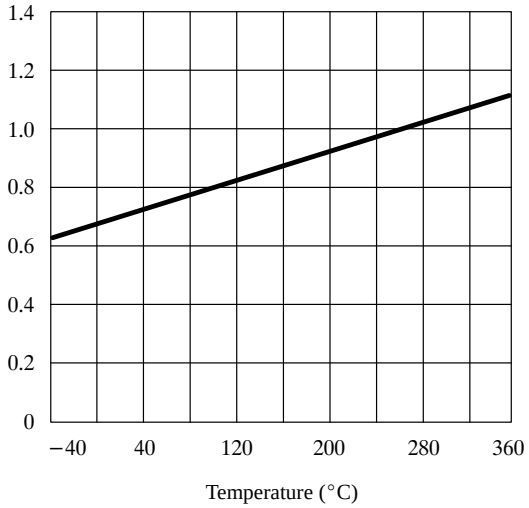

Figure 5b. Specific Heat of Silicon vs. Temperature (Ω sec/gm_)

If we assume L is constant, equation (7) is further reduced to

$$\Delta T_M \alpha\ l_o^{3/2} \quad (8)$$

which further identifies that

$$\Delta T_M \alpha\ E^{3/4} \quad (9)$$

If the parasitic bipolar transistor is *not* excited, equation (9) relates the peak temperature rise to the avalanche energy dissipation. This temperature rise then becomes the cause of the other failure mode referred to as "passive."

Test Results

The Siliconix avalanche-rated SMP30N10 is one of a family of dense-cell MOSPOWER FETs. Cell density for this family is 1.6M/in.^{2} (248K/cm^2). The overall chip area is 0.17 cm^2.

UIS avalanche breakdown was examined at a variety of inductance values (0.01 to 10 mH) at starting temperatures from ambient (25°C) to 150°C in 25°C increments. A sample size of 20 pieces for each inductance and at each temperature involved over 760 MOSFETs. All MOSFETs were from the same wafer lot.

The test method used the alternate circuit which removed V_{DD} immediately prior to switching. The equipment used, a ITC UIS Tester,* Model 5510E, allowed an increase of current, I_O, in 0.1-A increments to 26 A and thereafter in 1.0-A increments. A fixed gate-drive impedance of 25 Ω drove the device under test. A temperature-controlled heater was used to sink the power MOSFET (mounted in the TO-220 package) to provide a precise starting temperature throughout the UIS tests.

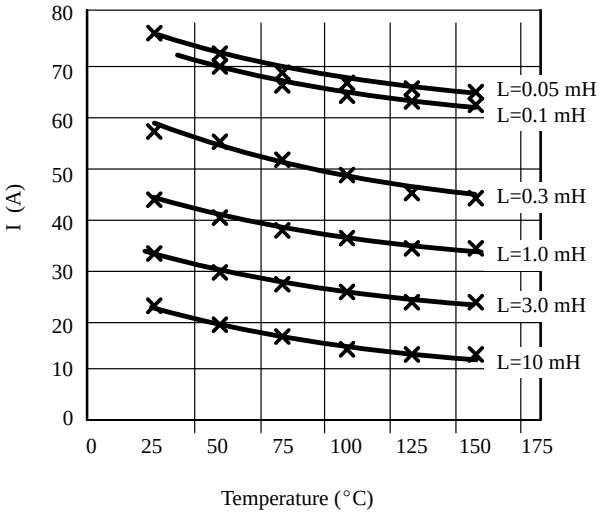

Figure 6. Avalanche Failure Current vs. Starting Temperature for the SMP30N10

Figure 6 shows avalanche current versus starting temperature for six values of inductance, ranging from 0.05 to 10 mH. These data represent single-event UIS failures and further identify that the device ratings, in particular the "absolute maximum ratings" of I_{AR} and T_J, are conservative. For any given inductance, the avalanche failure current decreased as the starting temperature increased, although not as dramatically nor with the tight convergence described by Stoltenburg.[4] Since Figure 6 represents the culmination of incremental increases in avalanche current, these data conclusively show that if Siliconix avalanche-rated power MOSFETs are operated within data sheet limits, they can enter into avalanche without fear of failure. Furthermore, these data tend to confirm that absolute maximum ratings are not so absolute as once thought. At the 150°C starting temperature and switching 32 A (at 1 mH), the calculated chip temperature, see equation (4), is 322°C!

The typical 2.2 mV/°C decay of V_{BE} and the increasing resistance of the p-doped region with increasing temperature suggests that the parasitic npn bipolar transistor becomes more susceptible to turn-on with increasing temperature. Although a rapid fall-off of avalanche current at higher temperatures might be anticipated because of this increased susceptibility, Figure 6 shows a reasonably slow decline. This behavior is attributed to the slow lateral spreading of the current along the p/n junction as the avalanche current increases. The dense cell design diminishes lateral spreading of avalanche current beyond the heavily doped p+ (Zener) region and, thus, enables more avalanche current than MOSFETs with less dense cell structures.

The measured data (see Figure 6) may be manipulated, with the help of equation (2), to identify interesting details of UIS phenomenon. Figure 7 plots avalanche failure current versus inductance across a temperature range from ambient to 150°C.

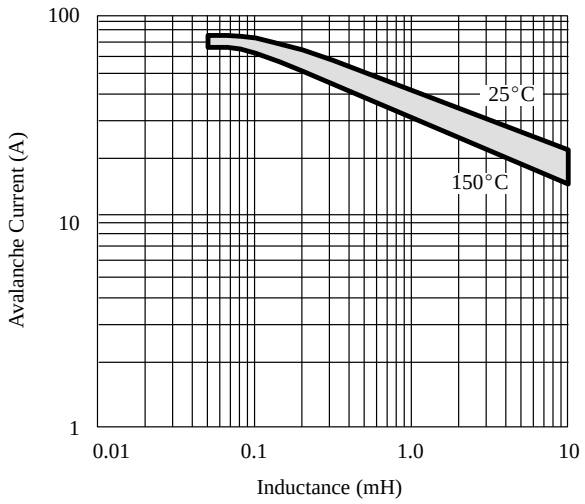

Figure 7. Avalanche Failure Current vs. Inductance for the SMP30N10

*Integrated Technology Corporation, 1228 N. Stadem Drive, Tempe, Arizona 85281

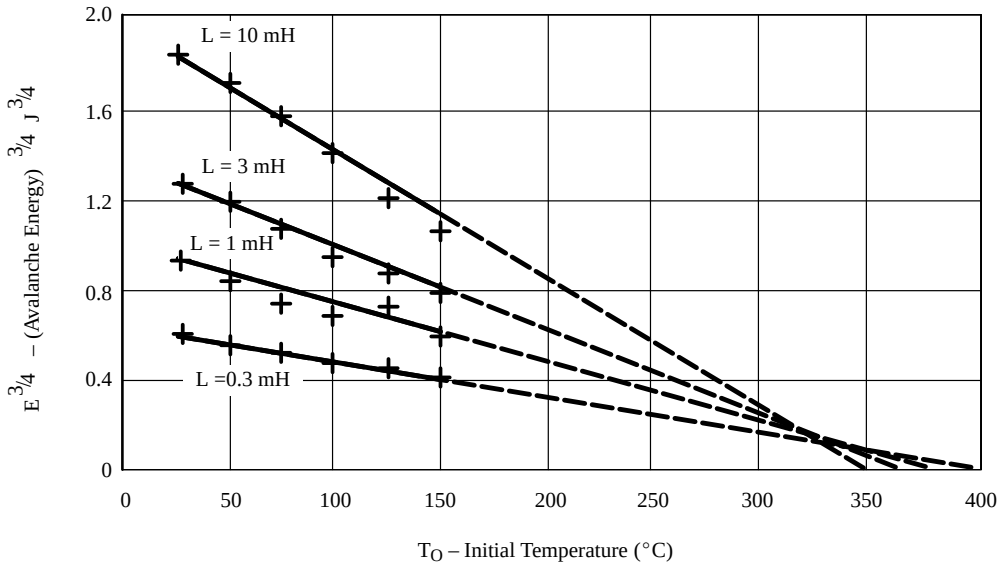

Figure 8. (Avalanche Energy)$^{3/4}$ vs. Starting Temperature for the SMP30N10

As shown in Figure 8, avalanche energy raised to the 3/4 power, representing equation (9), was plotted against the starting temperature. The x-axis intercepts are centered around 375°C. This, combined with the extraplation of V_{BE} vs. temperature (Figure 4) appears to identify a maximum instantaneous chip temperature beyond which a heavily-doped (low on-resistance) silicon power MOSFET cannot go!

Equation (4) suggests that the increase in temperature varies with the square root of the time in avalanche, t_{AV}. Plotting the actual results showed that temperature rise in practice varied with $^{2.2}\sqrt{t_{AV}}$, a relationship confirmed by Stoltenburg.[4] This deviation is probably due to multidimensional heat spreading and gives a slightly modified version of equation (4):

$$\Delta T_M = \frac{\sqrt{2}}{3} P_o K \, ^{2.2}\sqrt{t_{AV}} \qquad (10)$$

An Explanation for UIS Failure

A common misconception is that the absolute maximum temperature excursion for silicon transistors must be limited to 150°C. Although undoubtedly a good design rule, instantaneous chip temperatures can—and do— rise to appreciably higher levels under certain stressful environments. No detrimental effects were observed in the surviving power MOSFETs because of this swift temperature excursion.

The data confirms two failure modes: active (bipolar) and passive (thermal).

Low inductances provide little energy (equation (2) and Figure 9) to dissipate within the MOSFET chip, thus limiting the instantaneous temperature excursion. The higher avalanche currents associated with these low inductances tend to cascade laterally through the p-doped region of the MOSFET, increasing the probability of bipolar action from $I_A R_p$ excitation. This “active” failure occurs at currents much higher than the *rated* current of 30 A, proving the ruggedness of the cell structure used to manufacture the Siliconix SMP30N10.

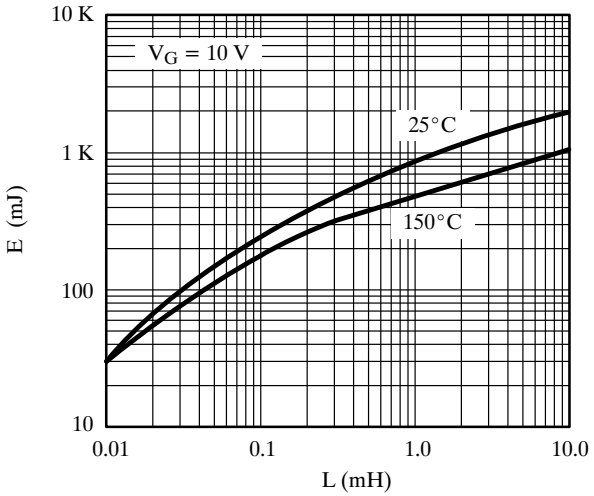

Figure 9. Avalanche Energy vs. Inductancefor the SMP30N10

At high inductances (i.e., at high energy levels), the extended decay time for the avalanche current dramatically raises the chip temperature. The silicon reaches its critical/intrinsic temperature, resulting in a mesoplasma and thermal runaway.

As mentioned earlier, Ghandhi[1] attributes secondary breakdown of bipolar transistors to mesoplasma formations at localized regions on the semiconductor, which in turn, will lead to thermal runaway. The data tends to confirm a critical temperature at which MOSFETs can no longer withstand avalanche current. For example, the 100-V, avalanche-rated Siliconix SMP30N10 exhibits a nominal epi doping of approximately 2.5 x 10^{15} a/cm^3, and the theoretical intrinsic temperature is $\sim$ 360°C,[1] which is believed to be close to the critical temperature. For power MOSFETs, it appears that the critical and intrinsic temperatures are synonymous. Above this critical/intrinsic temperature, current increases rapidly, forming a localized hot spot that quickly becomes a destructive mesoplasma.

Rating Power MOSFETs for Ruggedness

Most manufacturers of power MOSFETs rate avalanche current equal to the maximum drain current specification of the particular device. This is somewhat misleading since avalanche current does not pass through the gate-enhanced channel as does the drain current. As shown in this paper and as the name implies, it is an avalanche condition that completely bypasses the channel and is more a function of the junction area and quality of the p/n (Zener) diode[9] that bridges the MOSFET.

There is, however, some rationale for rating the avalanche current of power MOSFETs equal to the maximum drain current. During UIS breakdown, the avalanche current will never exceed the operating drain current; it will only decay from this point (see Figure 2). A reasonable approach to ensure MOSFET reliability would be to collectively identify 1) a safe avalanche current, 2) an operating junction temperature, and 3) a value of inductance.

For thermal (passive) failures, the data suggests that to ensure safe operation, the data sheet need only give the constants for use in equation (10) (or a graphical plot of it) and a maximum avalanche junction temperature.The user could then verify if the device is in the safe operating area under any conditions. Figure 10 graphically shows the temperature rise, calculated using equation (10) for devices taken to failure. The tight grouping and linear relationship proves the validity of this form of rating.

Avalanche energy ratings alone do not provide sufficient information to ensure against catastrophic failures because time in avalanche is also important. Furthermore, it is easily derived from the critical parameters of avalanche current and inductance, see equation (2). Consequently, it does not need to be specified on the data sheet.

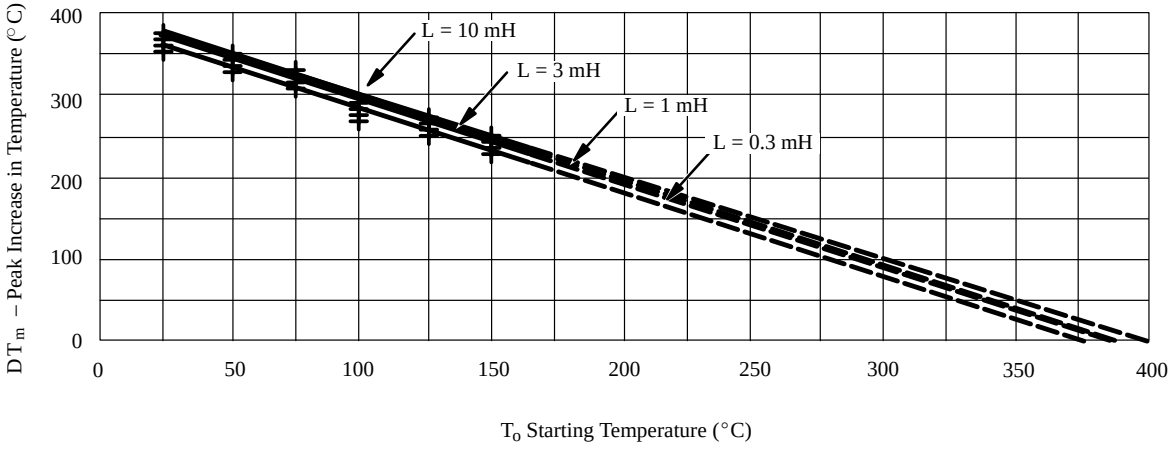

Figure 10. Temperature Increase vs. Starting Temperatures

References

1. Sorab K. Ghandhi, *Semiconductor Power Devices* (Wiley-Interscience: New York, 1977).

2. Edwin S. Oxner, "Static and Dynamic dV/dt Characteristics of Power MOSFETs," *PCI Proceedings*, 132–42, Atlantic City (1984).

3. D. S. Kuo, C. Hu, and M. H. Chi, "dV/dt Breakdown in Power MOSFETs," *IEEE Electron Device Letters*, EDL–4, No. 1 (Jan. 1983).

4. Rodney R. Stoltenburg, "Boundary of Power MOSFET Unclamped Inductive Switching (UIS), Avalanche-Current Capability," *IEEE Applied Power Electronics Conference Proceedings*, 359–64, (Mar. 1989).

5. David L. Blackburn, "Turn-off Failure of Power MOSFETs," *IEEE Power Electronics Specialists Conference*, 429–35 (June 1985).

6. John W. Worman, "Using Power MOSFETs in Unclamped Inductive Switching Applications," *Powertechnics* (Oct. 1988).

7. Chenming Hu and Min-Hwa Chi, "Second Breakdown of Vertical Power MOSFETs", *IEEE Transactions on Electron Devices*, ED–29, 1287–93 (Aug. 1988).

8. David L. Blackburn, "Power MOSFET Failure Revisited," IEEE Power Electronics Specialists Conference, Kyoto, Japan (Apr. 1988).

9. Alford L. Ward, "Calculations of Second Breakdown in Silicon Diodes," U.S. Army ERDC Harry Diamond Laboratories, HDL–TR–1978 (Aug. 1982).