

## JFET Biasing Techniques

### Introduction

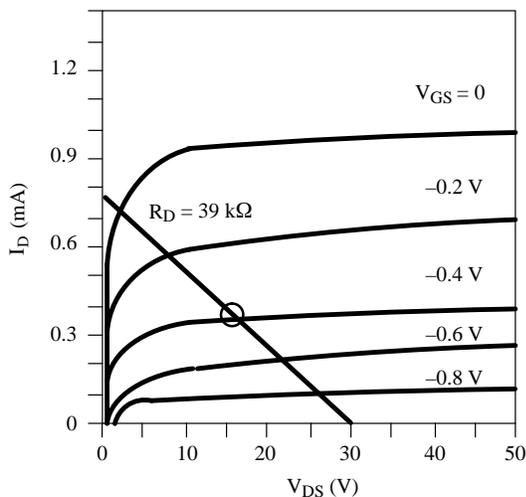
Engineers who are not familiar with proper biasing methods often design FET amplifiers that are unnecessarily sensitive to device characteristics.

One way to obtain consistent circuit performance, in spite of device variations, is to use a combination of constant voltage and self biasing. The combined circuit configuration turns out to be the same as that generally used with bipolar transistors, but its operation and design are quite different.

### Three Basic Circuits

Let's examine three basic common-source circuits that can be used to establish a FET's operating point (Q-point) and then see how two of them can be combined to provide greatly improved performance. The three basic biasing schemes are:

- Constant-voltage bias, which is most useful for RF and video amplifiers employing small dc drain resistors.
- Constant-current bias, which is best suited to low-drift dc amplifier applications such as source followers and source-coupled differential pairs.



**Figure 1.** Output Characteristic Curve—A large dynamic range is provided by the operating point at  $V_{DSQ} = 15\text{ V}$ ,  $I_{DQ} = 0.4\text{ mA}$ , and  $V_{GSQ} = -0.4\text{ V}$ .

- Self bias (also called source bias or automatic bias), which is a somewhat universal scheme particularly valuable for ac amplifiers.

The Q-point established by the intersection of the load line and the  $V_{GS} = -0.4\text{ V}$  output characteristic of Figure 1 provides a convenient starting point for the circuit comparison. The load line shows that a drain supply voltage,  $V_{DD}$ , of 30 V and a drain resistance,  $R_D$ , of 39 kΩ are being used.

The quiescent drain-to-source voltage,  $V_{DSQ}$ , is 16 V, allowing large signal excursions at the drain. Maximum input signal variations of  $\pm 0.2\text{ V}$  will produce output voltage swings of  $\pm 7.0\text{ V}$ , and a voltage gain of 35 where:

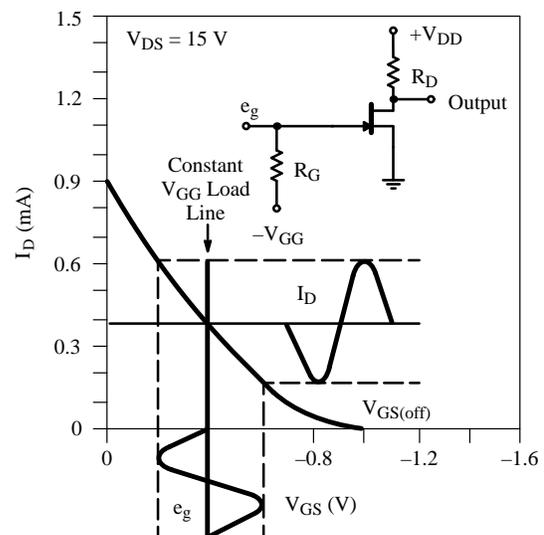
$$A_V = \frac{g_{fs} R_D}{1 + R_D g_{os}}, \quad g_{os} = \text{JFET output conductance} \quad (1)$$

In most applications,  $R_D g_{os}$  is negligible, therefore:

$$A_V \approx g_{fs} R_D \quad (2)$$

### Constant-Voltage Bias

The constant-voltage bias circuit (Figure 2) is analyzed by superimposing a line for  $V_{GG} = \text{constant}$  on the transfer characteristic of the FET (2N4339 typical device).



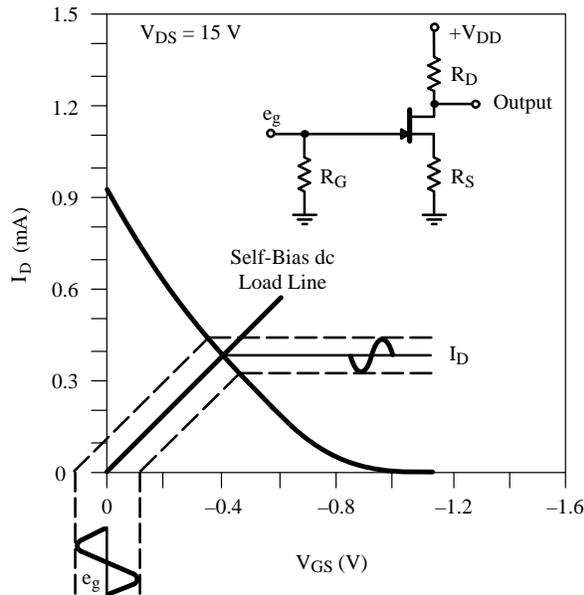
**Figure 2.** Transfer Curve—Constant-voltage bias is maintained by the  $V_{GG}$  supply as shown on this typical transfer curve. Input signal  $e_g$  moves the load line horizontally.



## Self-Bias Needs No Extra Supply

The self-bias circuit (Figure 5) establishes the Q-point by applying the voltage dropped across the source resistor,  $R_S$ , to the gate. Since no voltage is dropped across  $R_S$  when  $I_D = 0$ , the self-bias load line passes through the origin. Its slope is given by  $-1/R_S = I_{DQ}/V_{GSQ}$ .

The circuit is biased automatically at the desired Q-point, requiring no extra power supply, and providing a degree of current stabilization not possible with constant-voltage biasing.



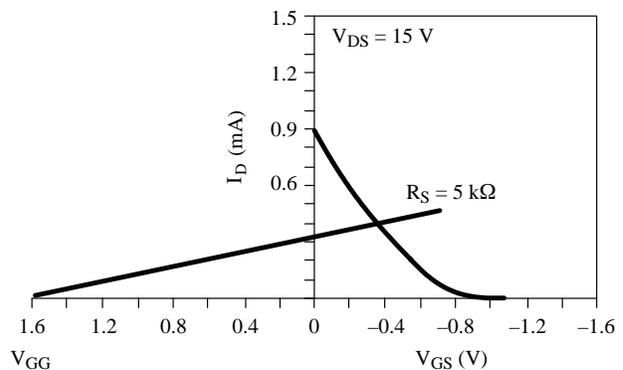
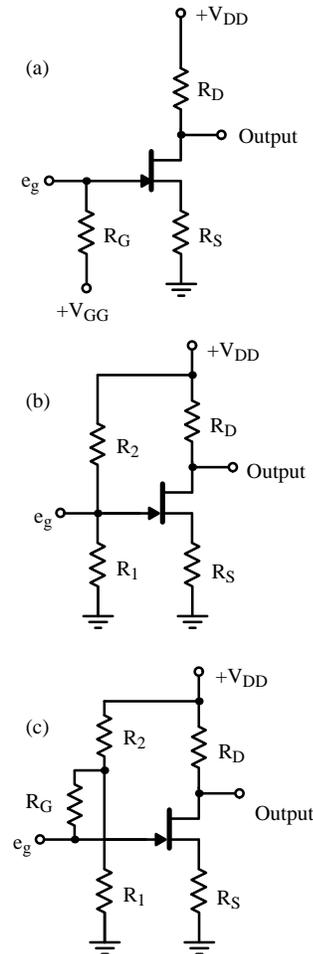
**Figure 5.** The self-bias load line passes through the origin with a slope  $-1/R_S$ . Bypassing  $R_S$  will steepen the slope and increase the gain of the circuit.

## Combo Constant-Current/Self-Biasing

A fourth biasing method, combining the advantages of constant-current biasing and self biasing, is obtained by combining the constant-voltage circuit with the self-bias circuit (Figure 6). A principal advantage of this configuration is that an approximation may be made to constant-current bias without any additional power supply. The bias load line may be drawn through the selected Q-point and given any desired slope by properly choosing  $V_{GG}$ . (The bias line intercepts the  $V_{GS}$  axis at  $V_{GG}$ .) The larger  $V_{GG}$  is made, the larger  $R_S$  will be and the better will be the approximation to constant-current biasing.

All three circuits in Figure 6 are equivalent. Circuit 6a requires an extra power supply. The need for an additional

supply is avoided in 6b by deriving  $V_{GG}$  from the drain supply.  $R_1$  and  $R_2$  are simply a voltage divider. To maintain the high input impedance of the FET,  $R_1$  and  $R_2$  must both be very large.



**Figure 6.** All three combination-bias circuits are equivalent. They add constant-voltage biasing to the self-bias circuit to establish a reasonably flat load line without sacrificing dynamic range.

Very large resistors cannot always be found in the exact ratio needed to derive the desired  $V_{GG}$  in every circuit application. Circuit 6c overcomes this problem by placing a large  $R_G$  between the center point of the divider and the gate. This allows  $R_1$  and  $R_2$  to be small, without lowering the input impedance.

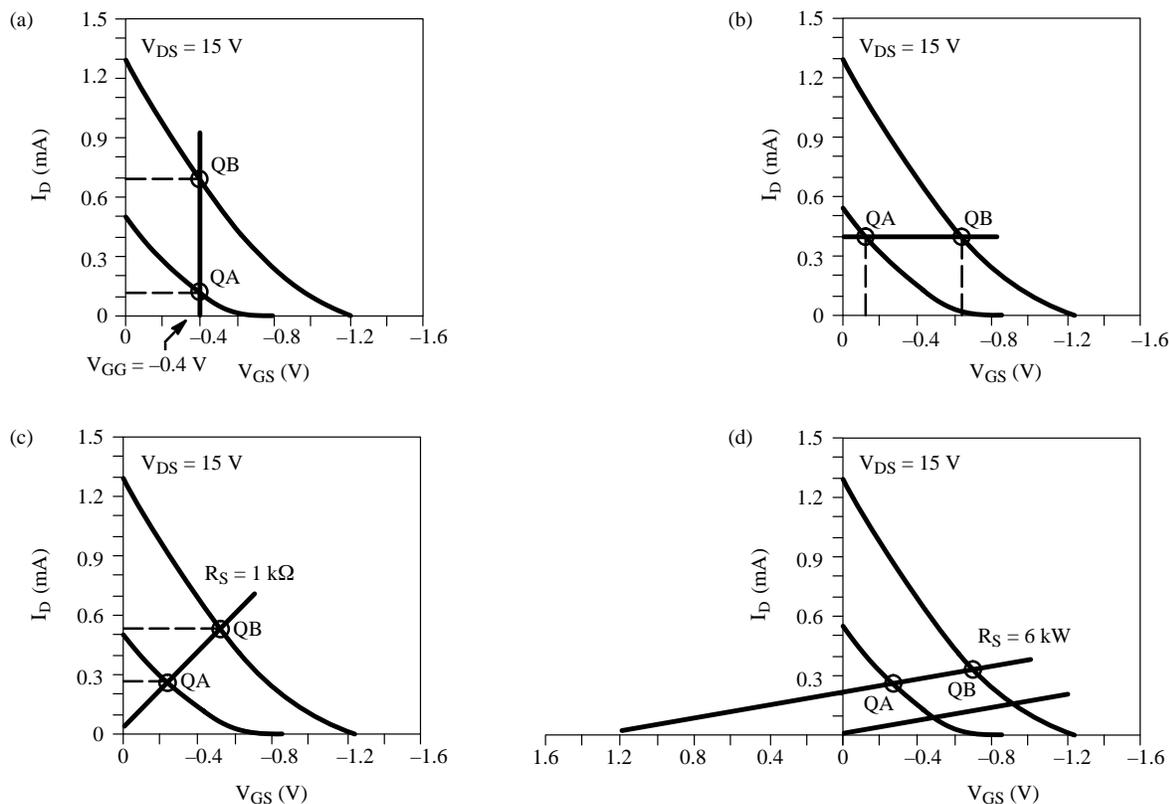
One point of caution is that as  $V_{GG}$  is increased,  $V_S$  increases, and  $V_{DS}$  decreases. Therefore, with low  $V_{DD}$ , there may be a significant decrease in the allowable output voltage swing.

## Biasing for Device Variations

The value of the combination-bias technique becomes apparent when one considers the normal production spread of device characteristics. The problem is illustrated in Figure 7 where the lower and higher ranges of the 2N4339 devices are shown. The two curves illustrate the operating current variations using various types of biasing in a normal production lot. Other devices with even wider min/max  $I_{DSS}$  limits will show wider variations.

Attempting to establish suitable constant-voltage bias conditions for a production spread of devices is practical only for circuits with very small values of dc drain resistance—for example, circuits with inductive loads. As the constant-voltage bias plot of Figure 7a reveals, constant gate bias causes a significant difference in operating  $I_{DQ}$  for the extreme limit devices. At  $V_{GS} = -0.4$  V, the range of  $I_{DQ}$  is 0.13 to 0.69 mA, and  $V_{GSQ}$  for a given  $R_D$  will vary greatly for most resistance-loaded circuits. For the example of Figure 1, with  $R_D = 39$  k $\Omega$  and  $V_{DD} = 30$  V,  $V_{GSQ}$  varies from near saturation (5 V) to 25 V.

An excellent method of biasing is the constant-current method of Figure 3. Biasing in this manner fixes the operating drain current for all devices and sets  $V_{DSQ}$  to  $V_{DD} - I_{DQ}R_L$  for any device in the production spread.  $V_{GS}$  automatically finds a value to set the appropriate  $I_{DQ} = \text{constant}$  for all devices. For the constant-current bias plot of Figure 7b, with  $I_{DQ} = 0.4$  mA,  $V_{GS}$  would range from  $-0.11$  to  $-0.67$  V.



**Figure 7.** Transfer Characteristic Curves—2N4339: The advantages of combination biasing, when one is working with a spread of device characteristics, are made obvious by plotting the load lines for the various types of biasing on a pair of limiting transfer curves.

Output characteristics are not needed as long as  $I_{DQ}$  is chosen to be below the minimum  $I_{DSS}$ . With  $R_D = 39\text{ k}\Omega$  and  $V_{DD} = 30\text{ V}$ ,  $V_{DSQ}$  is 14.8 V for all devices.

The disadvantages of the constant-current method are that it allows no signal to be developed unless the current source is bypassed and, as we shall see, it lacks the flexibility to provide constant gain despite variations in the forward transconductance,  $g_{fs}$ , of the devices.

The self-bias scheme is a reasonable choice for single-ended dc amplifiers and for ac amplifiers. In unbypassed or dc circuits, some compromise must be made between the gain loss due to current feedback degeneration and the advantage of current stabilization achieved with high  $R_S$ .

An appropriate choice of  $I_{DQ}$  limits can be made by using the pair of limiting transfer curves. For example, for  $R_S = 1\text{ k}\Omega$ , the load line shown on the self-bias curve of Figure 7c is established. The maximum  $I_D$  is 0.52 mA, and the minimum  $I_D$  is 0.24 mA. The operating range of  $V_{DSQ}$  may be calculated for any value of  $V_{DD}$  and  $R_D$ . Clearly, for  $R_D = 39\text{ k}\Omega$ , the maximum-limit device (device B) would operate with  $V_{DSQ} = 9.8\text{ V}$  and the minimum-limit device (device A) would operate with  $V_{DSQ} = 20.6\text{ V}$ . This results in satisfactory operation for all devices. However, such a variation in  $I_{DQ}$  imposes severe limitations on the circuit design.

A better approach is illustrated by the combination-bias curve of Figure 7d with  $V_{GG} = 1.2\text{ V}$ . The range of  $I_{DQ}$  for the bias condition is 0.25 mA to 0.32 mA.

A similar minimum difference in  $I_{DQ}$  could be achieved with  $R_S = 6\text{ k}\Omega$  and  $V_{GG} = 0$  (a self-bias condition) but the operating points would be pushed toward the toe of the transfer characteristics and allowable signal input would be reduced.

The combination circuit (Figure 7d) allows almost ideal operation over the full production spread of devices. Even with  $R_D = 6\text{ k}\Omega$ , the  $V_{DSQ}$  would range only between 10 and 15 V.

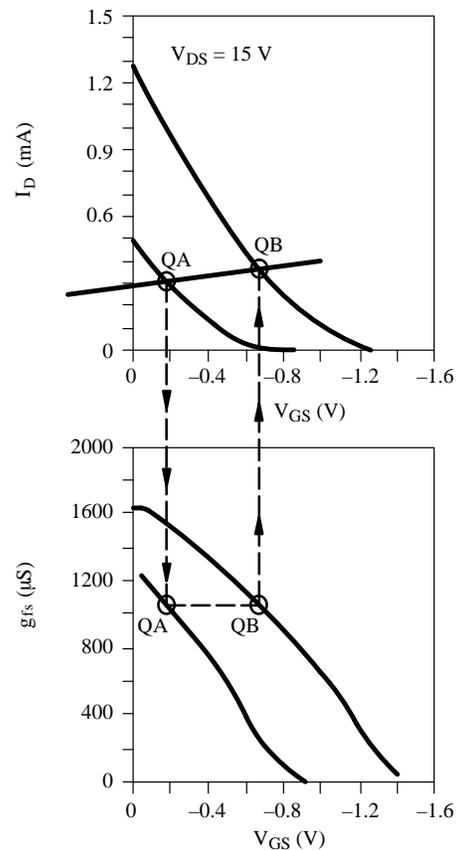
For the combination circuit,  $R_D$  should be chosen to allow the largest output signal swing for  $I_{DQ}$  midway between the two extremes of 0.25 and 0.32 mA; namely 0.285 mA. Setting the voltage drop across  $R_D$  at one-half of  $(V_{DD} - 2V_{GS(off)typ})$  or 14 V,  $(30-2)^{1/2}$  yields  $R_D = (14\text{ V}/0.285\text{ mA}) = 49\text{ k}\Omega$

Figure 10 shows the effect of temperature variation on the transfer characteristics from 25 to 125°C. The opposite change occurs from 25 to -55°C. The temperature effect is generally far less than the device-to-device variation.

## Minimize The Gain Variations

Leaving  $R_S$  unbypassed helps reduce gain variations from device to device by providing degenerative current feedback. However, this method for minimizing gain variations is only effective when a substantial amount of gain is sacrificed.

A better approach is to use the combination-bias technique with the bias point selected from the transfer and transconductance curves (Figure 8).



**Figure 8.** Gain variations are minimized when the load line is designed to intersect the pair of limiting transfer curves (top) at points of equal  $g_{fs}$  (bottom).

As Figure 8 shows, it is possible to find an  $R_S$  and a  $V_{GG}$  that will set  $I_{DQA}$  and  $I_{DQB}$  to values such that  $g_{fsQ}$  will be the same for both devices. The  $g_{fsQ}$  of all intermediate devices will be approximately equal to the limiting values. Thus, a constant, or nearly constant, stage gain is obtained even with a bypass capacitor.

The design procedure is as follows:

- Step 1.* Select a desired  $I_{DQA}$  below  $I_{DSSA}$ . A good value, allowing for temperature variations, is 60% of  $I_{DSSA}$ . This will allow for decreasing  $I_{DSS}$  due to temperature variation and for reasonable signal excursions in load current.
- Step 2.* Enter the transfer curves at  $I_{DQA} \sim 0.6 I_{DSSA}$  (0.3 mA) to find  $V_{GSQA}$ . Thus  $V_{GSQA} \sim -0.2$ .
- Step 3.* Drop vertically at  $V_{GSQA}$  to the minimum limit transconductance curve to find  $g_{fsQA}$ . The value as read from the plot is approximately 1000  $\mu S$ .
- Step 4.* Travel across the  $g_{fs}$  plot to the maximum curve to find  $V_{GSQB}$  at the same value of  $g_{fs}$ . This is  $V_{GSQB} \sim -0.7$  V.
- Step 5.* Travel vertically up to the maximum limit transfer curve to find  $I_{DQB}$  at  $V_{GSQB}$ . This is  $I_{DQB} \sim 0.36$  mA.
- Step 6.* Construct an  $R_S$  bias line through points QA and QB on the transfer curves. The slope of the line is  $1/R_S$ , and the intercept with the  $V_{GS}$  axis is the required  $V_{GG}$ .

As Figure 8 demonstrates, it may be somewhat inconvenient to perform Step 6 graphically. An algebraic solution can be employed instead. The source resistance is given by

$$R_S = (V_{GSQA} - V_{GSQB}) / (I_{DQB} - I_{DQA}) \quad (4)$$

and the bias voltage is

$$V_{GG} = R_S I_{DQB} + V_{GSQB} \quad (5)$$

Care should be taken to maintain the proper algebraic signs in Equations 4 and 5. For n-channel FETs,  $V_{GS}$  is negative and  $I_D$  is positive. For p-channel units, the signs are reversed.

If the transconductance curves of Figure 8 are not available,  $g_{fs}$  can be determined simply by measuring the slope of the transfer curve at the desired operating point.

Just place a straight-edge tangent to the curve at the Q-point and note the points at which it intercepts the  $I_D$  and  $V_{GS}$  axes. The slope and  $g_{fs}$  are given by:

$$\text{slope} = g_{fs} = I_{D(\text{intercept})} / -V_{GS(\text{intercept})} \quad (6)$$

In designing a constant-gain circuit, simply set the straight-edge tangent to the transfer curve of device A at point QA and slide it, without changing its slope, until it is tangent to the curve of device B. The tangent point is QB.

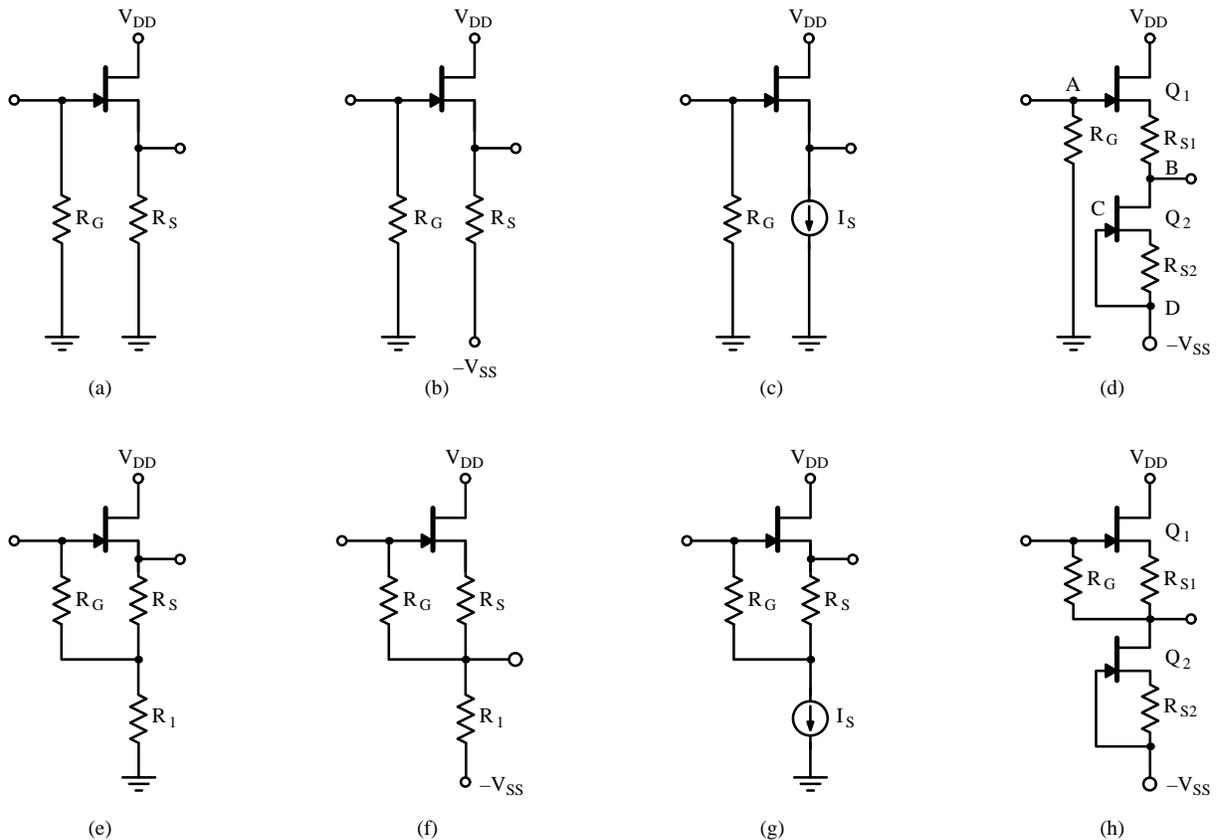
## FET Source-Follower Circuits

The common-drain amplifier, or source follower, is a particularly valuable configuration; its high input impedance and low output impedance make it very useful for impedance transformations between FETs and bipolar transistors. By considering eight circuits (Figure 9), which represent virtually every source-follower configuration, the designer can obtain consistent circuit performance despite wide device variations.

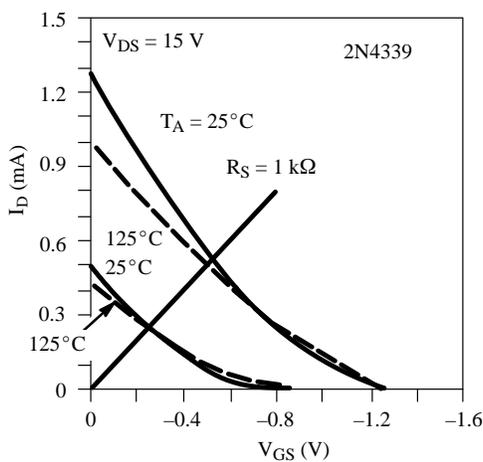
There are two basic connections for source followers: with and without gate feedback. Each connection comes in several variations. Circuits 9a through 9d have no gate feedback; their input impedances, therefore, are equal to  $R_G$ . Circuits 9e through 9h employ feedback to their gates to increase the input impedance above  $R_G$ .

Before getting into the details of bias-circuit design, several general observations can be made about the circuits of Figure 9:

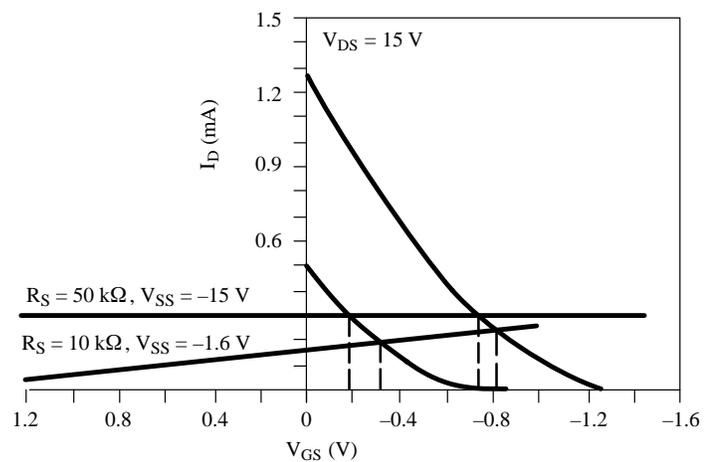
- Circuits a, c, e and g can accept only positive and small negative signals, because these circuits have their source resistors connected to ground. The other circuits can handle large positive and negative signals limited only by the available supply voltages and device breakdown voltage.
- Circuits c, d, g and h employ current sources to improve drain-current ( $I_D$ ) stability and increase gain.
- Circuits d and h employ JFETs as current sources.
- Circuits d, f and h employ a source resistor,  $R_S$ , which may be selected to set the quiescent output voltage equal to zero.
- Circuits d and h use matched FETs.  $R_S$  is selected to set  $I_D$ . The dc input-output offset voltage is zero.



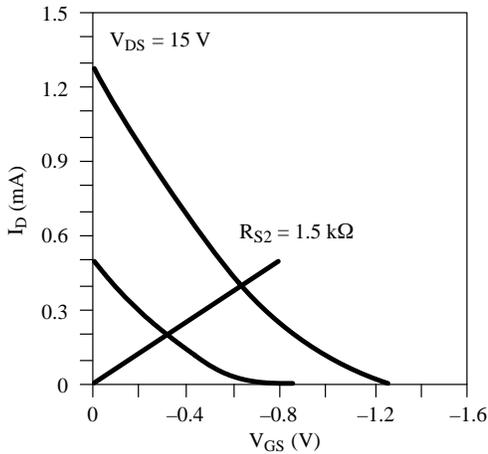
**Figure 9.** Virtually every practical source-follower configuration is represented in this collection of eight circuits. The configurations in the top row do not employ gate feedback; the corresponding configurations in the bottom row employ gate feedback.



**Figure 10.** Self-biasing (Figure 9a) uses the voltage dropped across the source resistor,  $R_S$  to bias the gate. The load line passes through the origin and has a slope of  $-1/R_S$ .



**Figure 11.** Adding a  $V_{SS}$  Supply to the self-bias circuit (Figure 9b) allows it to handle large negative signals. The load line's intercept with the  $V_{GS}$  axis is at  $V_{GS} = V_{SS}$ . Bias Lines are shown for  $V_{SS} = -15\text{ V}$  and  $V_{SS} = -1.6\text{ V}$ .



**Figure 12.** This load line is set by  $R_{S2}$  and  $Q_2$  which acts as a current source (Figure 9d). This source follower, therefore, exhibits zero or near-zero offset. If the FETs are matched at the operating  $I_D$ , the source follower will exhibit zero or near-zero temperature drift.

## Biasing Without Feedback Is Simple

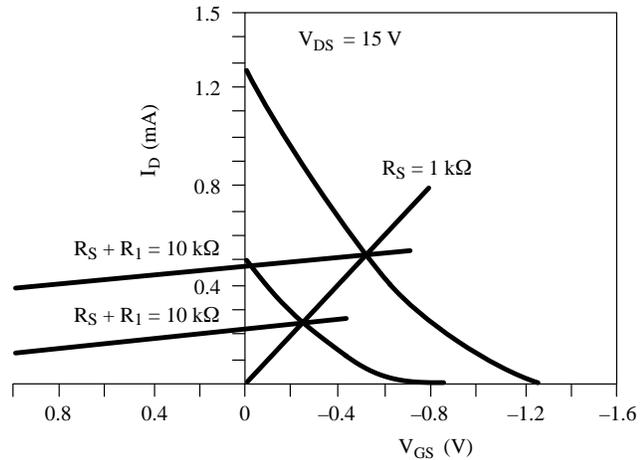
Circuit 9b is an example of source-resistor biasing with a  $-V_{SS}$  supply added. The advantage over circuit 9a is that the signal voltage can swing negative to approximately  $-V_{SS}$ . Two bias lines are shown in Figure 11, one for  $V_{SS} = -15$  V and the other  $V_{SS} = -1.6$  V. For the first case, the quiescent output voltage lies between 0.18 and 0.74 V. For the second, it lies between 0.3 and 0.82 V.

A pair of matched FETs is used in the circuit of Figure 9d, one as a source follower and the other as a current source. The operating drain current ( $I_{DQ}$ ) is set by  $R_{S2}$ , as indicated by the load line of Figure 13. In this illustration the drain current may be anywhere from 0.2 to 0.42 mA, as shown by the limiting transfer characteristic intercepts; however,  $V_{GS1} = V_{GS2}$  because the FETs are matched. Other dual devices, such as 2N5912 and SST441, can operate at 5 mA and frequencies above 400 MHz.

## Biasing With Feedback Increases $Z_{IN}$

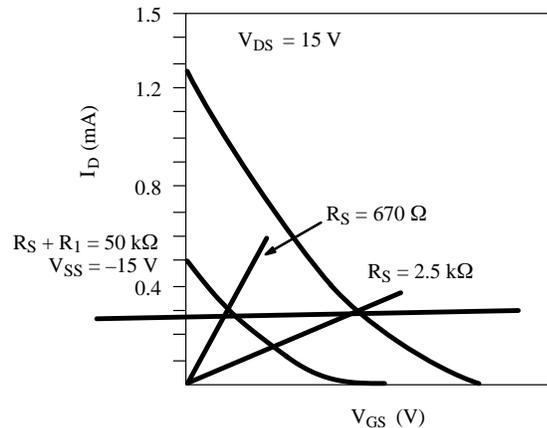
Each of the feedback-type source followers (Figure 9e through 9h) is biased by a method similar to that used with the nonfeedback circuit above it. However, in each case,  $R_G$  is returned to a point in the source circuit that provides almost unity feedback to the lower end of  $R_G$ . If  $R_S$  is chosen so that  $R_G$  is returned to zero dc volts (except in circuit 9e), then the input/output offset is zero.  $R_1$  is usually much larger than  $R_S$ .

Circuit 9e is useful principally for ac-coupled circuits.  $R_S$  is usually much less than  $R_1$  to provide near-unity



**Figure 13.** The bias load line is set by  $R_S$  but the output load line is determined by  $R_S + R_1$  when gate feedback is employed (Figure 9e). The feedback  $V_{FB}$  is determined by the intercept of the  $R_S + R_1$  load line and the  $V_{GS}$  axis.

feedback. The bias load line is set by  $R_S$  (Figure 13). The output load line, however is determined by the sum of  $R_S + R_1$ . The feedback voltage  $V_{FB}$ , measured at the junction of  $R_S$  and  $R_1$ , is determined by the intercept of the  $R_S + R_1$  load line with the  $V_{GS}$  axis. The quiescent output voltage is  $V_{FB} - V_{GS}$ .



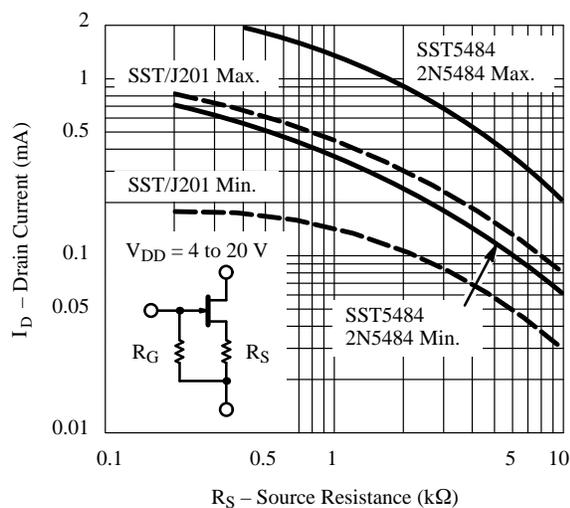
**Figure 14.**  $R_S$  can be trimmed to provide zero offset at some point between 670  $\Omega$  and 2.5 k $\Omega$  (Figure 9f). The source load line intercepts the  $V_{GS}$  axis at  $V_{SS} = V_{GG} = -15$  V. Note that this load line is not perfectly flat. It has a slope of  $-1/50$  k $\Omega$ , because the current source is not perfect; it has a finite impedance.

In the circuit of Figure 9f,  $R_S$  can be trimmed to provide zero offset. As the curves show (Figure 14),  $R_S$  will be between 670  $\Omega$  and 2.5 k $\Omega$ .  $R_S$  is much less than  $R_1$ . The source load line intercepts the  $V_{GS}$  axis at  $V_{SS} = -V_{GG} = -15$  V.

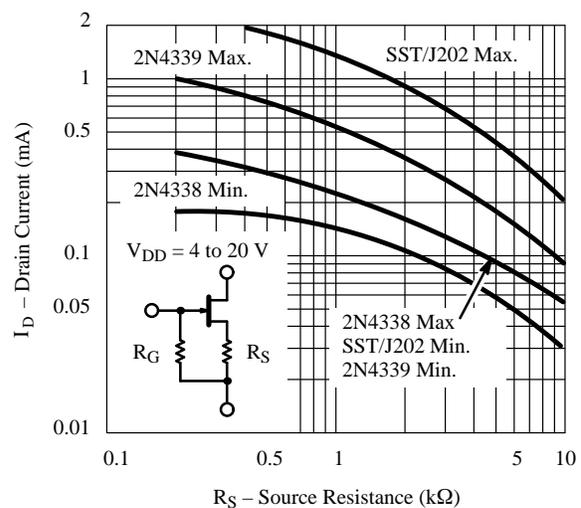
## Practical Amplifier Biasing Examples

All commercially available JFET part numbers exhibit a significant variation in the  $I_{DSS}$  and  $V_{GS(off)}$  parameters. Applying the Figure 9a and 9d biasing configurations, Figures 15 and 16 provide typical worst case drain-current extremes as a function of source resistance. Plotted are the popular low-current amplifiers.

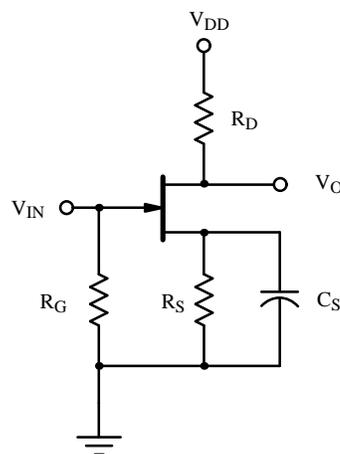
Part Number	Package
2N4338, 2N4339	TO-206AA (TO-18) Metal Can
J201, J202, 2N5484	TO-226AA (TO-92) Through-Hole Plastic
SST201, SST202, SST5484	TO-236 (SOT-23) Surface Mount



**Figure 15.** JFET Source Biased Drain-Current vs. Source Resistance

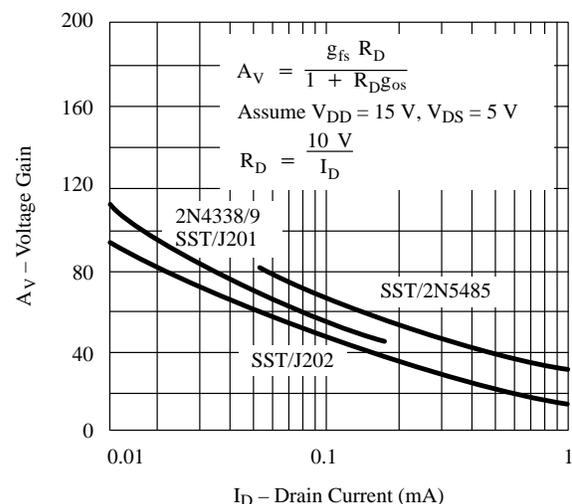


**Figure 16.** JFET Source Biased Drain-Current vs. Source Resistance



**Figure 17.** JFET Source Biased Amplifier

Applying the Figure 9a biasing technique to a small-signal amplifier circuit as illustrated in Figure 17, results in typical voltage gain as plotted in Figure 18. Note that as the drain current decreases the overall gain increases since  $R_D$  can be greater, despite transconductance  $g_{fs}$  decreasing.



**Figure 18.** Circuit Voltage Gain vs. Drain-Current