

Committed to flexible digital TV and PC/TV solutions, Philips Semiconductors has developed a complete DTV receiver reference design based on proven ICs from other reference designs. It is laid out according to Device Bay physical specifications and allows a DTV transport stream to be carried over Device Bay or IEEE 1394 connections.

## IEEE 1394/Device Bay ATSC DTV receiver

### Reference design



### Applications

- Digital ATSC-compliant terrestrial reception
- Personal computers with digital television capabilities
- Modular digital home entertainment systems

### Highly featured board

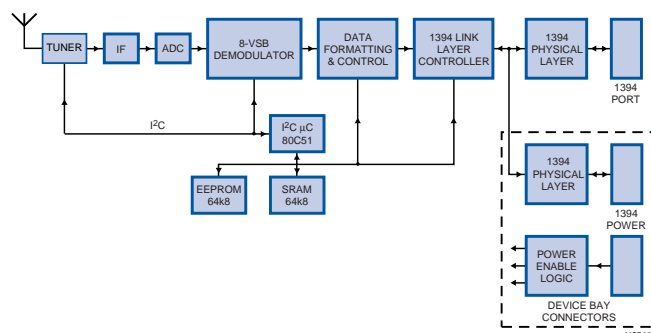
- Outputs a DTV transport stream over IEEE 1394 or Device Bay connections
- Reference design laid out according to Device Bay physical specifications
- Single-chip TDA8960 ATSC-compliant 8-VSB demodulator and decoder front-end
- PDI1394P11 IEEE 1394-1995 Physical layer controller supports data transfer at up to 200 Mbits/s
- PDI1394L11 IEEE 1394-1995 A/V Link layer controller with hardware support for IEC61883
- TDA9829 IF downconversion for VSB

### Highly integrated DTV front-end, with IEEE 1394/Device Bay transport stream output

In the fast moving digital broadcast market, where TV and PC technologies are converging, the high performance IEEE 1394 bus is now the established high-speed, real-time true plug-and-play serial bus system. As its popularity grows, it is becoming the accepted standard for connecting a variety of digital consumer electronics equipment to each other, as well as to multimedia PCs and workstations. Drawing on Philips Semiconductors' acknowledged expertise in digital TV systems and IEEE 1394 interface devices, this reference design combines these technologies in the emerging Device Bay format, creating a simple high performance DTV receiver for PC and other IEEE 1394-based applications.

Based around a proven 8-VSB (Vestigial SideBand) demodulator with on-chip digital tuner AGC control, used in the established 'Coney' PCI-based ATSC/NTSC PC-TV board, this reference design also incorporates Philips' advanced IEEE 1394 devices: a high-performance Link layer controller with isochronous operation and embedded IEC61883 support; and a three-port Physical layer interface. These high-speed devices enable the digital TV signal (MPEG2 transport stream) to be transferred over the IEEE 1394 bus at 200 Mbits/s, output via either 1394 port or Device Bay connections.

This reference design enables platform providers to concentrate on developing the user interfaces and applications that will differentiate them in a market where competition is very fierce. A licence is available, royalty-free, from Philips Semiconductors to use the PCB layout (Gerber) files as well as the original design schematics.



Let's make things better.



PHILIPS

# COMPLETE REFERENCE DESIGN FOR A IEEE 1394/DEVICE BAY ATSC DTV RECEIVER MODULE

*This reference design demonstrates a complete solution for capture, demodulation and decoding of ATSC-compliant DTV signals, and outputting DTV transport streams over the high speed IEEE 1394 bus using either IEEE 1394 or Device Bay connections. It uses just three core ICs: the TDA8960 VSB demodulator/decoder and two IEEE 1394 ICs - a physical layer controller and A/V link layer controller.*



## SINGLE-CHIP ATSC DEMODULATOR/DECODER

- TDA8960 ATSC-compliant 8-VSB demodulator and concatenated Trellis (Viterbi)/Reed-Solomon decoder with de-interleaver and de-randomizer
- 8-bit MPEG2 transport stream output
- On-chip digital tuner AGC control
- Integrated digital Square-Root Raised-Cosine (half Nyquist) filter with 11.5 % roll-off
- Feed forward adaptive equalizer including a Decision Feedback Equalizer (DFE)
- Reed-Solomon decoder with internal convolutional de-interleaving
- De-randomizer based on ATSC standard
- Rate 2/3 (rate 1/2 Ungerboeck-code-based) Trellis (Viterbi) decoder

One of the key chips in the Device Bay module, the TDA8960 accepts 8-VSB modulated signals from the IF block of the tuner front-end, or alternatively, the VSB IC AGC control output can be applied directly to the tuner. Adaptive equalization using the ATSC field sync (trained equalization) and/or the 8-VSB data itself (blind equalization) is performed via a decision feedback equalizer (DFE) following internal carrier recovery, half Nyquist filtering and symbol timing recovery.

Following trellis decoding, the stream is de-interleaved with a convolutional de-interleaver with on-chip memory. The ATSC-compliant Reed-Solomon decoder has a length of 207 and can correct up to 10 bytes. After decoding, the stream is de-randomized and passed to a FIFO, preventing irregular gaps in the data; this then outputs an 8-bit MPEG2 transport stream for de-multiplexing.

## PROVEN HIGH PERFORMANCE IEEE 1394 SILICON

Philips Semiconductors' controllers deliver a high-performance, low-cost, proven IEEE 1394 system solution. Our Physical layer controllers are fully interoperable with all 1394 link layer controllers including PCI/OCHI compatible devices, while our Link layer controllers offer support for MPEG2 and DV data streams, and IEC61883. Our latest full duplex A/V link layer controller (PDI1394L21) also supports processor based time stamp handling. All Philips IEEE 1394 silicon offers bus holder circuits on the Link/PHY interface, allowing effective node isolation - required in almost all 1394-enabled equipment. A single capacitor in series with each Link/PHY interface line provides economical yet highly effective isolation.

## **PDI1394L11 1394 A/V Link layer controller**

- Full IEEE 1394-1995 compliant
- Hardware support for IEC 61883 standard
- A/V interface port supports high-speed (isochronous) digital data streams
- Asynchronous interface port supports command and control functions
- Compatible with any IEEE 1394-1995 100, 200 and 400 Mbits/s physical layer devices

Philips' PDI1394L11, is an IEEE 1394-1995 link layer controller featuring an embedded A/V layer interface. The A/V layer is designed to pack and un-pack application data packets for transmission over an IEEE 1394 bus using isochronous data transfers.

Application data is packetized according to IEC61883 specification of digital interface for consumer electronic audio/video equipment. The A/V layer interface is a byte wide port capable of accommodating various MPEG2 and DV codecs. A byte wide host interface is provided for internal register configuration as well as performing asynchronous data transfers.

## **PDI1394P11 three-port Physical Layer Controller**

- IEEE 1394-1995 compliant
- Three cable ports capable of 100 Mbits/s and 200 Mbits/s data rates
- Energy saving power down feature offers lower power consumption than competing devices
- Interfaces to any IEEE 1394 standard link layer controller

Integrated on the main board for output over 1394 port connections, or on a Device Bay daughter card for output over a Device Bay signal connector, the PDI1394P11 provides the analog physical layer functions to connect to a three-port node in a 1394 application. It manages bus initialization and arbitration cycles, as well as transmission and reception of data bits. Supporting the IEEE 1394a short arbitrated bus reset, the PDI1394P11 reduces reset times and hence the risk of losing isochronous data.

## **TDA9829 IF downconverter**

The TDA9829 DTV IF amplifier/converter chip provides the signal stages for IF processing to the DVB standard, down-converting the digital Quadrature Amplitude Modulation (QAM) signal to a frequency matching the symbol rate. It features VCO for QAM carrier recovery, internal and external AGC for DVB, and is applicable for VSB (HDTV) IF and OFDM downconversion.

The board supports standard 6 MHz VHF/UHF digital terrestrial TV channels in the 38.9 MHz to 45.75 MHz frequency range.

IF gain is controlled using three AC-coupled, differential amplifier stages, with a feedback stage controlled by emitter-degeneration.

## **87C654 microcontroller**

Together with an FPGA, the microcontroller performs basic data, address and control signal handling, as well power-up and reset functions. A derivative of the 80C51 microcontroller family, with the same instruction set, it has a non-volatile 16 k x 8 EPROM and a volatile 256 x 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters, nested multiple interrupts, an I<sup>2</sup>C-bus interface and on-board UART.

## **The IEC61883 standard**

Today, transmission of digital video and audio data is commonplace, demanding standards to ensure compatibility of equipment and interfaces. IEC61883 specifies a digital interface for consumer electronic audio/video equipment. As a major contributor to the IEC61883 protocol Philips has in-depth expertise in the implementation of IEC61883 over IEEE 1394.

The IEC61883 standard describes the general packet format, data flow and connection management for audio/visual data. General transmission rules for control commands are also specified, as are the transmission protocol and control commands for digital audio and video equipment connecting via the IEEE 1394 interface. Data packetization and transmission timing for MPEG2 transport streams transmitted over the IEEE 1394 interface and specifications for the IEEE 1394 packet itself are also covered by IEC61883.

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