



# LC72191, 72191M, 72191JM

## PLL Frequency Synthesizer for Electronic Tuning in Car Stereo Tuners



### Overview

The LC72191, LC72191M and LC72191JM are PLL frequency synthesizers for electronic tuning. The LC72191, LC72191M and LC72191JM are optimal for AM/FM tuner circuits that require high mounting densities.

### Features

Designed for use in car stereos, the LC72191 provides a rich set of reference frequencies, I/O ports, a general-purpose counter, and an unlock detection circuit.

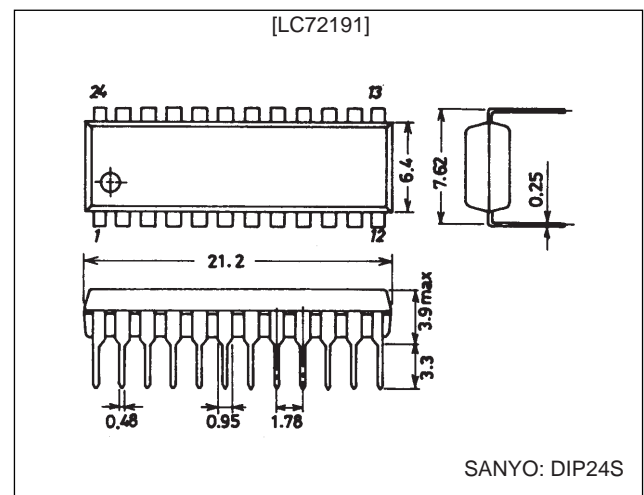
### Functions

- Programmable dividers
  - FMIN pin: 130 MHz at 70 mVrms and 160 MHz at 100 mVrms input (built-in prescaler)
  - AMIN pin: Pulse swallower and direct division techniques
- Reference frequencies: Ten selectable frequencies: 1, 5, 9, 10, 3.125, 6.25, 12.5, 25, 50 and 100 kHz
- Output ports: 7 pins
  - Complementary outputs: 2 pins
  - N-channel open drain outputs: 5 pins
- Input ports: 2 pins
- General-purpose counter: For measuring IF and other signals (Also used for station detection when functioning as an IF counter.)
  - HCTR pin: Frequency measurement (for inputs up to 70 MHz)
  - LCTR pin: Frequency and period measurement
- PLL unlock detection circuit
  - Detects phase differences of 0.55, 1.11, 2.22 and 3.33  $\mu$ s.
- Controller clock output: 400 kHz
- Clock time base output: 8 Hz
- Serial data I/O
  - Supports CCB format communication with the system controller.
- Package: LC72191: DIP24S  
LC72191M: MFP24  
LC72191JM: MFP24S

### Package Dimensions

unit: mm

3067-DIP24S



- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

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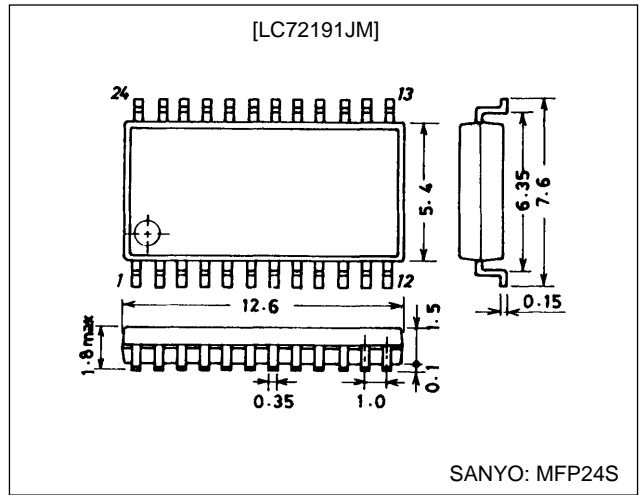
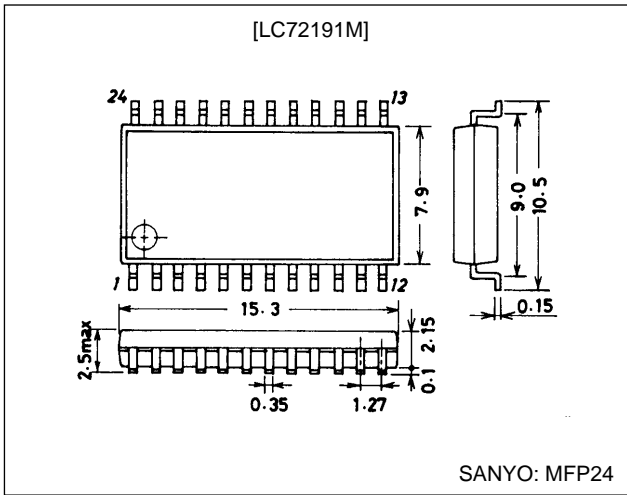
Package Dimensions

unit: mm

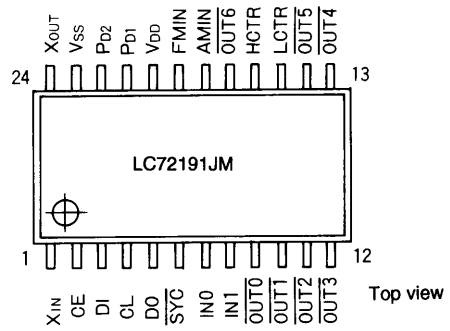
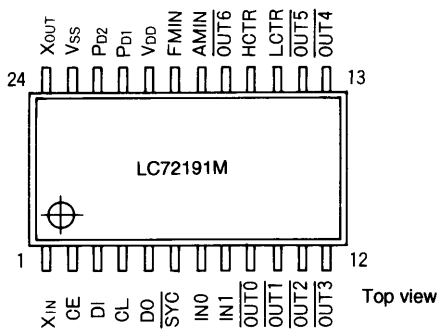
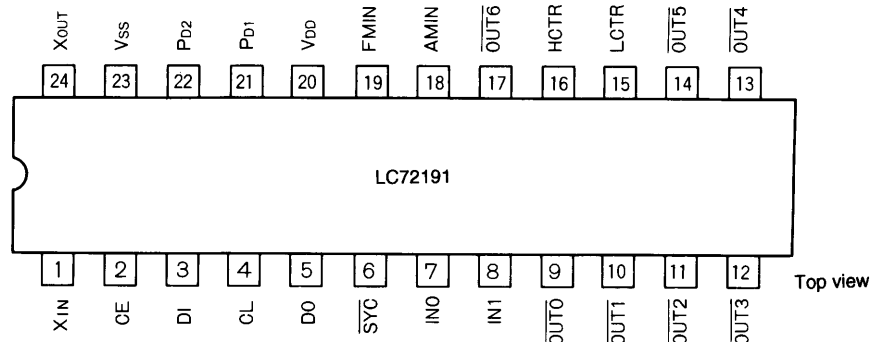
3045B-MFP24

unit: mm

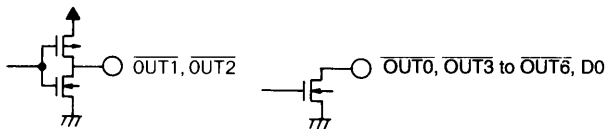
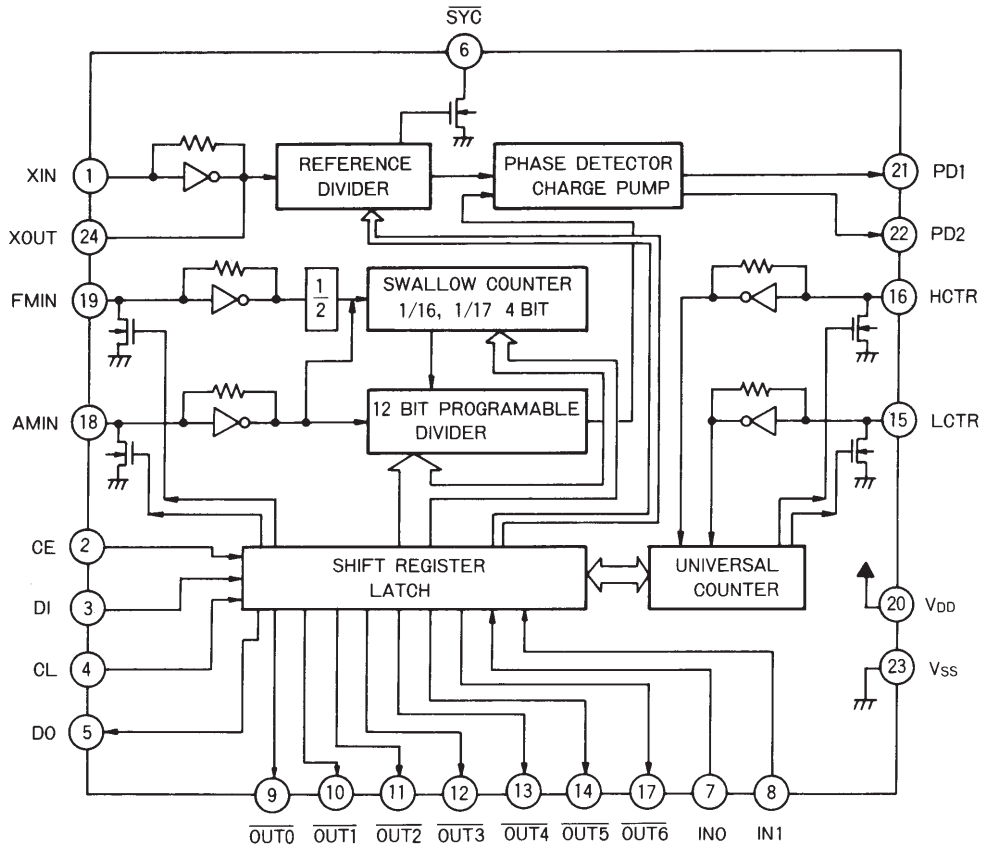
3112-MFP24S



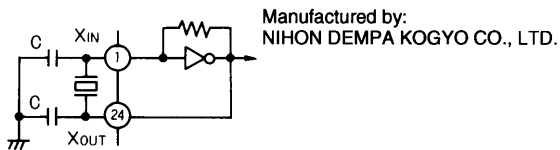
Pin Assignments



**Block Diagram**



**Note:** Crystal oscillator example: 7.200 MHz, CL16pF (C = 27 pF)  
 • LN-X-0702(NR-18 type)  
 • LN-P-0001 (AT-51 type)



**Pin Symbols**

- XIN, XOUT: Crystal oscillator (7.2 MHz)
- FMIN, AMIN: Local oscillator signal input
- CE, CL, DI, DO: Serial data I/O
- OUT0 to OUT6: Output ports
- IN0, IN1: Input ports
- HCTR, LCTR: General-purpose counter inputs
- PD1, PD2: Charge pump outputs
- SYC: Control clock (400 kHz)

**Specifications**

**Absolute Maximum Ratings at Ta = 25°C, VSS = 0 V**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>DD max</sub>	V <sub>DD</sub>	-0.3 to +7.0	V
Input voltage	V <sub>IN (1)</sub>	CE, CL, DI, IN0, IN1	-0.3 to +7.0	V
	V <sub>IN (2)</sub>	Input pins other than V <sub>IN (1)</sub>	-0.3 to V <sub>DD</sub> + 0.3	V
Output voltage	V <sub>OUT (1)</sub>	DO, SYC	-0.3 to +7.0	V
	V <sub>OUT (2)</sub>	OUT1, OUT2	-0.3 to V <sub>DD</sub> + 0.3	V
	V <sub>OUT (3)</sub>	OUT3 to OUT6, OUT0	-0.3 to +15	V
	V <sub>OUT (4)</sub>	Output pins other than V <sub>OUT (1)</sub> , V <sub>OUT (2)</sub> and V <sub>OUT (3)</sub>	-0.3 to V <sub>DD</sub> + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 85°C :LC72191	350	mW
		:LC72191M	300	
		:LC72191JM	200	
Operating temperature	T <sub>opr</sub>		-40 to +85	°C
Storage temperature	T <sub>stg</sub>		-55 to +125	°C

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### Allowable Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$ , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	$V_{DD} (1)$	$V_{DD}$	4.5		6.5	V
	$V_{DD} (2)$	$V_{DD}$ : Crystal oscillator guaranteed operation	3.5		6.5	V
Input high level voltage	$V_{IH} (1)$	CE, CL, DI, IN0, IN1	2.2		6.5	V
	$V_{IH} (2)$	LCTR: Pulse waveform, DC coupling*4	$0.7 V_{DD} (1)$		$V_{DD} (1)$	V
Input low level voltage	$V_{IL} (1)$	CE, CL, DI, IN0, IN1	0		0.7	V
	$V_{IL} (2)$	LCTR*4	0		$0.3 V_{DD} (1)$	V
Output voltage	$V_{OUT} (1)$	DO, $\overline{\text{SYC}}$			6.5	V
	$V_{OUT} (2)$	$\overline{\text{OUT3}}$ to $\overline{\text{OUT6}}$ , $\overline{\text{OUT0}}$			13	V
Input frequency	$f_{IN} (1)$	XIN: Sine wave capacitor coupling, $V_{DD} (2)$	1.0	7.2	8.0	MHz
	$f_{IN} (2)$	FMIN: Sine wave capacitor coupling, $V_{DD} (1)^{*1}$	10		$130 (160)^{*5}$	MHz
	$f_{IN} (3)$	AMIN: Sine wave capacitor coupling, $V_{DD} (1)^{*1}$	0.5		40	MHz
	$f_{IN} (4)$	HCTR: Sine wave capacitor coupling, $V_{DD} (1)^{*2}$	10		$60 (70)^{*6}$	MHz
	$f_{IN} (5)$	LCTR: Sine wave capacitor coupling, $V_{DD} (1)^{*3}$	15		500	kHz
	$f_{IN} (6)$	LCTR: Pulse wave DC coupling, $V_{DD} (1)^{*4}$	1.0		$20 \times 10^3$	Hz
Crystal oscillators for which operation is guaranteed	Xtal	$X_{IN}$ , $X_{OUT}$ : $Cl \leq 50 \Omega$	3.0	7.2	8.0	MHz
Input amplitude	$V_{IN} (1)$	$X_{IN}$ : Sine wave capacitor coupling, $V_{DD} (1)$	0.5		1.5	Vrms
	$V_{IN} (2)$	FMIN: Sine wave capacitor coupling, $V_{DD} (1)$	0.070 (0.100)*5		1.5	Vrms
	$V_{IN} (3)$	AMIN: Sine wave capacitor coupling, $V_{DD} (1)$	0.070		1.5	Vrms
	$V_{IN} (4)$	HCTR: Sine wave capacitor coupling, $V_{DD} (1)^{*2}$	0.070 (0.100)*6		1.5	Vrms
	$V_{IN} (5)$	LCTR: Sine wave capacitor coupling, $V_{DD} (1)^{*3}$	0.070		1.5	Vrms

Note: 1.

DV	SP	Input frequency	1/2 divider	1/16, 17 swallow	12-bit main divider	Input pin
1	*	10 to 130 (160) MHz	○	○	○	FMIN
0	1	2 to 40 MHz	—	○	○	AMIN
0	0	0.5 to 10 MHz	—	—	○	AMIN

DV and SP are bits in the serial data.

\*: don't care

2. Frequency measurement
3. Frequency measurement
4. Period measurement
5.  $f_{IN} (2)$ : 10 to 160 MHz/ $V_{IN} (2)$   
0.100 Vrms (minimum)
6.  $f_{IN} (4)$ : 10 to 70 MHz/ $V_{IN} (4)$   
0.100 Vrms (minimum)

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**Electrical Characteristics for the Allowable Operating Ranges**

Parameter	Symbol	Conditions	min	typ	max	Unit
Internal feedback resistance	Rf (1)	XIN		1.0		MΩ
	Rf (2)	FMIN		500		kΩ
	Rf (3)	AMIN		500		kΩ
	Rf (4)	HCTR		500		kΩ
	Rf (5)	LCTR		500		kΩ
Hysteresis	V <sub>H</sub>	LCTR	0.1 V <sub>DD</sub>		0.6 V <sub>DD</sub>	V
Input high level current	I <sub>IH</sub> (1)	CE, CL, DI: V <sub>I</sub> = 6.5 V			5.0	μA
	I <sub>IH</sub> (2)	IN0, IN1: V <sub>I</sub> = V <sub>DD</sub>			5.0	μA
	I <sub>IH</sub> (3)	XIN: V <sub>I</sub> = V <sub>DD</sub>			20	μA
	I <sub>IH</sub> (4)	FMIN, AMIN: V <sub>I</sub> = V <sub>DD</sub>			40	μA
	I <sub>IH</sub> (5)	HCTR, LCTR: V <sub>I</sub> = V <sub>DD</sub>			40	μA
Input low level current	I <sub>IL</sub> (1)	CE, CL, DI: V <sub>I</sub> = V <sub>SS</sub>			5.0	μA
	I <sub>IL</sub> (2)	IN0, IN1: V <sub>I</sub> = V <sub>SS</sub>			5.0	μA
	I <sub>IL</sub> (3)	XIN: V <sub>I</sub> = V <sub>SS</sub>			20	μA
	I <sub>IL</sub> (4)	FMIN, AMIN: V <sub>I</sub> = V <sub>SS</sub>			40	μA
	I <sub>IL</sub> (5)	HCTR, LCTR: V <sub>I</sub> = V <sub>SS</sub>			40	μA
Output high level voltage	V <sub>OH</sub> (1)	$\overline{\text{OUT1}}, \overline{\text{OUT2}}$ : I <sub>O</sub> = 1 mA	V <sub>DD</sub> - 1.0			V
	V <sub>OH</sub> (2)	PD1, PD2: I <sub>O</sub> = 0.5 mA	V <sub>DD</sub> - 1.0			V
Output low level voltage	V <sub>OL</sub> (1)	$\overline{\text{OUT1}}, \overline{\text{OUT2}}$ : I <sub>O</sub> = 1 mA			1.0	V
	V <sub>OL</sub> (2)	PD1, PD2: I <sub>O</sub> = 0.5 mA			1.0	V
	V <sub>OL</sub> (3)	$\overline{\text{OUT3}}$ to $\overline{\text{OUT6}}$ : I <sub>O</sub> = 5 mA			1.0	V
	V <sub>OL</sub> (4)	$\overline{\text{OUT0}}$ : I <sub>O</sub> = 1 mA			1.0	V
	V <sub>OL</sub> (5)	DO: I <sub>O</sub> = 5 mA			1.0	V
	V <sub>OL</sub> (6)	$\overline{\text{SYC}}$ : I <sub>O</sub> = 0.5 mA (V <sub>DD</sub> = 3.5 to 6.5 V)			1.0	V
Output off leakage current	I <sub>OFF</sub> (1)	$\overline{\text{OUT3}}$ to $\overline{\text{OUT6}}, \overline{\text{OUT0}}$ : V <sub>O</sub> = 13 V			5.0	μA
	I <sub>OFF</sub> (2)	DO: V <sub>O</sub> = 6.5 V			5.0	μA
	I <sub>OFF</sub> (3)	$\overline{\text{SYC}}$ : V <sub>O</sub> = 6.5 V (V <sub>DD</sub> = 3.5 to 6.5 V)			5.0	μA
Three-state high level off leakage current	I <sub>OFFH</sub>	PD1, PD2: V <sub>O</sub> = V <sub>DD</sub>		0.01	10.0	nA
Three-state low level off leakage current	I <sub>OFFL</sub>	PD1, PD2: V <sub>O</sub> = V <sub>SS</sub>		0.01	10.0	nA
Input capacitance	C <sub>IN</sub>	FMIN, HCTR	1	2	3	pF
Current drain	I <sub>DD</sub> (1)	V <sub>DD</sub> : f <sub>IN</sub> (2) = 130 MHz, V <sub>IN</sub> (2) = 70 mVrms, with a 7.2 MHz crystal, other input pins at V <sub>SS</sub> , output pins open		20	30	mA
	I <sub>DD</sub> (2)	V <sub>DD</sub> : PLL block stopped (PLL inhibit state), crystal oscillator operating ( $\overline{\text{SYC}}$ , TB), with a 7.2 MHz crystal, other input pins at V <sub>SS</sub> , output pins open		1.0		mA

Note: A capacitor of at least 2000 pF must be inserted between the power supply V<sub>DD</sub> and V<sub>SS</sub> potentials.

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### Pin Functions

Pin No.	Symbol	I/O	Type	Function
1 24	X <sub>IN</sub> X <sub>OUT</sub>	Input Output	Xtal OSC	<ul style="list-style-type: none"> <li>Connections for a 7.2 MHz crystal oscillator</li> </ul>
19	FMIN	Input	Local oscillator signal input	<ul style="list-style-type: none"> <li>FMIN is selected when DV in the serial input data is set to 1.</li> <li>Input frequency range: 10 to 130 MHz (70 mVrms minimum)</li> <li>The signal passes through an internal divide-by-two prescaler and is then supplied to the swallow counter.</li> <li>Although the divisor setting is in the range 256 to 65,536, the actual divisor will be twice the set value due to the presence of the internal divide-by-two prescaler.</li> </ul>
18	AMIN	Input	Local oscillator signal input	<ul style="list-style-type: none"> <li>AMIN is selected when DV in the serial input data is set to 0.</li> <li>When SP in the serial input data is set to 1: <ul style="list-style-type: none"> <li>Input frequency range: 2 to 40 MHz (70 mVrms minimum).</li> <li>The signal is supplied directly to the swallow counter without passing through the internal divide-by-two prescaler.</li> <li>The divisor setting is in the range 256 to 65,536 and the actual divisor will be the value set.</li> </ul> </li> <li>When SP in the serial input data is set to 0: <ul style="list-style-type: none"> <li>Input frequency range: 0.5 to 10 MHz (70 mVrms minimum).</li> <li>The signal is supplied directly to a 12-bit programmable divider.</li> <li>The divisor setting is in the range 4 to 4,096 and the actual divisor will be the value set.</li> </ul> </li> </ul>
21 22	PD1 PD2	Three-state	Charge pump outputs	<ul style="list-style-type: none"> <li>PLL charge pump outputs. High levels are output from PD1 and PD2 when the local oscillator frequency divided by n is higher than the reference frequency, and low levels are output when that frequency is lower than the reference frequency. These pins go to the floating state when the frequencies agree.</li> </ul>
6	$\overline{\text{SYC}}$	N-channel open drain	Controller clock	<ul style="list-style-type: none"> <li><math>\overline{\text{SYC}}</math> is a controller clock source. The LC72191 outputs a 400 kHz 66% duty signal from this pin after power is applied.</li> </ul>
20	V <sub>DD</sub>	—	Power supply	<ul style="list-style-type: none"> <li>The LC72191 power supply pin. A voltage of between 4.5 and 6.5 V must be provided when the PLL is operating. The supply voltage can be lowered to 3.5 V when only operating the crystal oscillator circuit to acquire the controller clock and the clock time base outputs.</li> </ul>
23	V <sub>SS</sub>	—	Ground	<ul style="list-style-type: none"> <li>The LC72191 ground pin</li> </ul>
2	CE	Input*1	Chip enable	<ul style="list-style-type: none"> <li>This pin must be set high when inputting serial data (via DI) or when outputting serial data (via DO).</li> </ul>
4	CL	Input*1	Clock	<ul style="list-style-type: none"> <li>The clock input used for data signal synchronization during serial data input (via DI) or output (via DO).</li> </ul>
3	DI	Input*1	Input data	<ul style="list-style-type: none"> <li>Input pin used when transferring serial data from the controller to the LC72191.</li> <li>A total of 36 bits of data must be supplied to set up the LC72191 initial state.</li> </ul>
5	DO	Output (N-channel open drain)	Output data	<ul style="list-style-type: none"> <li>Output pin used when transferring serial data to the controller from the LC72191.</li> <li>A total of 28 bits from an internal shift register can be output in synchronization with the CL signal.</li> </ul>
9 10 11 12 13 14 17	$\overline{\text{OUT0}}$ $\overline{\text{OUT1}}$ $\overline{\text{OUT2}}$ $\overline{\text{OUT3}}$ $\overline{\text{OUT4}}$ $\overline{\text{OUT5}}$ $\overline{\text{OUT6}}$	Output*2	Output port	<ul style="list-style-type: none"> <li>These pins latch bits O<sub>0</sub> to O<sub>6</sub> in the serial data transferred from the controller, invert that data and output the inverted data in parallel.</li> <li>The <math>\overline{\text{OUT0}}</math> pin can also be used to output an 8 Hz clock time base signal. (When TB is 1.)</li> <li><math>\overline{\text{OUT1}}</math> and <math>\overline{\text{OUT2}}</math> are complementary outputs.</li> <li><math>\overline{\text{OUT0}}</math>, <math>\overline{\text{OUT3}}</math>, <math>\overline{\text{OUT4}}</math>, <math>\overline{\text{OUT5}}</math> and <math>\overline{\text{OUT6}}</math> are N-channel open drain outputs that can handle up to 13 V.</li> </ul>

Note: \*1. The high and low level input voltages for the CE, CL, DI, IN0 and IN1 pins are V<sub>IH</sub> = 2.2 to 6.5 V and V<sub>IL</sub> = 0 to 0.7 V, regardless of the power supply voltage V<sub>DD</sub>.

\*2. Since the output port states are undefined when power is first applied, transfer the control data quickly.

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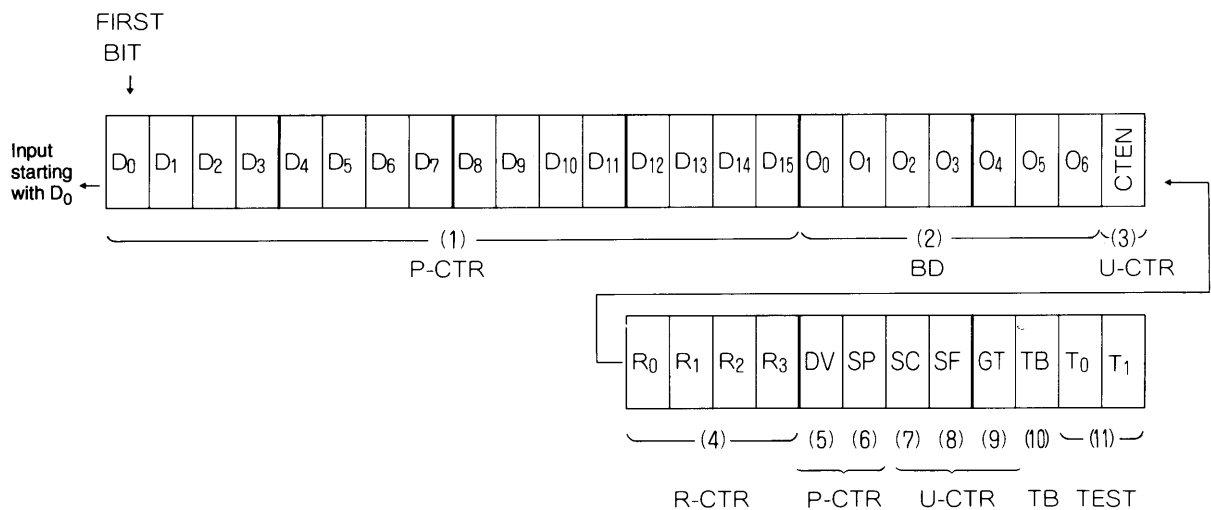
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Pin No.	Symbol	I/O	Type	Function
7 8	IN0 IN1	Input*	Input port	<ul style="list-style-type: none"> <li>The values of the IN0 and IN1 input ports can be converted from parallel to serial and output from the DO output pin.</li> </ul>
16	HCTR	Input	General-purpose counter Frequency measurement signal input pin	<ul style="list-style-type: none"> <li>HCTR is selected when SC in the serial input data is set to 1.</li> <li>Input frequency range: 10 to 60 MHz (70 mVrms minimum)</li> <li>The signal is supplied to a general-purpose 20-bit binary counter after passing through a divide-by-eight circuit. Therefore, the value of the counter is 1/8 of the frequency actually input to HCTR.</li> <li>When HCTR is selected the LC72191 will function in frequency measurement mode and the measurement period can be selected to be either 12 or 24 ms. (GT = 0: 12 ms, 1: 24 ms)</li> <li>The result of the measurement (the value of the general-purpose counter) can be output MSB first from the DO output pin.</li> </ul>
15	LCTR	Input	General-purpose counter Frequency or period measurement signal input pin	<ul style="list-style-type: none"> <li>LCTR is selected when SC in the serial input data is set to 0.</li> <li>When SF in the serial input data is set to 1: <ul style="list-style-type: none"> <li>Frequency measurement mode is selected.</li> <li>Input frequency range: 15 to 500 kHz (70 mVrms minimum).</li> <li>The signal is supplied directly to the general-purpose counter without passing through the internal divide-by-eight circuit.</li> <li>The measurement period is the same as for HCTR.</li> </ul> </li> <li>When SF in the serial input data is set to 0: <ul style="list-style-type: none"> <li>Period measurement mode is selected.</li> <li>Input frequency range: 1 Hz to 20 kHz (<math>V_{IH} = 0.7 V_{DD}</math> minimum, <math>V_{IL} = 0.3 \cdot V_{DD}</math> maximum)</li> <li>The measurement can be selected to be for one or two cycles. If two cycle measurement is selected the input frequency range becomes 2 Hz to 20 kHz. (GT = 0: one cycle, 1: two cycles)</li> </ul> </li> <li>Measurement results are output in the same manner as HCTR measurement results.</li> </ul>

Note: \* The high and low level input voltages for the CE, CL, DI, IN0 and IN1 pins are  $V_{IH} = 2.2$  to 6.5 V and  $V_{IL} = 0$  to 0.7 V, regardless of the power supply voltage  $V_{DD}$ .

### Control Data Format (serial input data)



The LC72191 control data consists of 36 bits. All 36 bits must be input after power is applied to set up the LC72191 initial state. This is because the last two bits, while being unrelated to user functions, are data that switches the LSI test modes.

Once the LC72191 has been initialized, the contents of the first 24 bits ( $D_0$  to  $CTEN$ ) can be changed without changing the contents of the last 12 bits ( $R_0$  to  $T_1$ ) by inputting data to DI in serial data input mode.

**LC72191, 72191M, 72191JM**

No.	Control block/data	Description	Related data																																																																																		
(1)	Programmable divider data D <sub>0</sub> to D <sub>15</sub>	<ul style="list-style-type: none"> <li>This data sets up the programmable divider. D<sub>0</sub> to D<sub>15</sub> is a binary value with D<sub>15</sub> as the MSB. The position of the LSB is changed by DV and SP as listed in the table below.</li> </ul> <table border="1"> <thead> <tr> <th>DV</th> <th>SP</th> <th>LSB</th> <th>Divisor setting</th> <th>Actual divisor</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>*</td> <td>D0</td> <td>256 to 65536</td> <td>Twice the set value</td> </tr> <tr> <td>0</td> <td>1</td> <td>D0</td> <td>256 to 65536</td> <td>The set value</td> </tr> <tr> <td>0</td> <td>0</td> <td>D4</td> <td>4 to 4096</td> <td>The set value</td> </tr> </tbody> </table> <p>* don't care When D<sub>4</sub> is the LSB, bits D<sub>0</sub> to D<sub>3</sub> are ignored.</p>	DV	SP	LSB	Divisor setting	Actual divisor	1	*	D0	256 to 65536	Twice the set value	0	1	D0	256 to 65536	The set value	0	0	D4	4 to 4096	The set value	DV SP																																																														
DV	SP	LSB	Divisor setting	Actual divisor																																																																																	
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0	1	D0	256 to 65536	The set value																																																																																	
0	0	D4	4 to 4096	The set value																																																																																	
(2)	Output port data O <sub>0</sub> to O <sub>6</sub>	<ul style="list-style-type: none"> <li>Data that determines the states of the output ports <math>\overline{OUT0}</math> to <math>\overline{OUT6}</math>. O<sub>0</sub> determines the <math>\overline{OUT0}</math> pin output. However, note that when O<sub>0</sub> is 0, <math>\overline{OUT0}</math> will output a high level, and when O<sub>0</sub> is 1, <math>\overline{OUT0}</math> will output a low level. O<sub>1</sub> to O<sub>6</sub> function in the same manner.</li> <li>These can be used for a wide range of purposes, including, for example, band switching signals.</li> <li>When the TB bit is set to 1, the O<sub>0</sub> data is ignored and the <math>\overline{OUT0}</math> pin outputs an 8 Hz clock time base signal.</li> <li>Since the output port states are undefined when power is first applied, transfer the control data quickly.</li> </ul>	TB																																																																																		
(3)	General-purpose counter initial data CTEN	<ul style="list-style-type: none"> <li>Data that determines the operation of the general-purpose counter. When CTEN is 0, the 20-bit binary counter (the general-purpose counter) is reset and the HCTR and LCTR pins are pulled down to ground. When CTEN is set to 1, the general-purpose counter reset state is cleared and the counter operates according to the SC bit (the general-purpose selection data). In this state, the general-purpose counter will count either the HCTR or LCTR input signal.</li> <li>Since the general-purpose counter is reset by setting CTEN to 0, the result of a count operation must be sent to the controller while CTEN is still 1.</li> </ul>	SC SF GT																																																																																		
(4)	Reference frequency data R <sub>0</sub> to R <sub>3</sub>	<ul style="list-style-type: none"> <li>Data that selects one of the ten LC72191 reference frequencies or sets the LC72191 to backup mode in which PLL operation is disabled.</li> </ul> <table border="1"> <thead> <tr> <th>R<sub>0</sub></th> <th>R<sub>1</sub></th> <th>R<sub>2</sub></th> <th>R<sub>3</sub></th> <th>Reference frequency (kHz)</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>100</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>50</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>10</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>9</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td rowspan="4">PLL inhibit state*</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table> <p>Note: * PLL inhibit (backup mode) The programmable divider block is turned off, both the FMIN and AMIN pins are pulled down to ground, and the charge pump outputs go to the floating state.</p>	R <sub>0</sub>	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	Reference frequency (kHz)	0	0	0	0	100	0	0	0	1	50	0	0	1	0	25	0	0	1	1	25	0	1	0	0	12.5	0	1	0	1	6.25	0	1	1	0	3.125	0	1	1	1	3.125	1	0	0	0	10	1	0	0	1	9	1	0	1	0	5	1	0	1	1	1	1	1	0	0	PLL inhibit state*	1	1	0	1	1	1	1	0	1	1	1	1	
R <sub>0</sub>	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	Reference frequency (kHz)																																																																																	
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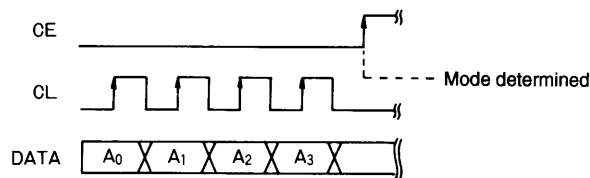


**Serial Data I/O Methods**

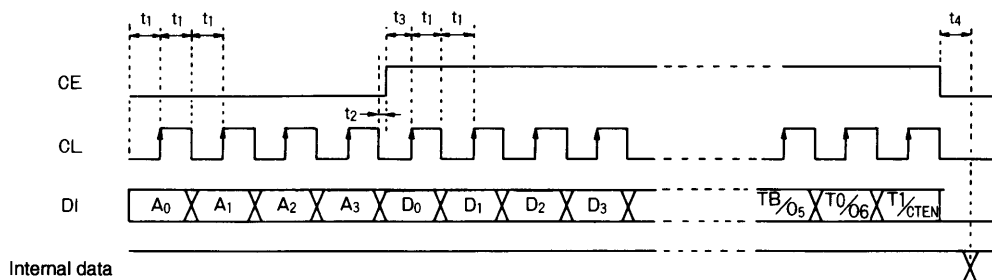
The LC72191 supports a total of three I/O modes: two control data input (serial data input) modes and one DO output (serial data output) mode. Data I/O is performed after the mode has been determined.

The mode is selected by four data items ( $A_0$  to  $A_3$ ) synchronized with a clock (the CL pin) applied before the CE pin is set high. The mode is determined when the CE pin goes high.

Mode	$A_3$	$A_2$	$A_1$	$A_0$	Item	Function
1	0	0	0	1	Serial data input (all bits)	<ul style="list-style-type: none"> <li>This mode is used to input all 36 bits of the control data (serial input data). This mode is used for initialization following power on and to change data that cannot be changed in mode 2. All 36 bits of the control data is input from the LC72191 DI pin.</li> </ul>
2	0	0	1	0	Serial data input (partial input)	<ul style="list-style-type: none"> <li>This mode is used to input a subset (24 bits) of the control data (serial input data). This mode is used to change three data items: the programmable divider data (<math>D_0</math> to <math>D_{15}</math>), the output port data (<math>O_0</math> to <math>O_6</math>) and the general-purpose counter start data (CTEN), for a total of 24 bits. The other 12 bits of control data are not changed by a mode 2 operation. (Use mode 1 when the other 12 bits must be changed.)</li> </ul>
3	0	0	1	1	Serial data output	<ul style="list-style-type: none"> <li>The DO output mode (serial data output) is used to output three data items from the DO pin: the input port data, the general-purpose counter binary data and the PLL unlock state data.</li> </ul>
	0 to 0	1 to 0	0 to 0	0 to 0	Invalid setting	<ul style="list-style-type: none"> <li>This mode is invalid and does not support any data input or output operations.</li> </ul>

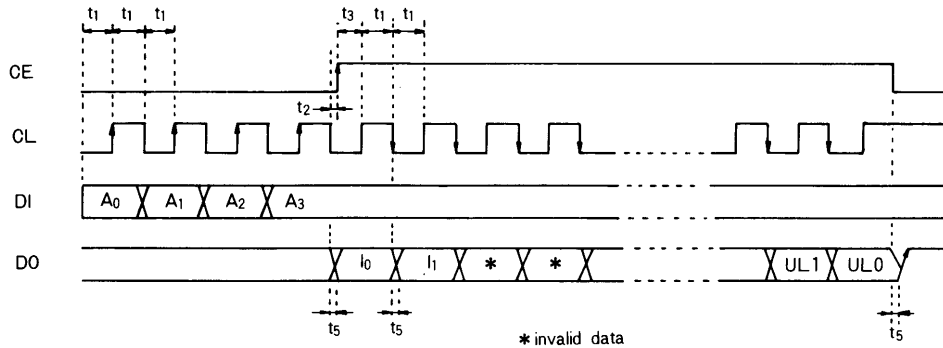


1. In the serial data input modes (modes 1 and 2),  $t_1 \geq 1.5 \mu\text{s}$ ,  $t_2 \geq 0 \mu\text{s}$ ,  $t_3 \geq 1.5 \mu\text{s}$ , and  $t_4 < 1.5 \mu\text{s}$ .



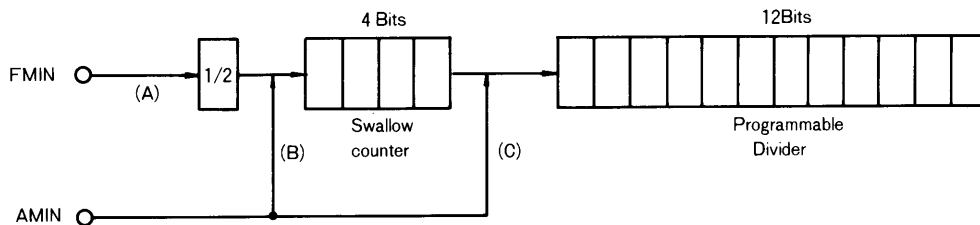
- Mode 1: A total of 40 bits, the four mode selection bits and the 36 control data bits (from  $D_0$  to  $T_1$ ), are input from the DI pin in synchronization with the clock (CL) signal.
- Mode 2: A total of 28 bits, the four mode selection bits and 24 control data bits (from  $D_0$  to CTEN), are input from the DI pin in synchronization with the clock (CL) signal.

2. In serial data output mode (mode 3),  $t_1 \geq 1.5 \mu\text{s}$ ,  $t_2 \geq 0 \mu\text{s}$ ,  $t_3 \geq 1.5 \mu\text{s}$ , and  $t_5 < 1.5 \mu\text{s}$ . (However, note that since the DO pin is an n-channel open drain output, the transition time depends on the value of the pull-up resistor.)



- Mode 3: Serial output mode (mode 3) is selected by the four bits of mode selection data. When the CE pin goes high,  $I_0$  is output from the DO pin. After that, the internal shift register is shifted and the next bit is output from the DO pin on each falling edge of the CL signal. (Thus 27 clock cycles are required to output all data through the UL0 bit after CE goes high.) When this mode is selected, at the point the CE pin falls to the low level, the DO pin will be forcibly set to the high level. The DO pin will go low if the IN0 pin input changes state or if a general-purpose counter measurement completes. (General-purpose counter completion takes precedence over changes in the IN0 pin signal.)

**Structure of the Programmable Divider**



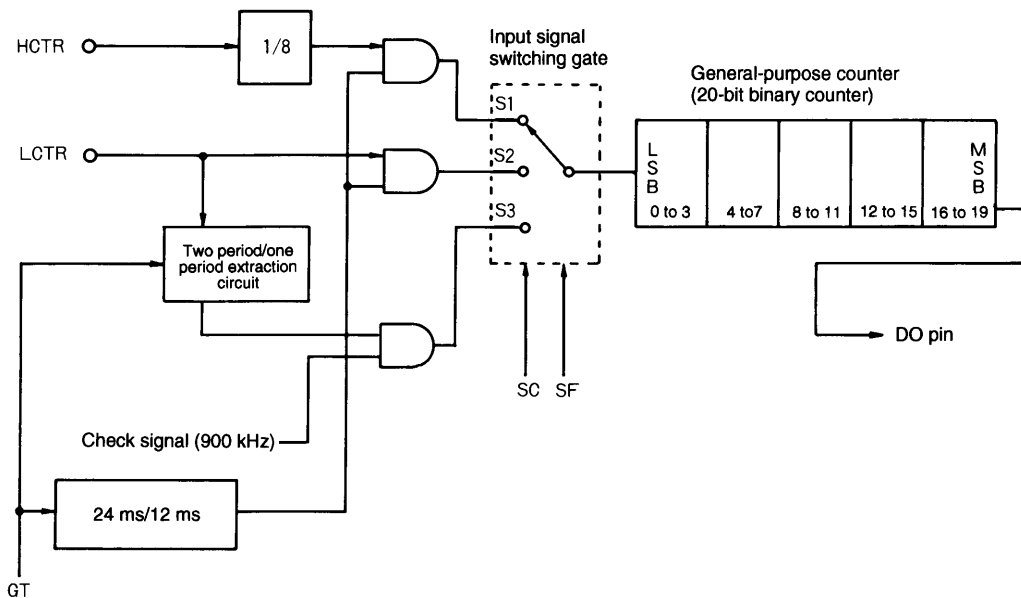
	DV	SP	Input pin	Divisor setting	Actual divisor	Input frequency range (MHz)
(A)	1	*	FMIN	256 to 65536	Twice the set value	10 to 130
(B)	0	1	AMIN	256 to 65536	The set value	2 to 40
(C)	0	0	AMIN	4 to 4096	The set value	0.5 to 10

- Note: 1. The actual divisor will be twice the set value when FMIN (A) is used.  
 For example, if the divisor setting is 1000 the actual divisor will be 2000 and if the divisor setting is 1001 the actual divisor will be 2002. In other words, the channel skip will be twice the reference frequency.
2. To set the channel skips of 1, 5 and 9 kHz using FMIN (A), the crystal oscillator should be changed to 3.6 MHz. However, the times listed in the table that follows change since they are referenced to the crystal oscillator frequency.  
 Note that care must be taken to prevent overtone oscillation when a 3.6 MHz crystal oscillator is used.

## LC72191, 72191M, 72191JM

Item	Xtal	
	7.2 MHz	3.6 MHz
Time base clock	8 Hz	4 Hz
System clock	400 kHz	200 kHz
Frequency measurement time	24/12 ms	48/24 ms
Frequency measurement check signal	900 kHz	450 kHz
Reference frequencies	100, 50, 25, ..... 10, 9, 5, 1 kHz	50, 25, 12, 5, ..... 5, 4.5, 2.5, 0.5 kHz
Serial data I/O (CL)	$t_1 \geq 1.5 \mu\text{s}$ , $t_3 \geq 1.5 \mu\text{s}$	$t_1 \geq 3.0 \mu\text{s}$ , $t_3 \geq 3.0 \mu\text{s}$

### Structure of the General-Purpose Counter



	SC	SF	Input pin	Measurement item	Measurement frequency range	GT (1/0)
$S_1$	1	*	HCTR	Frequency measurement	10 to 60 MHz (sine wave)	24 m/12 ms
$S_2$	0	1	LCTR	Frequency measurement	15 to 500 kHz (sine wave)	24 m/12 ms
$S_3$	0	0	LCTR	Period measurement	1 Hz to 20 kHz (pulse wave)	Two periods/one period

The LC72191 general-purpose counter is a 20-bit binary counter.

The value of the counter can be read out, msb first, from the DO pin.

When the general-purpose counter is used for frequency measurement, GT selects the measurement period to be one of two periods, 12 or 24 ms. The frequency of the signal input to the HCTR or LCTR pin can be measured by determining the number of pulses input to the general-purpose counter during the measurement period.

When the general-purpose counter is used for period measurement, the period of the signal input to the LCTR pin can be measured by determining the number of check signal (900 kHz) cycles input to the general-purpose counter during one or two periods of the signal input to the LCTR pin.

The general-purpose counter is started by setting CTEN to 1 in the serial data. While the serial data is acquired internally in the LC72191 at the point the CE signal goes from high to low, the input to the HCTR or LCTR pin must be provided within 2 ms after CE goes low.

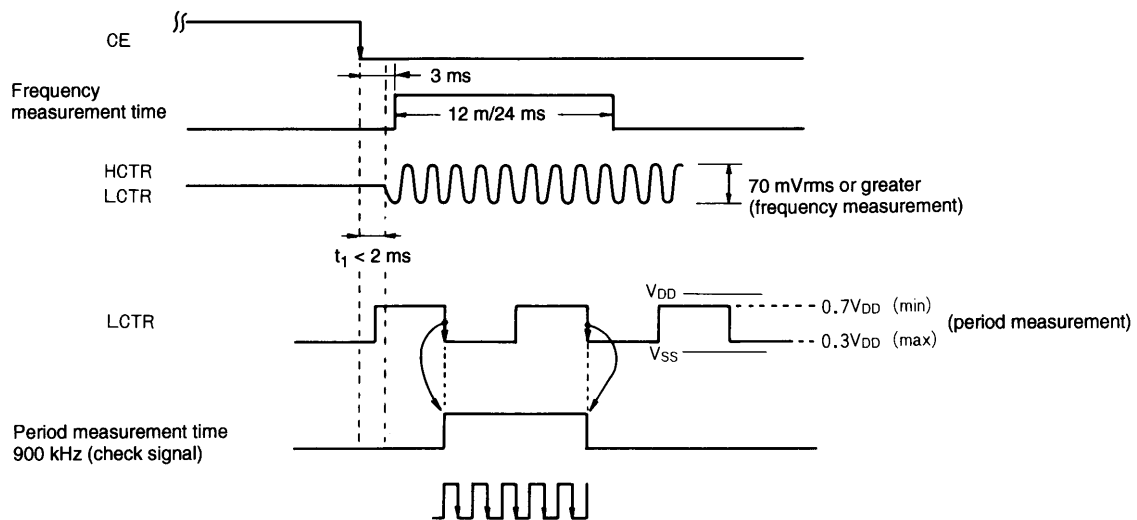
## LC72191, 72191M, 72191JM

Next, the value of the general-purpose counter after the measurement completes must be read out while CTEN is still 1. (The general-purpose counter is reset when CTEN is set to 0.)

Another point that requires care here is that before starting the general-purpose counter, it must be reset by setting CTEN to 0.

Note that although signals input to the LCTR pin are transmitted directly to the general-purpose counter, signals input to the HCTR pin are divided by eight internally before being transmitted to the general-purpose counter. Therefore the value of the general-purpose counter will be 1/8 of the actual frequency input to the HCTR pin.

When counting intermediate frequency signals, always have the controller first check for the presence of the IF-IC SD (station detect) signal and then turn on the IF counter buffer output only when the SD signal is present. Auto-search techniques that use an IF count only are subject to stopping at frequencies where there is no station due to leakage output from the IF counter buffer.



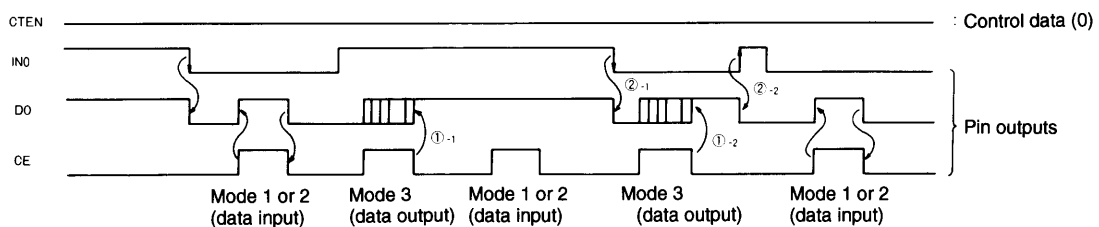
Note that although the DO pin is forced to the high level when the general-purpose counter is started (when CTEN is set to 1), the DO pin automatically goes low when the measurement completes (after either 24 or 12 ms has elapsed or when a signal has been applied for one or two periods). Therefore the DO pin can be used to check for measurement completion.

### Comparison of counting times

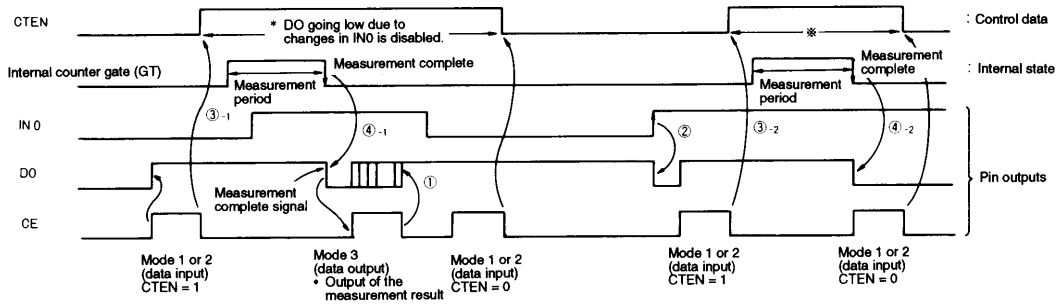
Catalog no.	Measurement time (tG)		Wait time (tW)
	GT = 0	GT = 1	
LC72191/M/JM	12 ms	24 ms	2 to 3 ms*
LC7219/M	60 ms	30 ms	10 to 15 ms
LC7218/M/JM	60 ms	120 ms	10 to 15 ms

Notes: \* The value of the coupling capacitor must be under 1000 pF, since this product has a shorter wait time than the other products.

1. When the general-purpose is not used (when CTEN is 0) the DO pin can be used to check for changes in external signals.

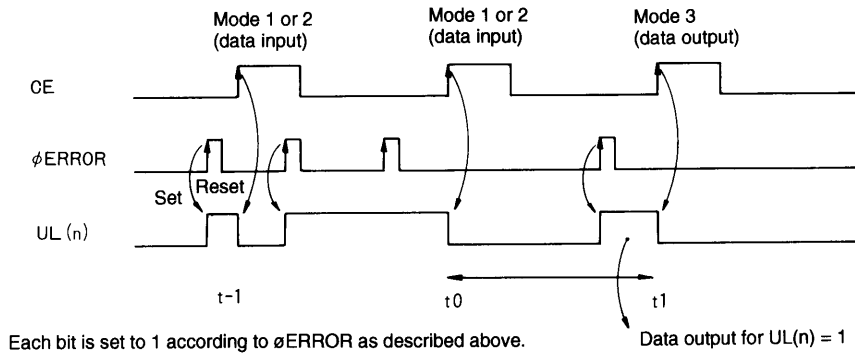


- When mode 3 is specified and data is output through DO, DO will automatically go high after data output has completed, i.e., when CE goes low.
  - After that, DO goes low automatically when the IN0 signal changes state.  
(That is, DO can be used to check for changes in an external signal input to IN0.)
2. When the general-purpose counter is used the DO pin can be used to check for completion of the general-purpose counter measurement.



- When CTEN is set to 1, DO going low due to changes in IN0 is disabled and DO is set high automatically.
- DO is automatically set low when the general-purpose counter measurement completes.  
(That is, DO can be used to check for measurement completion.)

**PLL Unlock Data Read Out Procedure**



The internal data UL(n) is set on the rising edge of phi ERROR  $\uparrow$  and reset on the rising edge of CE  $\uparrow$ . The phi ERROR data UL(n) from before the previous CE  $\uparrow$  rising edge can be read out in mode 3 (data output). In the example above, the data from the period between t<sub>0</sub> and t<sub>1</sub> is read out.

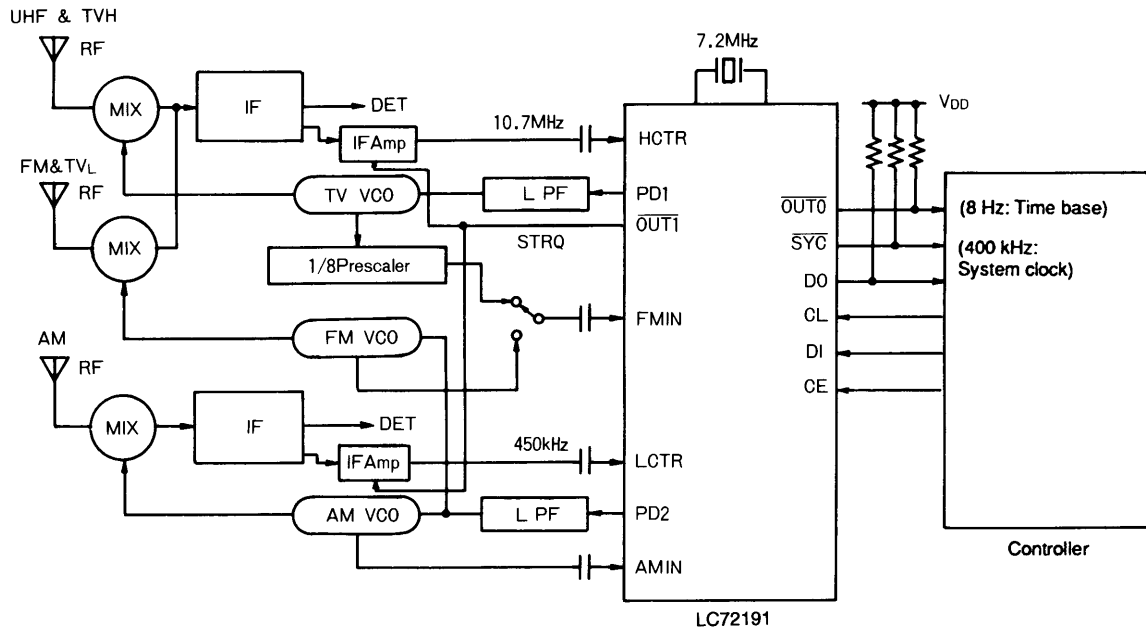
	UL (n)
	3210
0	0000
1	1000
2	1001
3	1011
4	1111

UL0 : 1.11  $\mu$ s }  
 UL1 : 2.22  $\mu$ s } Each bit is set to 1 according to phi ERROR as described above.  
 UL2 : 3.33  $\mu$ s }  
 UL3 : 0.55  $\mu$ s }

phi ERROR: the phase difference (for a 7.2 MHz crystal)

**Sample Application System**

TV/FM/AM (When IF count is performed)



- Note: 1. The coupling capacitors used on the FMIN, AMIN, HCTR, and LCTR pins should be between 50 and 100 pF. However, a 1000 pF capacitor should be used for LCTR if frequencies under 100 kHz are to be used.  
 2. Coupling capacitors should be located as close to their pin as possible.  
 3. When counting intermediate frequency signals, always have the controller first check for the presence of the IF-IC SD signal and then only turn on the IF counter buffer output only when the SD signal is present.

1. TV, 50 kHz steps  
 When the UHF RF = 637.75 MHz (IF = +10.7 MHz)  
 TV VCO = 648.45 MHz  
 PLL fref = 3.125 kHz  
 DV = 1, SP = \* (FMIN selected)  
 Programmable divider divisor  
 Set N = 12969 (decimal).
2. FM, 100 kHz steps  
 When the FM RF = 90 MHz (IF = +10.7 MHz)  
 FM VCO = 100.7 MHz  
 PLL fref = 50 kHz  
 DV = 1, SP = \* (FMIN selected)  
 Programmable divider divisor  
 Set N = 1007 (decimal).
3. AM, 10 kHz steps  
 When the AM RF = 1000 kHz (IF = +450 kHz)  
 AM VCO = 1450 kHz  
 PLL fref = 10 kHz  
 DV = 0, SP = 0 (AMIN, low speed measurement selected)  
 Programmable divider divisor  
 Set N = 145 (decimal).  
 \*: Do not care

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