



ST626x-EMU2

REAL TIME EMULATION DEVELOPMENT TOOLS FOR ST620x/1x/2x/5x/6x MCUs

HARDWARE FEATURES

- Supports ST62 and ST63 family
- Real time emulation
- 32 KBytes of emulation memory
- Breakpoint on a single address or on an address area
- Break events can be defined on Program Space, Data space mixed with up to 4 external signals
- 2 full programmable output for synchronisation
- Read/Write registers on the fly (without wait state)
- Selective trace in Range or Start/Stop
- Break on Stack Overflow
- 1K of real trace memory
- Tracing of up to 32 bits including 4 external signals

SOFTWARE FEATURES

- Symbolic debugger at source level
- On-line assembler/disassembler
- Log files capable of storing any displayed screen
- Command files able to execute a set of debugger commands

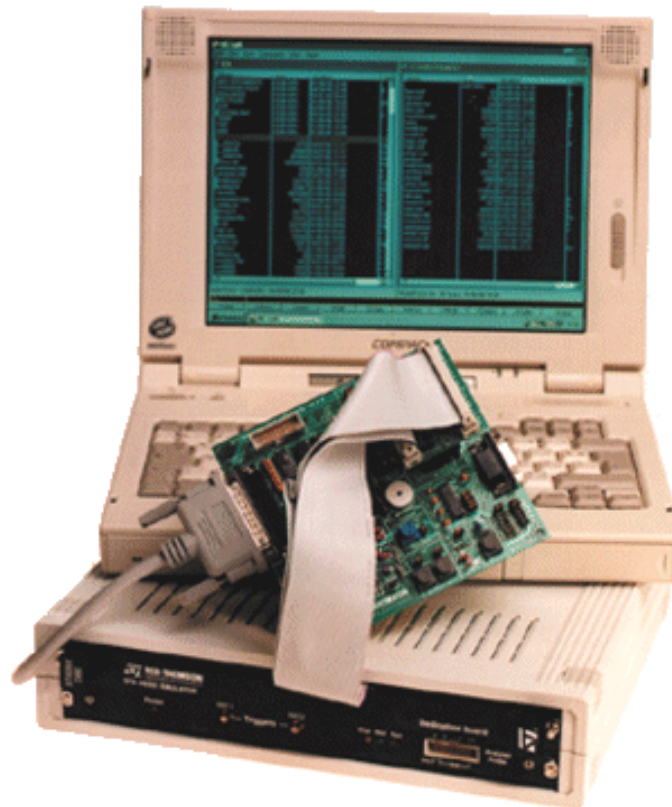


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1 DELIVERY CHECK

This development tool is able to emulate all components belonging to the ST620X/1X/2X, ST625X/6X and to ST629X family.

The dedication board is common for emulating the three families. The choice of emulated ROM Device is made by **properly setting** the configuration on the dedication board, and connecting the **appropriate PROBE** on the **appropriate connectors**.

The development tool is delivered with:

- the ST6 mainframe emulator or the new ST6 HDS2 emulator
- a 5 Volts power supply is added with the new ST6 HDS2 emulator
- 2 flat cables for connecting one of the probes to the dedication board

To emulate ST626X/9X families:

- a **28 pin DIL** emulation probe for **ST625X/6X** and **ST629X** (Ref. DB051 with DIL28 footprint).
- a **20 pin DIL** emulation probe for **ST625X/6X** and **ST629X** (Ref. DB051 with DIL20 footprint).

To emulate ST620X/1X /2X families:

- a **28 pin DIL** emulation probe for **ST620X/1X/2X** (Ref. DB210 with DIL28 footprint).
- a **20 pin DIL** emulation probe for **ST620/1X/2X** (Ref. DB210 with DIL20 footprint).
- a **16 pin DIL** emulation probe for **ST620X/1X/2X** (Ref. DB210 with DIL16 footprint).

Finally, a DIL footprint to SO footprint adapter is also included in the package:

- DB090: a 28 pin **DIL** to 28 pin **SO** adapter
- DB093/20: a 20 pin **DIL** to 20 pin **SO** adapter
- DB093/1: a 16 pin **DIL** to 16 pin **SO** adapter

Instructions for use - Warning

This development tool conforms with the EN55022 emissions standard for ITE, and with generic 50082-1 immunity standards. Then, it complies with the 89/336/EEC directive.

The product is a A Class apparatus. In a residential environment this device may cause radioelectrical disturbance which may require that the user adopts appropriate precautions.

2 ST6 HDS2 NEW MAINFRAME EMULATOR

The new ST6 HDS2 mainframe has been designed to replace the old one.

The main modifications are:

- communication transfer rate: it is now much faster thanks to the use of parallel port.
- dimension and weight: the old 3 boards, basic part of the system, have been redesigned in one board.
- the cost of the overall system has been well reduced

In the second version of ST6 HDS2, (metal box with MB174 main Board) modified for EMC conformity, new features have been introduced:

- Read/Write registers on the fly during execution of program without any wait state.
- Selective record of bus in logical analyser in Range or Start/Stop mode.
- Output OUT1 and OUT2 for synchronisation of an external equipment, programmable in the same way as Selective trace, in Range or Start/Stop mode.

- Stack overflow: a break is automatically generated (by default) in case of stack overflow.

- Break execution: in this new version, the program stops before the execution of the fetch.

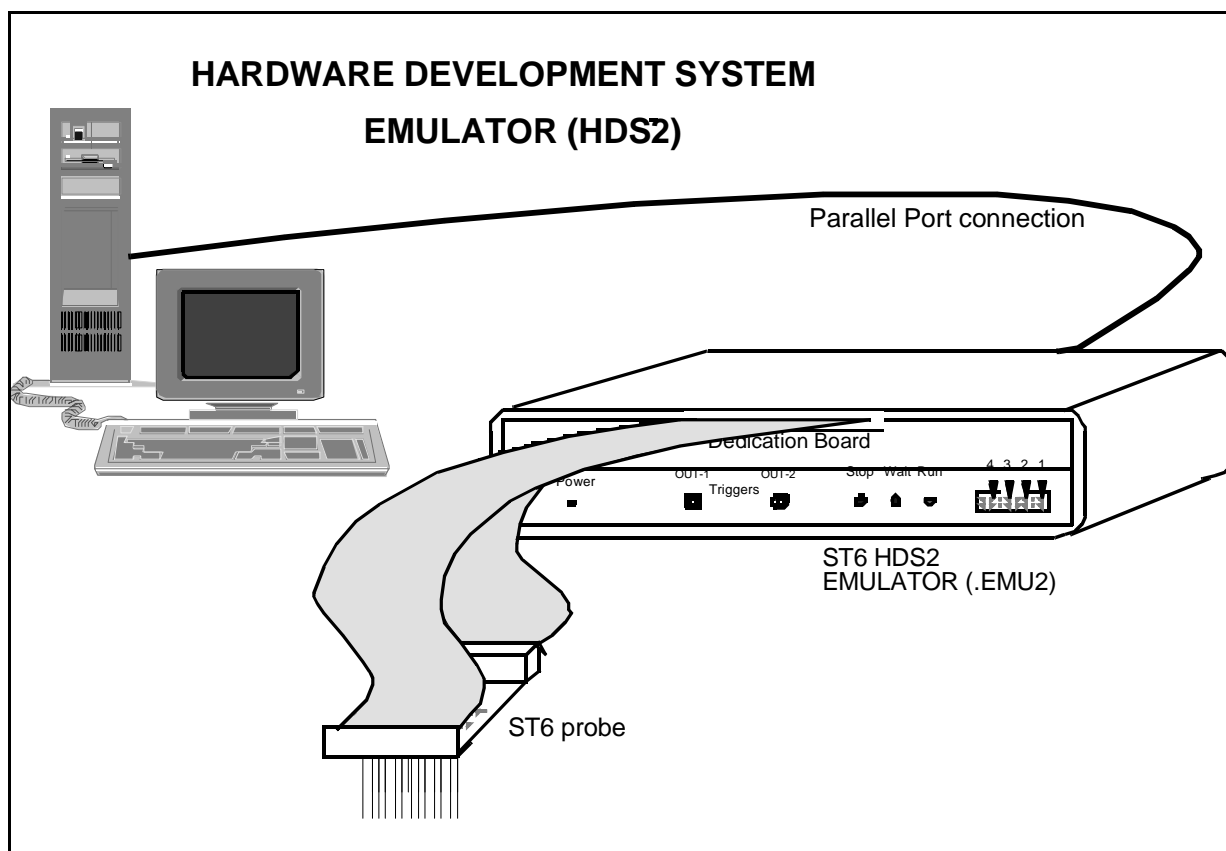
These new mainframes consist of a basic part, common to all ST6 devices, and one ST62 or ST63 sub family dedicated board depending on the specific device to emulate. This new emulator is fully compatible with existing dedicated boards, excepting ST638X and ST631XX which have been designed in 2 boards.

Only the dedicated board (DBE) has to be changed to emulate a new device within the ST62/ST63 sub families.

The use of parallel port allows a very fast communication transfer rate. The symbolic debugger, software part of the real time emulation tool, can be run on a PC, and is common to all ST62 and ST63 devices.

The debugger uses a windowed menu driven interface, and enables the user to set the configuration of the emulator.

Figure 1. Hardware Development System Emulator



2.1 MAIN BOARD

The Main board controls the emulator thanks to a ST9 central processing unit which performs commands coming from host computer through the parallel line.

The board contains, all emulation resources, the core of the ST6, Program ROM emulation, break point, trace memory, automaton and all necessary logic for a real time emulation.

Two connectors, J1 and J2, are used to exchange signals with the interface board.

The amount of program memory in the main board is **factory set at 32k**, in fact the size of the memory depends on the dedication board, which contains the **Program Rom Pagnation Register (PRPR)** if it exists (no PRPR for memory size lower than 4k).

No configuration jumpers are required.

2.2 ST6 HDS2 MAIN BOARD

On the rear panel there is:

- a power plug to connect power: 5 Volts 3 Amp min. (The delivered power is 100 volts to 240 volts input and 5 Amp output).
- a power switch.
- a parallel connector for an IBM PC(TM) compatible.

On front panel:

- a led "POWER ON" signal.
- OUT 1 and OUT 2 signals which can be used for synchronizing an external equipment.
- 3 leds indicating when the ST6 core is in "STOP", "WAIT" or "RUN" mode.
- a 16 pin connector for data acquisition signals. The explanation of these signals is done in the debugger manual.

2.2.1 External output: OUT1 and OUT2

For debugging hardware it is very useful to have synchronization signals. The goal of the outputs 1 and 2 is to offer this feature to the user. They can be programmed differently whether the debugger used is the DOS debugger ST6NDB or the Source Level Debugger WGDB6, as explained in the two following paragraph. They are full programmable with WGDB6.

Output OUT1 and OUT2 under ST6NDB

When using old DOS Version of debugger ST6NDB:

This feature is programmable thanks to Hardware Breakpoint Menu. The breakpoint MENU allows to define breaking events. These events will generate an actual breakpoint only if break enable is ON. When break is off, these events are existing in the development tool. In the HDS2 emulator version up to 4.3, the signals OUT1 and OUT2 are connected to these internal breaking events. Therefore these signals can be used to synchronize an external device while running (breakpoint off).

Output OUT1 and OUT2 under WGDB6

When using WGDB6 new Version of debugger at source level under Windows™ :

This feature is full programmable thanks to Hardware Events/Trigger Menu. Output OUT1 and OUT2 can be programmed in two ways:

- Events for synchronisation: it allows to the user to preset pulses synchronisation for an external equipment. The events can be defined by addresses or by range of addresses.
- Events for Timing Measure: it allows to the user to measure time elapsed during a subroutine for example. In this case, output OUT2 is SET on a user defined address, and RESET on an other one, OUT1 is the ST6 clock cycle gated by OUT2.

These 2 functioning modes are clearly displayed on screen.

2.2.2 Data acquisition signals

In a same way as are recorded Buses, Flags, Bank registers in the trace memory, the ST6 HDS2 offers to the user the possibility to record 4 external signals. These signals must be connected on the pin of the Analyser probe connector on the front panel of the HDS2, as shown below.

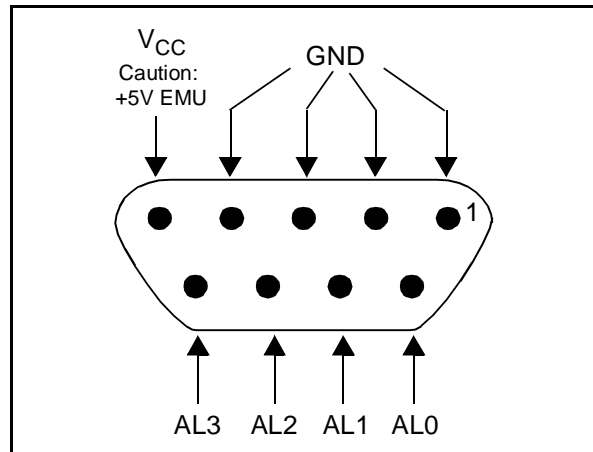
These inputs are CMOS compatible at 5 Volts.

2.2.3 LEDs RUN, STOP, WAIT

Three leds have been added to indicate to the user the state of the core or of the development tool during emulation.

When user's program is running (in real time), led **RUN** is on.

When **ST6 core** is in **WAIT** mode, led **WAIT** is **ON**.



When **ST6 core** is in **STOP** mode, both leds **STOP** and **WAIT** are **ON**.

2.3 INSTALLING THE PROBE:

Before installing the probe, the user must choose the device to be emulated: **ST620x/1x/2x** or **ST625x/6x** or **ST629x**

Then,

- Connect the 2 flat cables on the appropriate connectors, if the board is inside the main frame, **unscrew** the 2 screws on each side of the dedication board, and **press outward** on the **release buttons** to extract the board.
- The connectors are **J1** and **J2** for **ST625X/6X** and **ST629X** family (printed on board).
- The connectors are **J3** and **J4** for **ST620X/1X/2X** family (printed on board).

To prevent mistakes, a bump on connectors impose to set them right.

Furthermore, we can verify that the **pin 1** for each connector, which is clearly printed on both boards, is on the **same side** as the **red line** on the flat cables.

Then connect the chosen probe on the opposite side of the flat cables, with respect to the pin 1 of each connector.

Schematics of these probes are shown in annex.

The ST620X/1X/2X probes emulate the oscillator function if the jumper on the probe is set on crystal. If set on OSCIN, a clock must be given on OSCIN input. To use this clock issued from probe, the dedication board must be set on external clock.

2.4 INSTALLING AN ST6 EMU2 DEVELOPMENT TOOL

When receiving a **whole development tool**, the **dedication board** is delivered **inside** the mainframe.

The user has just to:

- connect the power supply to the mains(100 to 240 volts).
- connect the output (5Volts) of power supply on the DIN connector of the rear panel
- connect the parallel cable between the parallel connector and the host computer.

2.5 INSTALLING A ST626X-DBE DEDICATION BOARD IN AN ST6 HDS2

If there is already a dedication board in the development tool, the user has simply to:

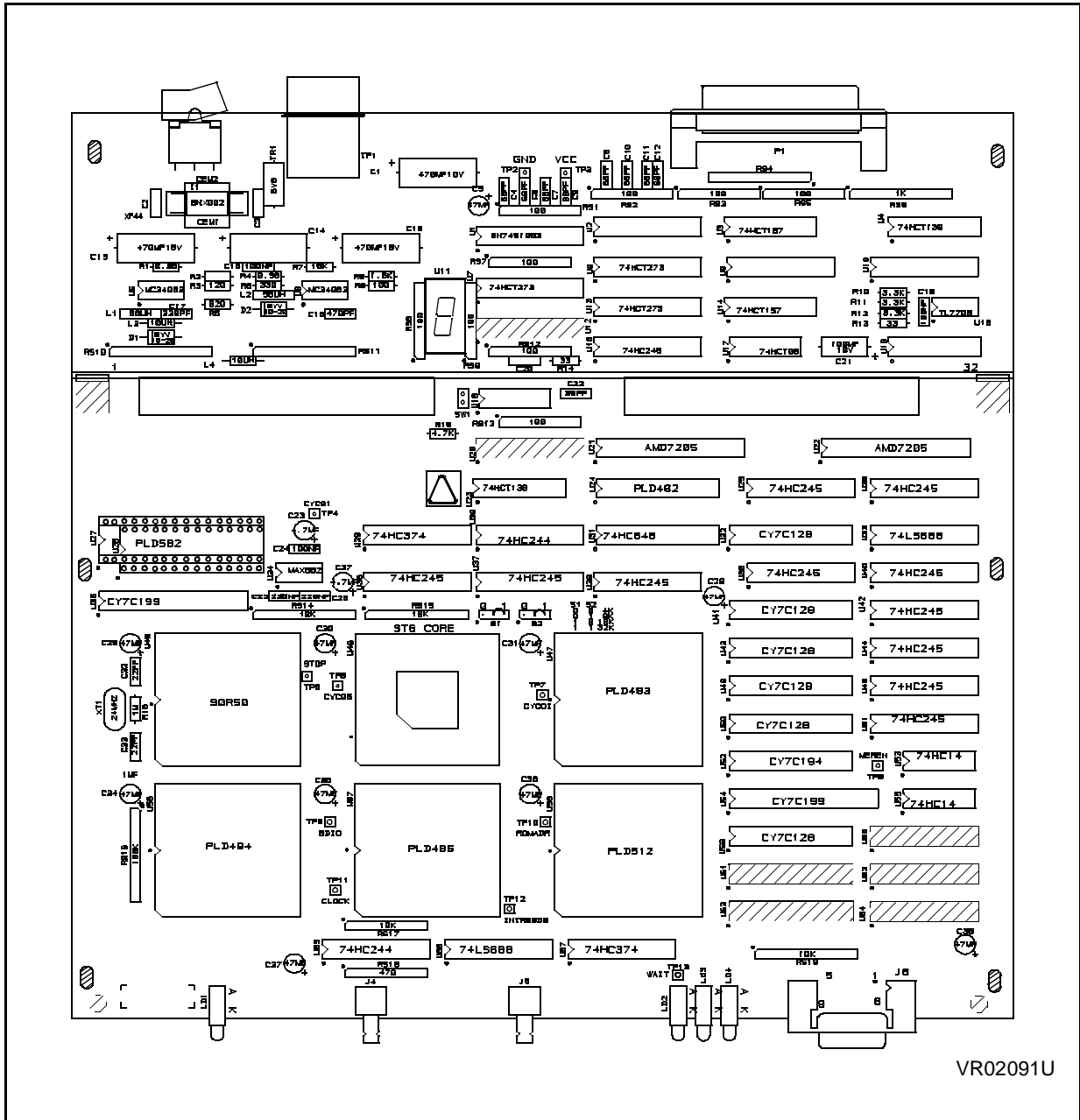
- **unscrew** the 2 screws on each side of the dedication board, and **press outward** on the **release buttons** to extract the board.

Then insert the new dedication board in the **guide rods** and **push** it hardly in the backplane, and:

- **screw** the 2 screws on each side of the dedication board.

ST626x-EMU2 - ST6 HDS2 NEW MAINFRAME EMULATOR

2.7 COMPONENTS LAYOUT OF ST6 MAIN BOARD (MB174)



VR02091U

3 ST6 MAINFRAME EMULATOR (FIRST GENERATION)

The ST6 mainframe emulator contains positions for 5 boards:

- Mother board (CLZ80) must be inserted on the first (bottom) position
- Real time board (GPFM/3) must be on second position
- interface N (DB014) must be inserted on third position
- dedication board ST620X/1X/2X/5X/6X/9X-DBE (MB064) inserted in one of the two top position

On the rear panel there is:

- a main-power selector to select 110 volts or 220 volts.
- a power plug
- a power switch

On front panel:

- the RS232 connector to link the emulator with an IBM PC
- EXT-SIG connector that allows you to choose between 3 groups of 4 signals to be memorize on trace memory. These signals are independent from the probe data acquisition signals. The explanation of these signals is done in the debugger manual
- Mother board reset push button
- ST6 INT push-button

3.1 MOTHER BOARD (CLZ80)

The mother board (CLZ80) controls the mainframe emulator and it is linked to an IBM PC through an RS232 line. On this board only 2 connectors are used:

- J5 connected to the front panel RS232 25 pin connector
- J4 connected to the front panel mother board reset push-button

3.2 REAL TIME BOARD (GPFM/3)

Real time board (GPFM/3) contains the emulation resources:

- ROM Program emulation, break point, trace memory.
- Two connectors, J3 and J4, are used to exchange signals with the interface board.

When emulating ST62XX or ST63XX, the interface board is an N-WELL interface board.

The two connectors are used.

For emulating components of other families, the interface board can be a P-WELL interface board: in this case only one connector is used, the jumpers of W2 must be plugged.

JUMPERS SETTING for ST62XX and ST63XX emulation:

W1:

All jumpers must be removed.

W2:

One jumper only must be set to link pin 1 to pin 16.

CONNECTORS:

J3 and J4:

Used to link this board with the N-WELL interface board.

J5:

Used to connect the data acquisition probe.

ST626x-EMU2 - ST6 MAINFRAME EMULATOR (FIRST GENERATION)

3.3 INTERFACE BOARD

The interface board emulates the CPU-core.

JUMPERS SETTINGS:

S1:

- not used in emulation mode
- allows the definition of the type of EPROM (27256/27128) used in stand-alone (without CLZ80 and GPFM/3 boards) mode

S2, S3: size of emulation program ROM

The position reference names depend on the version of the board. For S2 they can be identified as 0 and 1 or OLD and NEW on the board.

For S3 it can be 0 and 1 or 4K and 8K.

S2	S3	Size	Comment
0 or OLD	0 or 4K	4K	
0 or OLD	1 or 8K	8K	
1 or NEW	0 or 4K	16K	normal setting
1 or NEW	1 or 8K	32K	not supported

The purpose of this jumper is to allow the emulator to check the amount of emulation program ROM that is used.

TEST/NO TEST: must be in NO TEST position

CONNECTORS:

J1 and **J4** to link this board to GPFM/3 board.

J2: receives signals from J1-EXT SIG. connector situated on the front panel of the ST6 emulator.

J3: is connected to ST6-RESET, ST6-INT push-buttons, STOP-LED and WAIT-LED situated on the front panel of the ST6 emulator.

3.4 ST626X-EMU DEVELOPMENT TOOL

When receiving a **whole development tool**, the **dedication board** is delivered **inside** the mainframe, it is plugged in one of the two top position in the backplane.

First of all, it is mandatory to verify the mainframe:

- remove the 2 screws on the rear panel of the main frame
- lift the lid on the side of the rear panel
- pull the lid from the rear panel, it dissociates it from the front panel
- remove the lid, pay attention to the wire for the ground connection

Verify that all boards are correctly inserted in the backplane of the mainframe in the right order:

- CLZ80 board must be inserted on the first (bottom) position
- GPFM/3 board must be on second position
- Interface N (DB014) must be inserted on third position
- The two top positions are intended to receive one or a couple of dedication boards in order to emulate **one family** of component: in this case, only the **ST626X-DBE board** must be in **one of the two top positions**.

3.5 INSTALLING ST626X-DBE DEDICATION BOARD

When receiving only a dedication board, the user must install his dedication board as described below.

Open the main frame by removing the lid:

- remove the 2 screws on the rear panel of the main frame
- lift the lid on the side of the rear panel
- pull the lid from the rear panel, it dissociates it from the front panel
- remove the lid, pay attention to the wire for the ground connection

Then **remove the dedication board or the two dedication board** which are plugged in the two top position of the backplane, which was for emulating an other family of STMicroelectronics devices.

After that, plug the new dedication board in one of the two top positions of the backplane.

3.6 INSTALLING THE PROBE

Before installing the probe, the user must choose the device to be emulated, please refer to 4.2.1 chapter.

Then,

- Connect the 2 flat cables on the appropriate connectors.

The connectors are **J1** and **J2** for **ST625X/6X** and **ST629X** family (printed on board).

The connectors are **J3** and **J4** for **ST620X/1X/2X** family (printed on board).

To prevent mistakes, a bump on connectors impose to set them right.

Furthermore, we can verify that the **pin 1** for each connector, which is clearly printed on both boards, is on the **same side** as the **red line** on the flat cables.

- Then, remove the 2 screws which are holding a small metal cover on the bottom of the development tool.

- Stick the flat cables through this new opening.

Then connect the chosen probe on the opposite side of the flat cables, with respect to the pin 1 of each connector.

4 DEDICATION BOARD (DBE)

This board contains the specific functions for ST620X/1X/2X, ST625X/6X and ST629X emulation :

- Oscillator
- EEPROM (Byte mode and parallel mode)
- RAM
- Timer A
- Timer 2
- Watchdog
- Analog to Digital Converter
- Serial Peripheral Interface
- Analog to Digital Converter
- Port A: 8 Bits
- Port B: 8 Bits
- Port C: 8 Bits (one part for ST625X/6X, ST629X, the other for ST620X/1X/2X)
- Low Voltage Inhibit
- Pagination Registers

A white dot indicates the position 1 for all jumpers and components on the board.

Note for the **VCC pin**:

When the input power pin VCC is connected, this input is used as a **reference voltage** by the emulator.(please refer to [Figure 4.1](#) chapter)

No power is given or taken at this pin by the emulator.

Notes on **write-only registers**:

Several Data Space registers of the emulated ROM device are write-only, however, to offer more flexibility to the user, they are readable when commands such as “watching register” are used.

4.1 VOLTAGE FUNCTIONING RANGE

This board has been designed to emulate the ROM device in the range of 3 to 6 Volts.

When the input power **VCC pin** is connected, this input is used as a **reference voltage** by the emulator. This reference voltage is buffered thanks to an operational amplifier and an emitter follower for powering the output buffers, and for giving the high reference voltage to the ADC.

Then all the outputs of the peripherals are fully compatible at CMOS level with an application which is powered in the range from 3 to 6 Volts.

When this input is not connected, all buffers are powered with 5 volts.

No power is given nor taken at this pin by the emulator.

4.2 JUMPER DESCRIPTION ON DEDICATION BOARD

Jumpers on the board are used to select the amount of MEMORY, the emulated PERIPHERALS, and metal MASK OPTION of the ROM device.

This chapter explains how to select these features.

Note for **ST620X/1X/2X**:

The difference between ST620X/1X and ST622X is only about the size of ROM and A/D presence.

As the Development Tool offers the maximum of ROM, the choice will be always a device of the **ST622X** family.

4.2.1 Choosing the emulated device: W7

This board has been designed to emulate 3 families of ST6 components: ST621X/2X, ST626X and ST629X.

The choices are different whether ADC and SIO are used, or Pin 23 or Pin 17 respectively is NMI or CKOUT, or with the amount of DATA space memory.

To select this choice, only one jumper must be set on W7 in front of the name of the name of the device, clearly printed on the board.

When a peripheral is not used, for example SIO for ST6292, registers of this peripheral are at zero value, and they cannot be written.

4.2.1.1 Emulating ST621X/2X family: J3 and J4

To emulate a ROM device of the **ST621X/2X** family, a ST621X/2X probe must be connected on **J3 and J4** through the flat cables.

There is one probe for emulating 28 pins ROM devices (DB031), and one probe for emulating 20 pins ROM devices(DB030).

J3 of the dedication board must be connected on **J1** of the probe.

J4 of the dedication board must be connected on **J2** of the probe.

The number of the pins are clearly printed on both boards, and the red line on the flat cables must be on the same side of the 1 of the connectors.

4.2.1.2 Emulating ST626X or ST629X family: J1 and J2

To emulate a ROM device of the **ST629X or ST626X** family, the corresponding probe must be connected from **J1 and J2** of the dedication board to **respectively J1 and J2** of the probe, through the flat cables.

The 28 pins probe emulate 28 pins ROM devices, the 20 pins probe emulate 20 pins ROM devices.

The following table shows the difference between emulating ST626X or emulating ST629X.

Emulated Device	Jumper on W7	NMI/CKOUT	ADC/SIO	SPI	Data Space Memory
ST6293/94	ST6293/94	CKOUT	YES	YES	1 RAM Bank (0->3F) 2 EEPROM BANK (0->3F)
ST6291/92	ST6291/92	CKOUT	NO	NO	EEPROM (0->2F)
ST6260/65	ST6260/65	NMI	YES	YES	1 RAM Bank (0->3F) 2 EEPROM BANK (0->3F)
ST6263*	ST620/65	NMI	YES	NO	1 RAM Bank (0->3F) 1 EEPROM BANK (0->3F)
ST6253*	ST6260/65	NMI	YES	NO	1 RAM Bank (0->3F) 0 EEPROM BANK

* Be careful not to try to emulate the SPI on ST6253/63 and also the EEPROM on ST6253 as those peripherals don't exist on these devices

4.2.2 Mask option on Port B: W3 and W4 for ST626X and ST629X

There is two option bits for the state of the bit port PB0, PB1, PB2, PB3 during RESET.

This state can be input with pull-up or high impedance.

The option byte 4 is for both PB0 and PB1, the other, option Byte 5, is for PB2 and PB3.

OPT4: Option Byte 4

When the jumper is between 1 and 2 the option is 0: Pull-up during reset for PB0 and PB1.

When the jumper is between 2 and 3 the option is 1: high impedance during reset for PB0 and PB1.

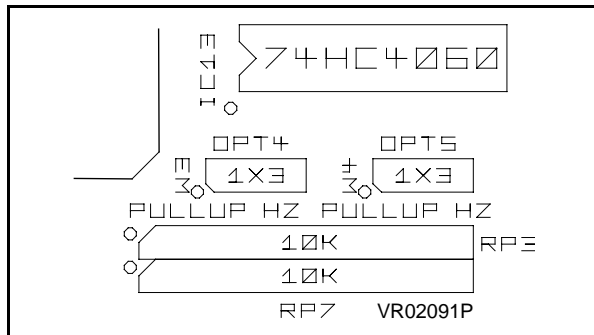
OPT5: Option Byte 5

When a jumper is between 1 and 2 the option is 0: Pull-up during reset for PB2 and PB3.

When a jumper is between 2 and 3 the option is 1: high impedance during reset for PB2 and PB3.

The **factory setting** for these jumpers is: **Pull-up** during reset.

When emulating **ST621X or ST622X** these jumpers are **ignored**.



4.2.3 Hardware WATCHDOG selection: W1

The jumper W1 permits to emulate the “hardware WATCHDOG” metal mask option of the ROM device.

The watchdog can be activated in two ways in the ROM device:

- The software Watchdog is activated by setting, by software, bit 0 of the watchdog register.
- The other way is to be in “watchdog HARD”, it means the watchdog is automatically armed after RESET (generated by watchdog or not).

Jumper setting:

- 1-2: Watchdog is automatically activated by HARDWARE
- 2-3: Watchdog is only activated by SOFTWARE

The jumper setting is clearly printed on board as shown in the following figure 3.

Note:

When activating watchdog, STOP instructions are automatically executed as WAIT instructions by the processor, see following chapter for special use of STOP mode.

4.2.4 MIXT option: Wake UP by NMI in STOP mode

A special option is to effectively execute STOP mode when encountered, and to wake up from this STOP mode by using NMI pin.

This feature is only available when ST6223/24, or ST626X when MIXT option is selected.

When this feature is selected, even if watchdog has been activated (Hard or soft), STOP instructions are effectively executed, when pin NMI is HIGH.

If pin NMI goes low, or was low before executing STOP, STOP instructions are converted in WAIT instructions.

Jumper setting W7:

Two ways:

- Select ST6223/24 clearly printed on board
- Put a jumper between pin 3 and 4 pin of W7 and select ST6260/65 clearly printed on board.

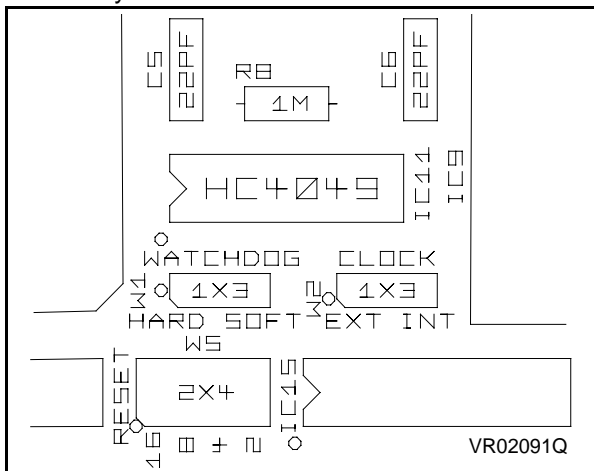
4.2.5 Clock Source Selection: W2

The system CLOCK can be chosen between internal on board oscillator and pin OSCIN (or XTAL) input of the probe.

This jumper setting is clearly printed on board, with **INT** for INTERNAL clock and **EXT** for EXTERNAL clock.

Jumper setting:

- 1-2 In this case the external clock is selected: it means the Clock issued from the probe is selected.
- 2-3 The internal clock is selected. In this case the internal clock is made thanks to an oscillator with a quartz, this quartz XT1, can be exchanged if desired by the user.



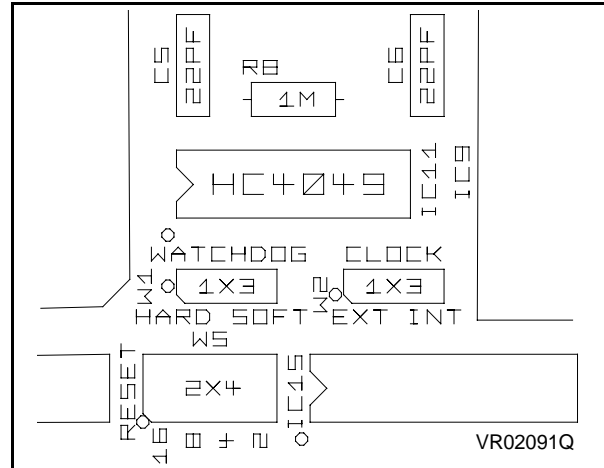
4.2.6 Reset delay duration: W5

For as long as the reset pin is kept at the low level, the processor remains in the reset state.

After the pin reset has been released, a counter provides a delay between the detection of the reset high level and the release of the MCU reset: a jumper on W5 permits to select the duration of this delay.

The standard delay is 2048 oscillator cycles: the jumper must be in front of 2.

For delay of 4096, 8192 or 16384 the jumper must be in front of respectively 4, 8, or 16, clearly printed on the board.



Note for CLOCK "issued from the probe":

If the user uses a probe made by STMicroelectronics, this probe is able to send a clock to the dedication board in two ways thanks to a jumper:

- a clock made by the on board oscillator on the probe.
- a clock directly issued from the application. In this case the signal on OSCIN must be at CMOS level.

When oscillator is not used, it is mandatory to disable the oscillator by putting a jumper on "oscillator disable" (factory setting).

WARNING on probe on board oscillator:

Probe: The "open" schematic of this probe permits to the user to reconstruct on the probe, the same oscillator as on his own application. The probe is able to support a cristal or a resonator 3 pins with or without capacitor, it can be of course used also with an RC.

PROBE: Installing the ferrite coil for EMC compatibility

To be conform to the EMC directive, particularly in emission, the delivered ferrite coil must be placed as follow:

- 1) Place each part on each side of the flat cables
- 2) Place the metal clip to fix them together

4.3 EMULATED PERIPHERALS

4.3.1 Oscillator

For the ST621X/2X it is a standard oscillator as described in the data sheet of the ROM device.

For ST626X and ST629X, the four bits of the oscillator control write only register 0DCH are emulated, including RC oscillator frequency control (if Bit2=1 then Fosc is approximately divided by 100), but the pin XTAL and EXTAL are respectively input and output clock for the emulator, according to **W2** selector.

These two pin XTAL and EXTAL **do not emulate an actual oscillator**, on which it can be connected a crystal or an RC.

4.3.2 Mapping

Program memory size is always valid up to 4 k Bytes (0FFFH)

Data space memory size depends on the emulated device.

The mapping of data space can be different in two ways: there is bank memory in the range 0 to 03FH or not.

- No Memory Banks: case of ST6291, ST6292.
- In this case, there is **always** EEPROM from 0 to 02FH, and nothing from 30 to 3F.
- The Memory Bank Register (0E8H), is at 0 value, and it is not possible to write it.
- Memory Banks exist: case of ST6293, ST6294, ST626X.
- In this case the range from 0 to 03FH is fully used through the content of the Memory Bank Register located in 0E8H (write only).
The meaning of each one of these bits is:
Bit 0 if set selects the first EEPROM bank
Bit 1 if set selects the second EEPROM bank
Bit 4 if set selects the RAM bank.
The others are not used and not existing.

Care must be taken that only one of these three bit must be set at a time, for more details see Data Sheet of the corresponding ROM device.

4.3.3 Timer A, Timer 2, Watchdog

Clock of these devices are voluntarily validated only during emulation, it provides to see the evolving values of them. Therefore pay attention that in NEXT mode the values of counters can be slightly different of a real time session because of setting ON and OFF emulation.

For using these peripherals, please, refer to data sheet of the corresponding ROM DEVICE.

4.3.4 Analog to Digital Converter

This peripheral is available only when one component of **ST620X/1X/2X, ST629X or ST625X/6X** family, which contains ADC, has been selected with W7 jumper.

Except these devices, ADC registers are at zero value and are not able to be written.

The ADC input can be connected at one of the 13 inputs, the 8 of port A and the 5 of port C, by properly programming the registers of these ports (one at a time). If more than one ADC input are selected, they will be short circuited each other's.

The analog to Digital Converter converts the input value in about 50µS at 8 Mhz of Xtal clock. Clock conversion is always present, it means that a data conversion is always accomplished after writing a start conversion even if it is made in NEXT mode of emulation.

It allows to the user to convert analog input step by step.

Note on ADC **voltage reference**:

The **high voltage reference** for the ADC is the applied voltage on the **pin VCC** internally buffered in the board.

The **low voltage reference** is the **GROUND**.

Then to have a conversion result of 0FFFH, the voltage at the analog input must be equal to the voltage of the VCC pin.

4.3.5 Serial Peripheral Interface (SPI)

This peripheral is available only when one of **ST6293, ST6294 or ST626X** has been selected with W7.

For other devices, SPI registers are at zero value and are not able to be written.

The Serial Peripheral Interface, when validated, is always active: it means clock and data do not depend whether on the system is in step by step mode or not.

For using this peripheral, please, refer to Data Sheet of the corresponding ROM device.

Note: to use this peripheral, do not forget to set bit 1 of LVI register...

4.3.6 Port A

This port is always selected whatever is the emulated device, and if ADC is permitted (see 3.3.4 chapter), each input of this port can be an ADC input (one at a time).

The functioning mode of each 8 input is selected by properly programming the three associated registers: Data Register (DRA), Data Direction Register (DRB), Data Direction Register (DDRB), and Option Register (DDRA), and Option Register (ORA) as follow.

DDR	OPR	DR	I/O Mode
0	0	1	Input without pullup, interrupt disabled
0	1	0	Input with pullup, interrupt enabled
0	0	0	Input with pullup, interrupt disabled
0	1	1	Analog Input
1	1	X	Push Pull Output
1	0	X	Open Drain NMOS output

Beware of **mixing input and output modes** in the same port, in this case, do not use SET or RES instructions on Data Registers:

When a port bit is in input mode, the data read is the state of the pin of the device (or the probe); when a port bit is in output mode the data read is the data register, so when using a read/modify/write instruction, a bit port mode can be changed from input mode to analog input mode unintentionally!

For more details about this peripheral, please, refer to Data Sheet of the corresponding ROM Device.

4.3.7 Port B

This port is always selected, the functioning mode of his 8 input is selected by properly programming the three associated registers: Data Register (DRB), Data Direction Register (DDRB), and Option Register (ORB) as follow.

DDR	OPR	DR	I/O Mode
0	X	1	Input without pullup, interrupt disabled
0	1	0	Input with pullup, interrupt enabled
0	0	0	Input with pullup, interrupt disabled
1	1	X	Push Pull Output
1	0	X	Open Drain NMOS output

Beware of **mixing input and output modes** in the same port, in this case do not use SET or RES instructions on Data Registers:

When a port bit is in input mode, the data read is the state of the pin of the device (or the probe); when a port bit is in output mode the data read is the data register, so when using a read/modify/write instruction, a bit port mode can be changed from input mode to analog input mode unintentionally!

For more details about this peripheral, please, refer to Data Sheet of the corresponding ROM Device.

4.3.8 Port C

This port is always selected, and if ADC is permitted (see 3.3.4 chapter), each input of this 8 bit port can be an ADC input (one at a time).

The functioning mode of each 8 input is selected by properly programming the three associated registers: Data Register (DRC), Data Direction Register (DDRC), and Option Register (ORC) as follow. Bit PC0 to PC4 are used for ST626X/9X, PC4 to PC7 are used for ST621X emulation.

DDR	OPR	DR	I/O Mode
0	0	1	Input without pullup, interrupt disabled
0	1	0	Input with pullup, interrupt enabled
0	0	0	Input with pullup, interrupt disabled
0	1	1	Analog Input
1	1	X	Push Pull Output
1	0	X	Open Drain NMOS output

Beware of **mixing input and output modes** in the same port, in this case, do not use SET or RES instructions on Data Registers:

When a port bit is in input mode, the data read is the state of the pin of the device (or the probe); when a port bit is in output mode the data read is the data register, so when using a read/modify/write instruction, a bit port mode can be changed

from input mode to analog input mode unintentionally!

For more details about this peripheral, please, refer to Data Sheet of the corresponding ROM Device.

4.3.9 Low Voltage Inhibit, Pin VCC (LVI)

Pin VCC on the probe is an input for LVI system, and do not furnish any power to the application.

A low Voltage inhibit system permanently watches Pin VCC on the probe. It generates a RESET when pin VCC goes under 2.5 Volts threshold and releases it when it goes over 3 Volts, at the same time bit 7 of LVI register (ODDH) is set to one.

For more details about this peripheral, please, refer to Data Sheet of the corresponding ROM Device.

4.3.10 NMI/CKOUT

The NMI/CKOUT PIN, pin 23 for 28 Pin package, pin 17 for the 20 pin package, can be either NMI entry or CKOUT output depending on the selected device (see 3.3.1 chapter).

It is NMI input for ST626X family, and CKOUT for ST629X.

When NMI is selected, the pin is the Non Maskable interrupt input for UC.

When CKOUT is selected, the pin is an output clock whose the frequency is clock on XTAL divided by 2.

CKOUT output is controlled by bit 3 of Oscillator Control Register (ODCH):

If bit 3 is set: CKOUT is low

If bit 3 is reset: CKOUT = $F_{osc}/2$

For more details about this peripheral, please, refer to Data Sheet of the ROM Device.

5 TROUBLESHOOTING

5.1 - AT POWER UP

At the beginning of an emulation session, on screen of PC must appear the debugger message, with "WAIT" during software connection establishment.

If a "TIMEOUT" message is encountered, there is a connection problem, which can come from one of these reasons:

- when using ST6HDS2
 - ST6 development Tool is not power ON
 - The parallel line is not well connected
- or when using old main frame:
 - verify that the delivered cable is actually connected directly to the Main Frame.
 - and if necessary there is another cable which is either a "wire to wire" connection or a 25 to 9 pin adaptor.
 - The serial line is not connected to the right I/O port of the computer.

5.2 DURING EMULATION

During emulation: Problem with program Counter

In case of "Check Hardware Jumpering" or wrongly executing code in step mode:

Most of the time, this problem occurs with HDS1 emulator or with HDS2 plastic BOX up to 4.3 version, it is coming from that the development tool is in RESET state, it can be caused by:

- The application where probe is connected is not powered on, then the schmitt trigger on pin Reset is active and causes the RESET
- The pin Reset of emulated device is at low level
- A probe is connected, but is not powered either by an application or by a voltage on the VCC input.

For properly emulating RESET please refer to the following chapter.

During emulation: Reset emulation

With ST6HDS2 new metal box, it is now possible to begin an emulation session even if application is off, it is required particularly in MONITOR or TV applications.

With old ST6 HDS1 emulator, or with HDS2 plastic BOX up to 4.3 Version, if the application requires that software must be executed just after power ON, it is mandatory to proceed as follow:

- not connect, or remove probe from application.
- power ON emulator.
- begin emulation session: load program.
- then start execution of program in Real Time.
- plug the probe in the application (which is off), at this time the ST6 emulator is in reset state, because Reset and VCC pins are at low level.
- Power ON the application, then the execution of software will start.

5.3 DISCREPANCIES BETWEEN EMULATOR AND ROM OR EPROM DEVICE

When some differences of behaviour are appearing between the emulator and the ROM device, in most cases, it comes from **using read/modify/write instructions** on:

- registers which are **only writable**.
- registers in which **some bits** are **writable**, and some bits **readable**.

For these registers, trouble are caused, because when reading, a random value is read by the CPU, after calculating the mask, this random value is written in the register, changing it unintentionally!

The same problem can occur with registers, where some bits have a different function during writing or during reading.

Example for **Ports**:

When **reading** a bit port in **input** mode, the read **value** is the **level** of the pin.

When **reading** a bit port in **output**, the read **value** is the value of the corresponding bit in the **Data Register**.

The user has to **check** if each used register is correctly accessed.

The principle ST6 registers, with which care must be taken, are listed below:

- The EEPROM control registers
- The control registers of SPIs
- The Data registers of the 3 Ports A, B and C
- Analog to Digital Converter Control Register
- The Interrupt Option Register
- The Program Rom Pagination Registers
- The Data RAM/EEPROM Banking Register
- The Data ROM window Register

5.4 AVOID THE MOST FREQUENT PROBLEMS WHEN PROGRAMMING ST6 MICROS!

5.4.1 Execution of Interrupt

If interrupt are not executed, in most cases, it comes from:

- The core is not in normal mode: after **RESET** the core is in **NMI mode**, to enter the **normal mode** which let execute interrupt, the core must execute a **RETI** instruction.
- The global enable interrupt bit has not been SET, or has been unintentionally cleared, then the IOR register must be checked. The default value to enable Interrupts is 010H.
- The enable interrupt bit of the desired peripheral has not been SET, or has been unintentionally cleared.
- The Interrupt Option Register is **write only**, and has been wrongly written by a read/modify/write instruction, only **LDI** is **permitted**.

5.4.2 Execution of WAIT and STOP instructions

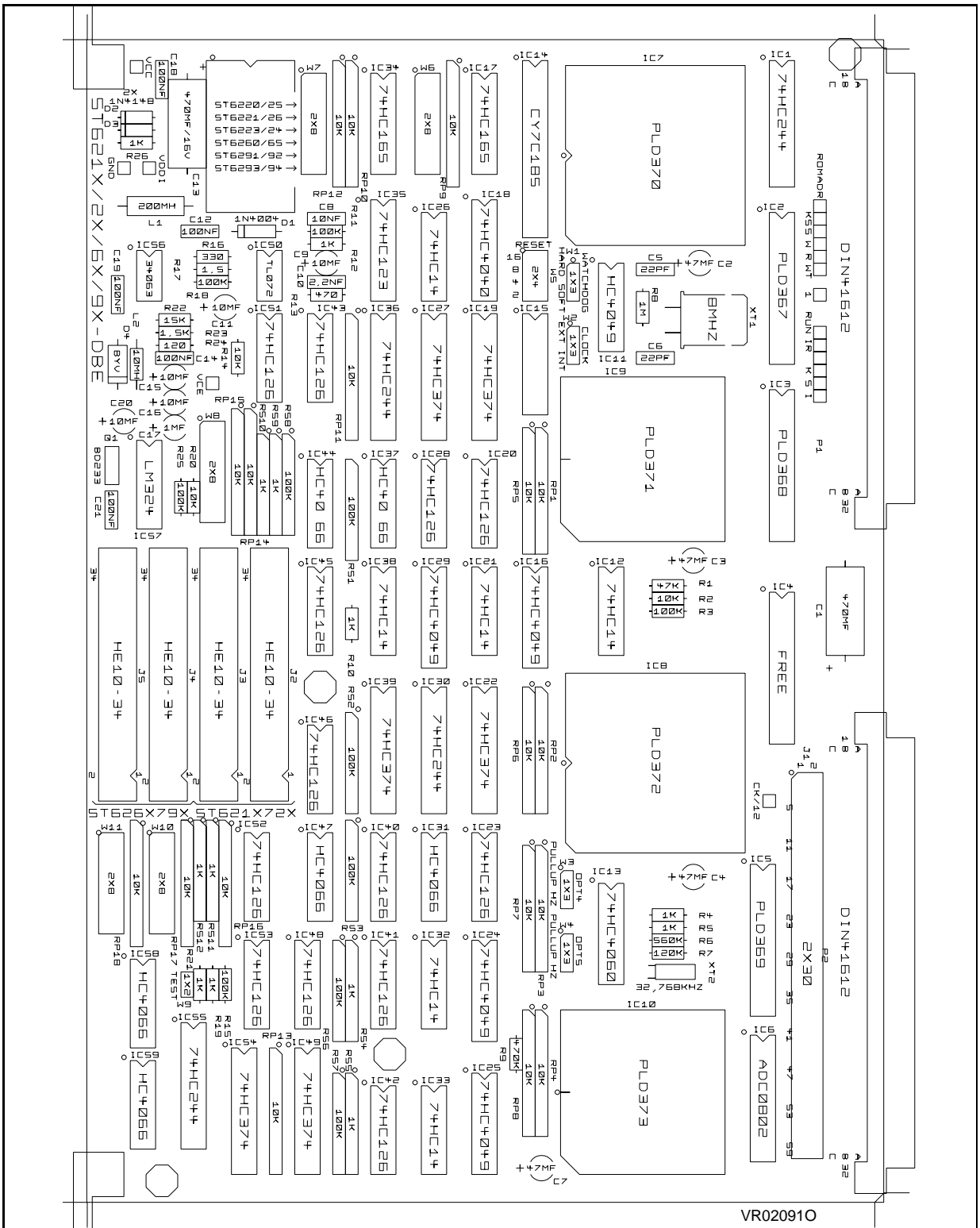
In WAIT mode, led WAIT is ON, in STOP mode the 2 led WAIT and STOP are ON (on the front panel of the emulator).

If STOP or WAIT instructions are not exited, it comes from:

- The core is not in normal mode: after **RESET** the core is in **NMI mode**, to enter the **normal mode** which let execute interrupt to exit from these states, the core must execute a **RETI** instruction.

6 ANNEX

6.1 COMPONENTS LAYOUT



6.2 ST626X-DBE SCHEMATICS

Figure 1. Main sheet

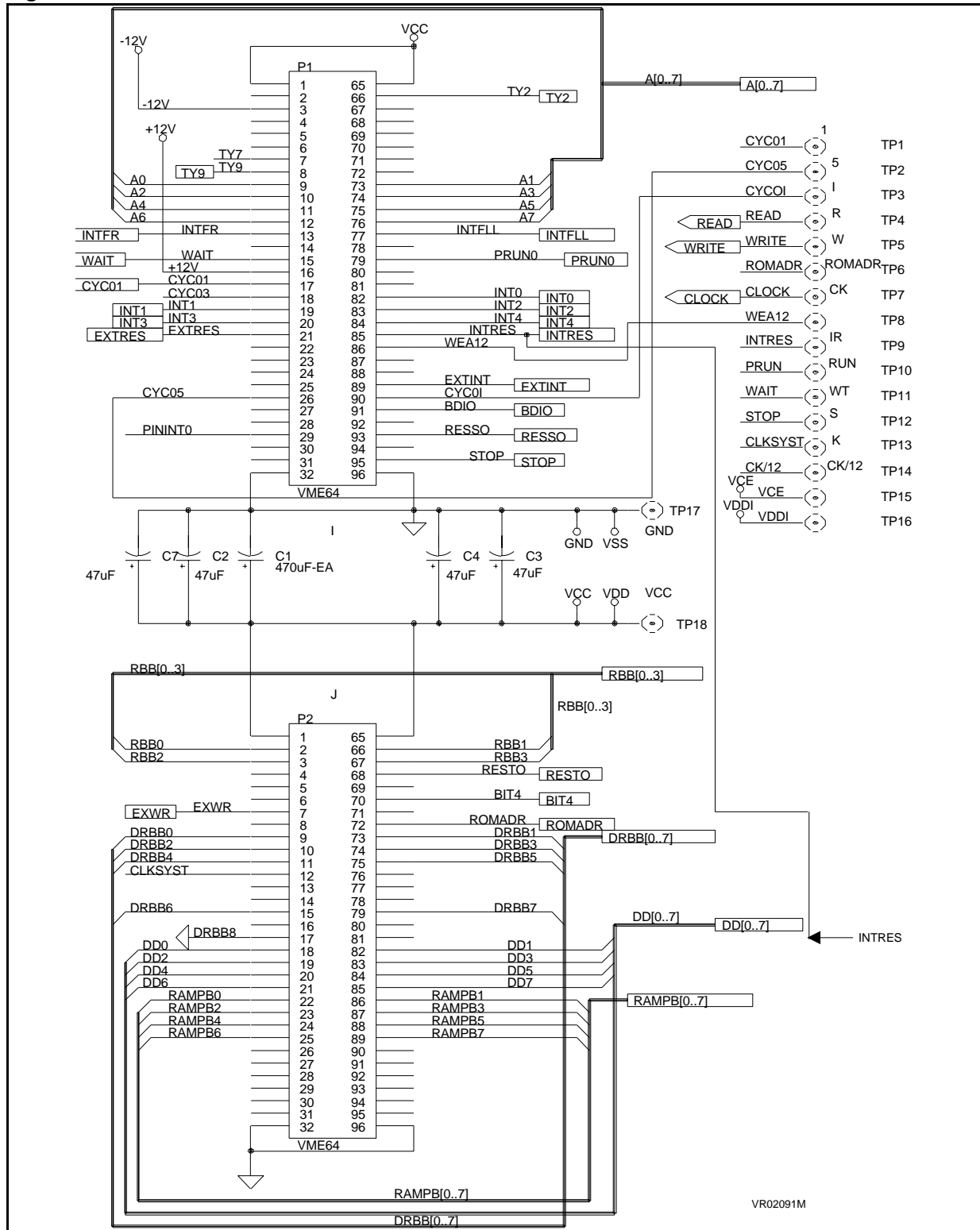


Figure 1. Main sheet (Cont'd)

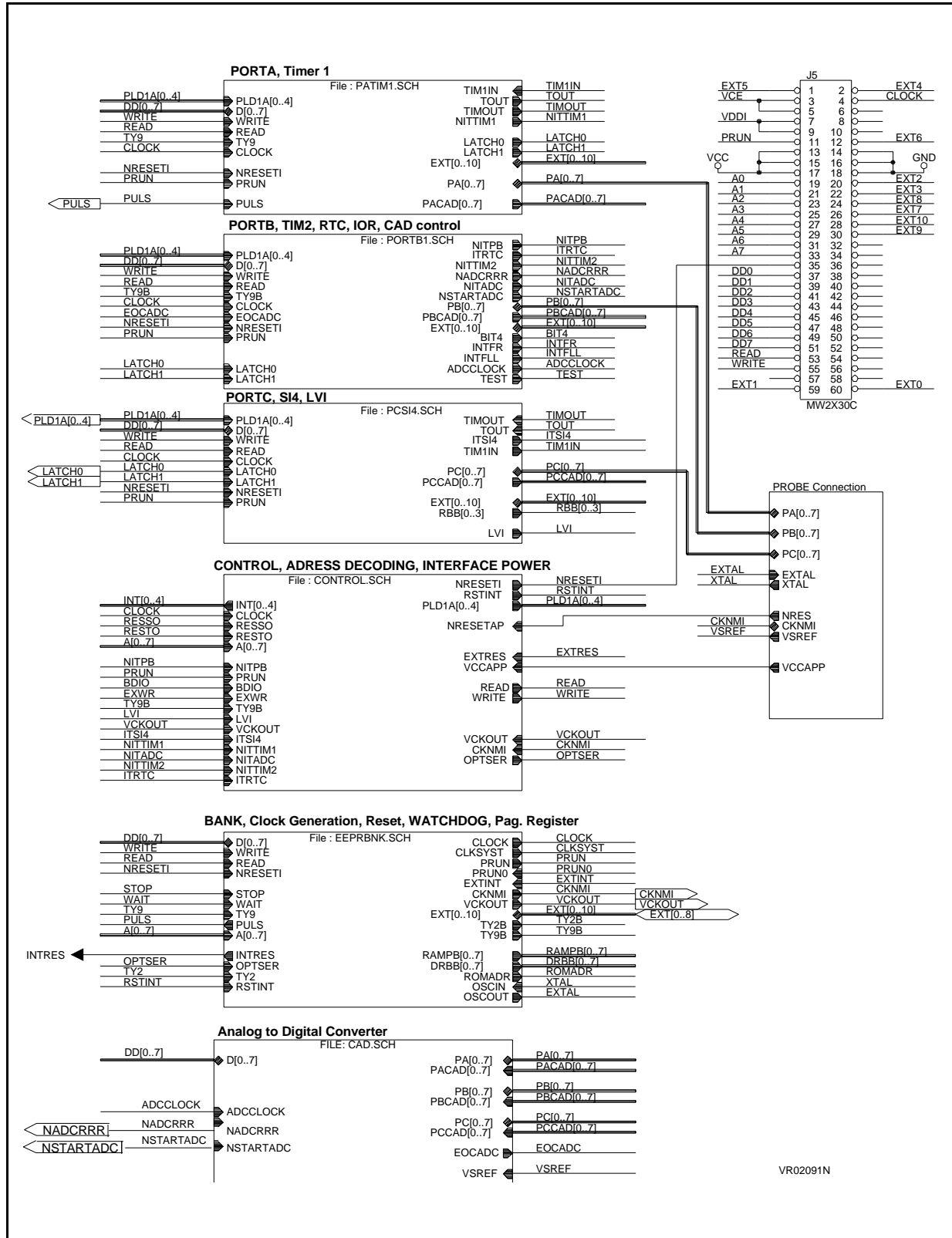


Figure 2. Port A and Timer 1

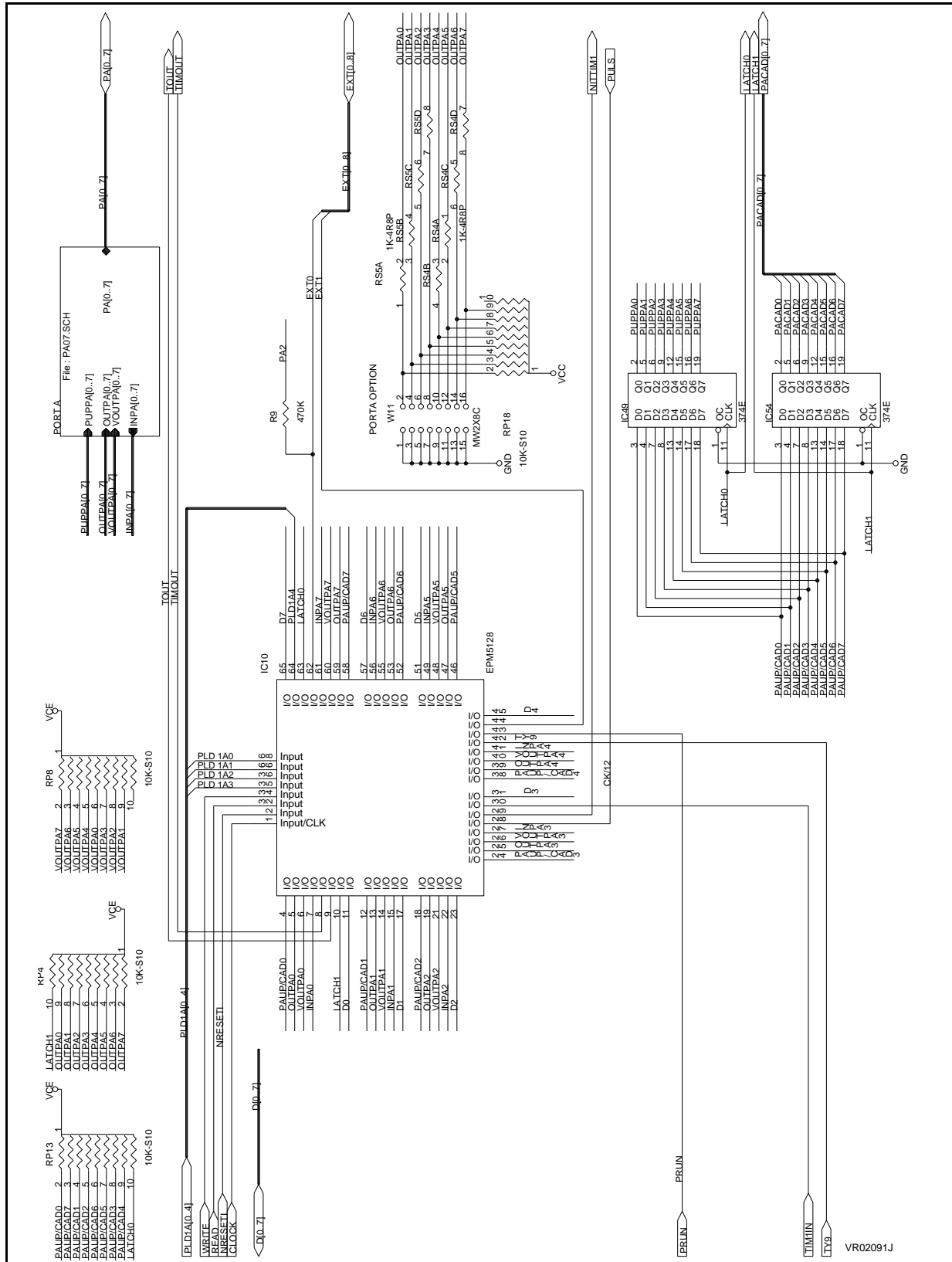


Figure 3. Port A buffers

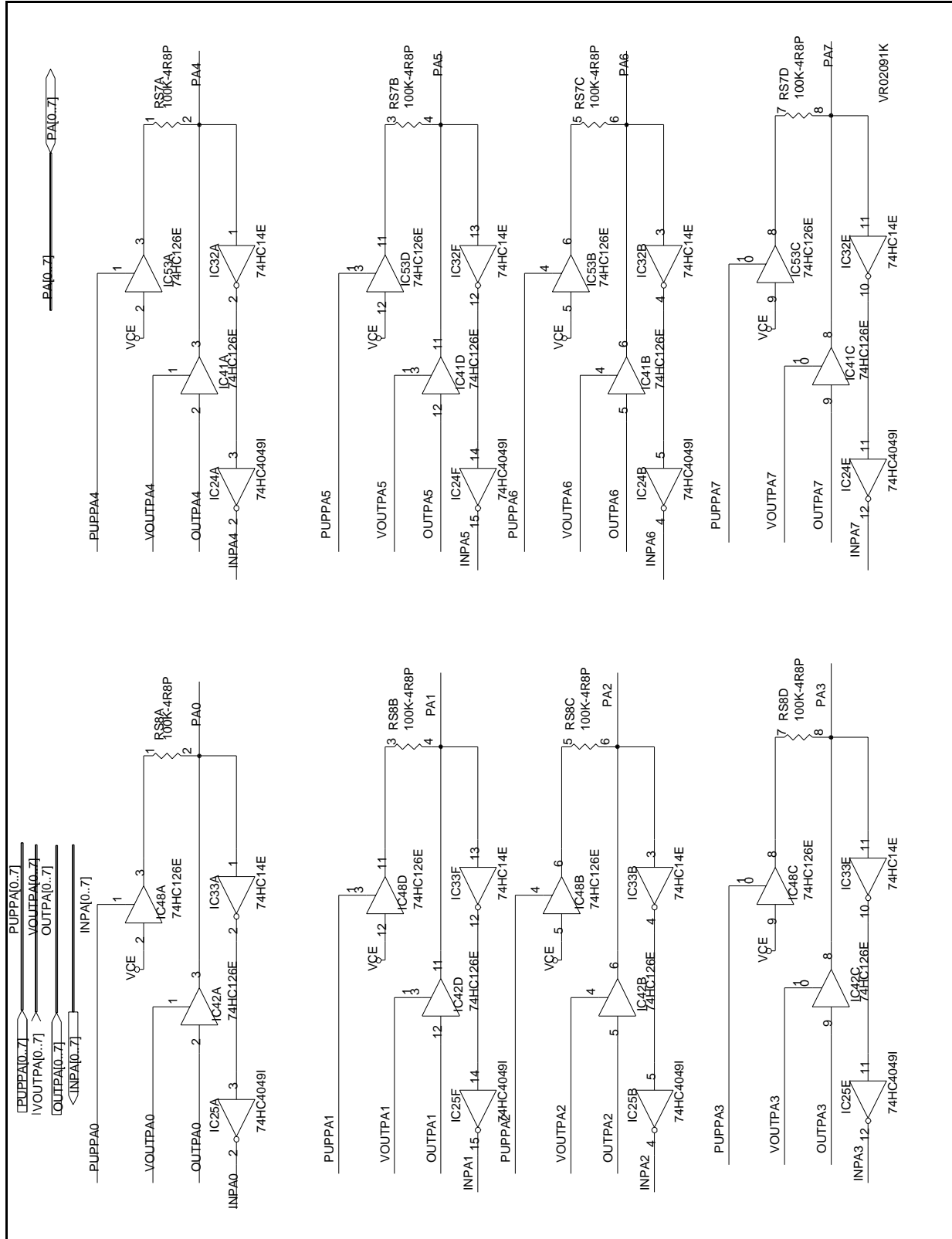


Figure 4. Port B and Timer 2

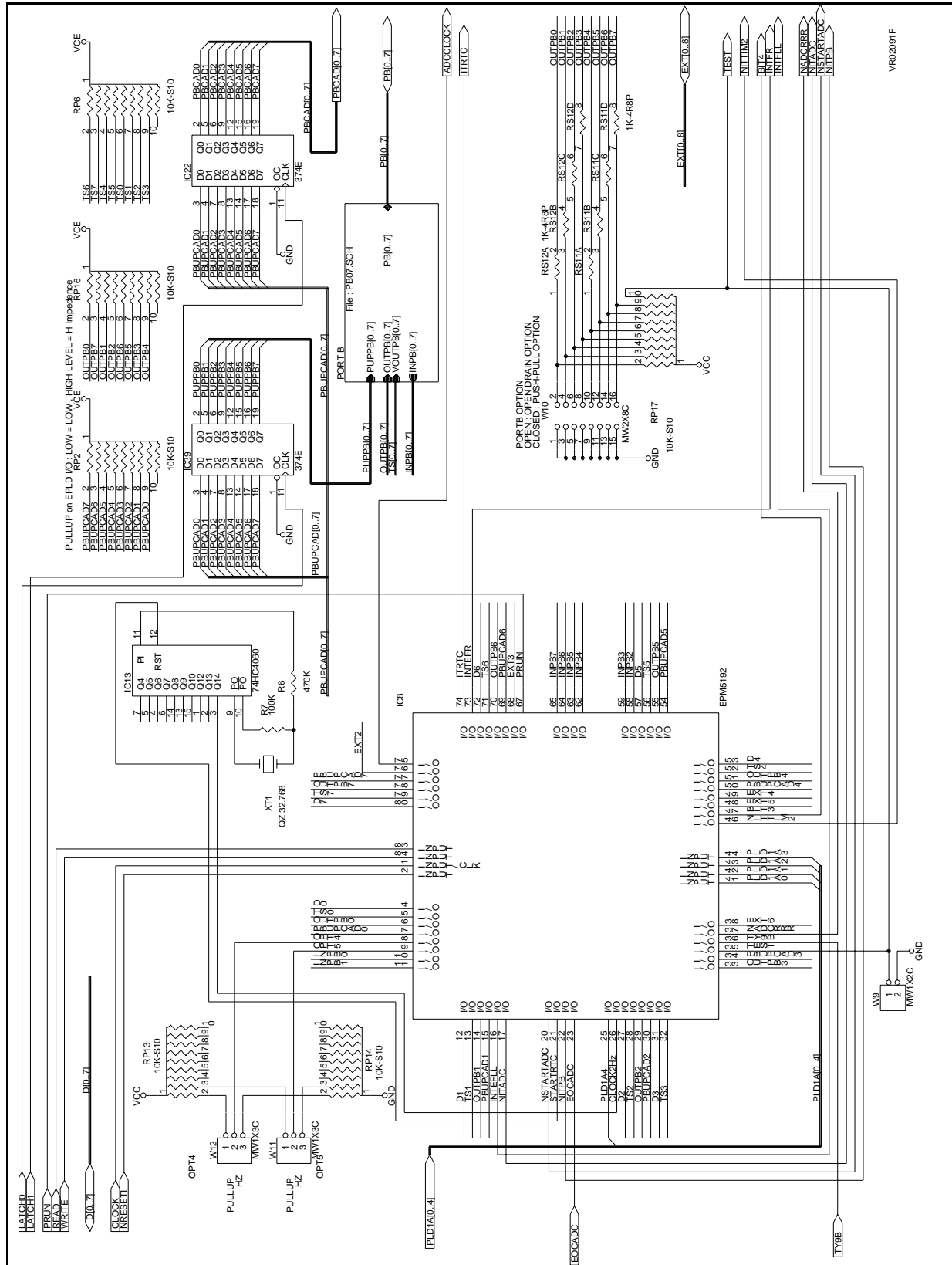


Figure 5. Port B and Timer 2 buffer

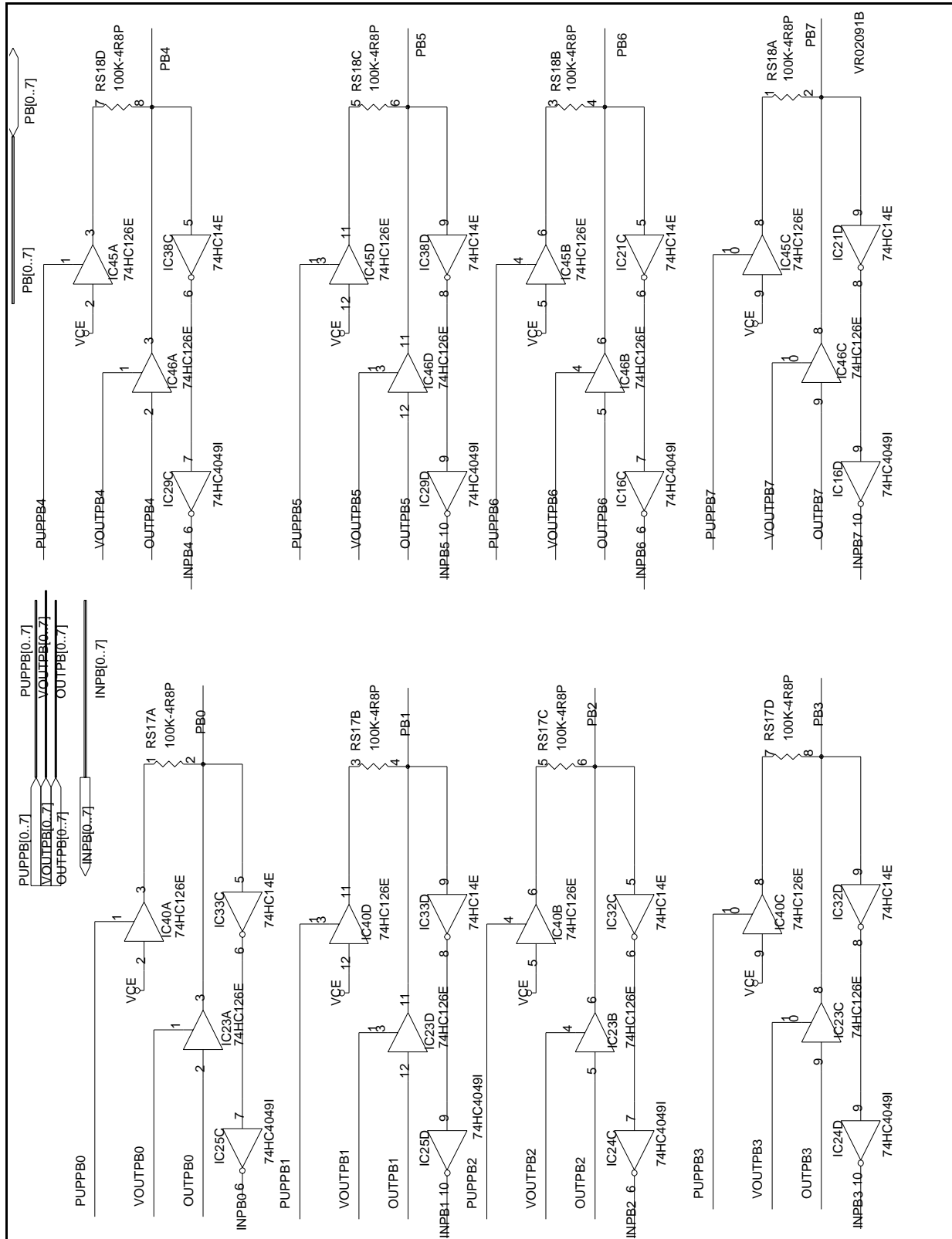


Figure 6. Port C and SIO

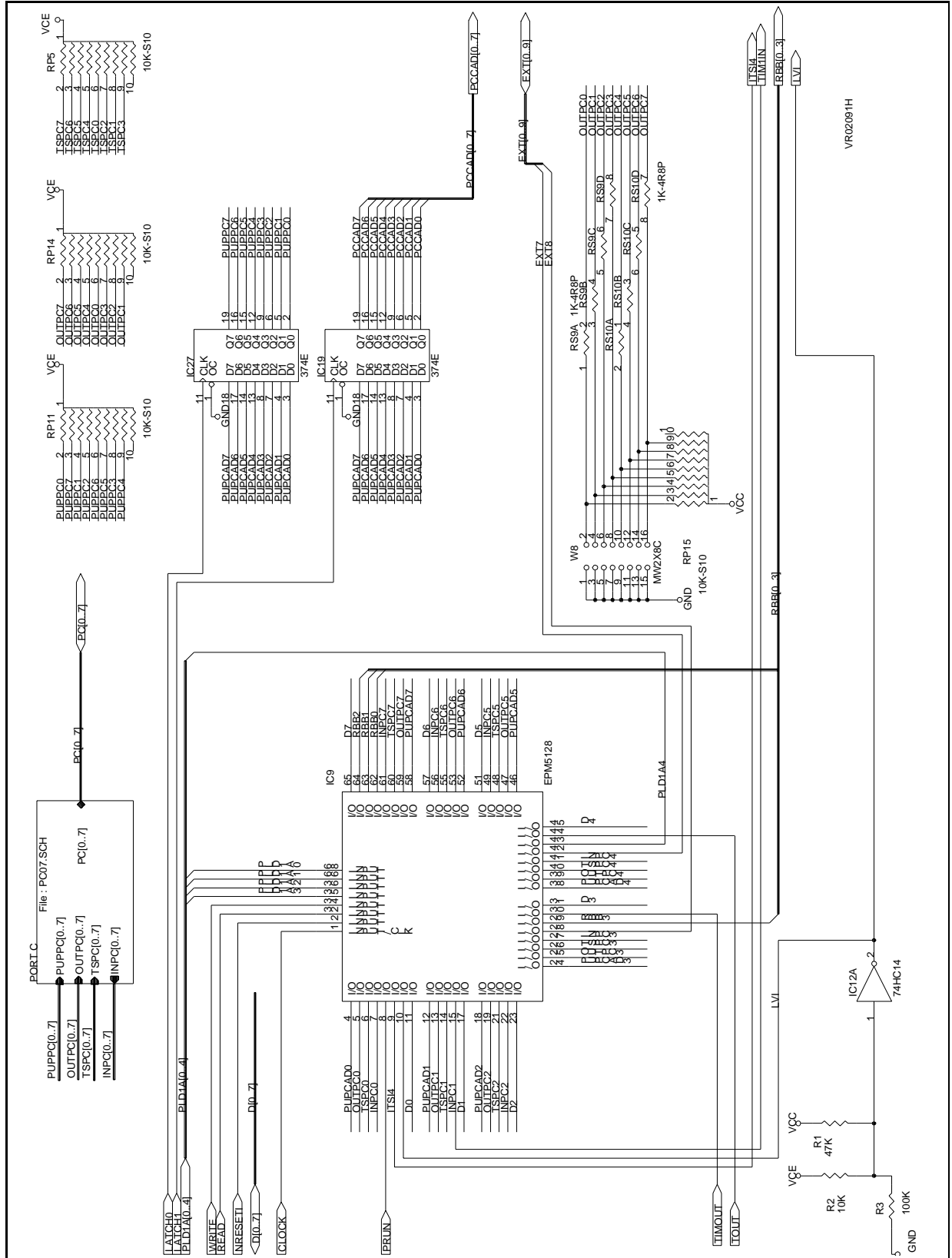


Figure 7. Port C and SIO buffers

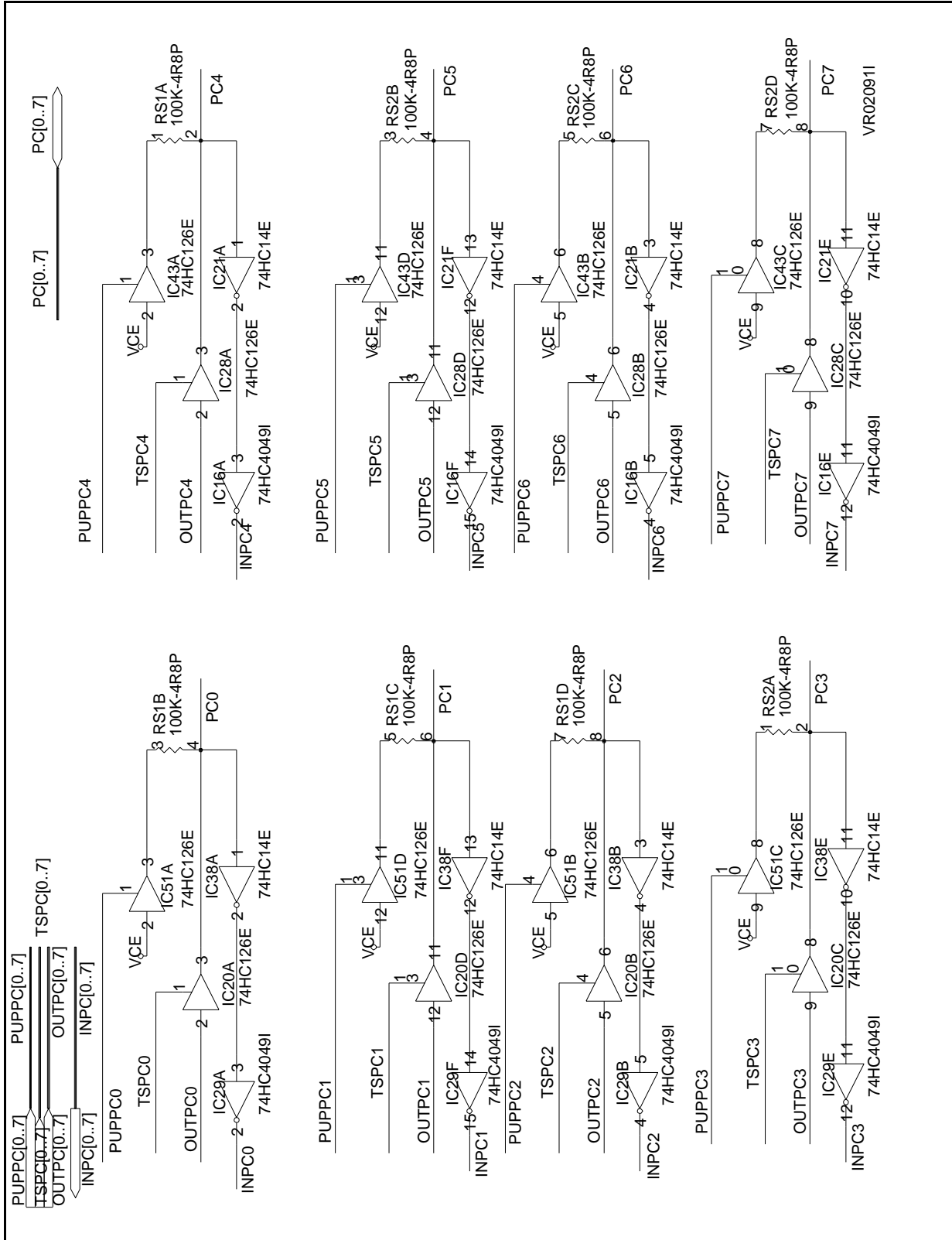


Figure 8. RAM, EEPROM, Bank reg., Data ROM windowing, watchdog, Reset

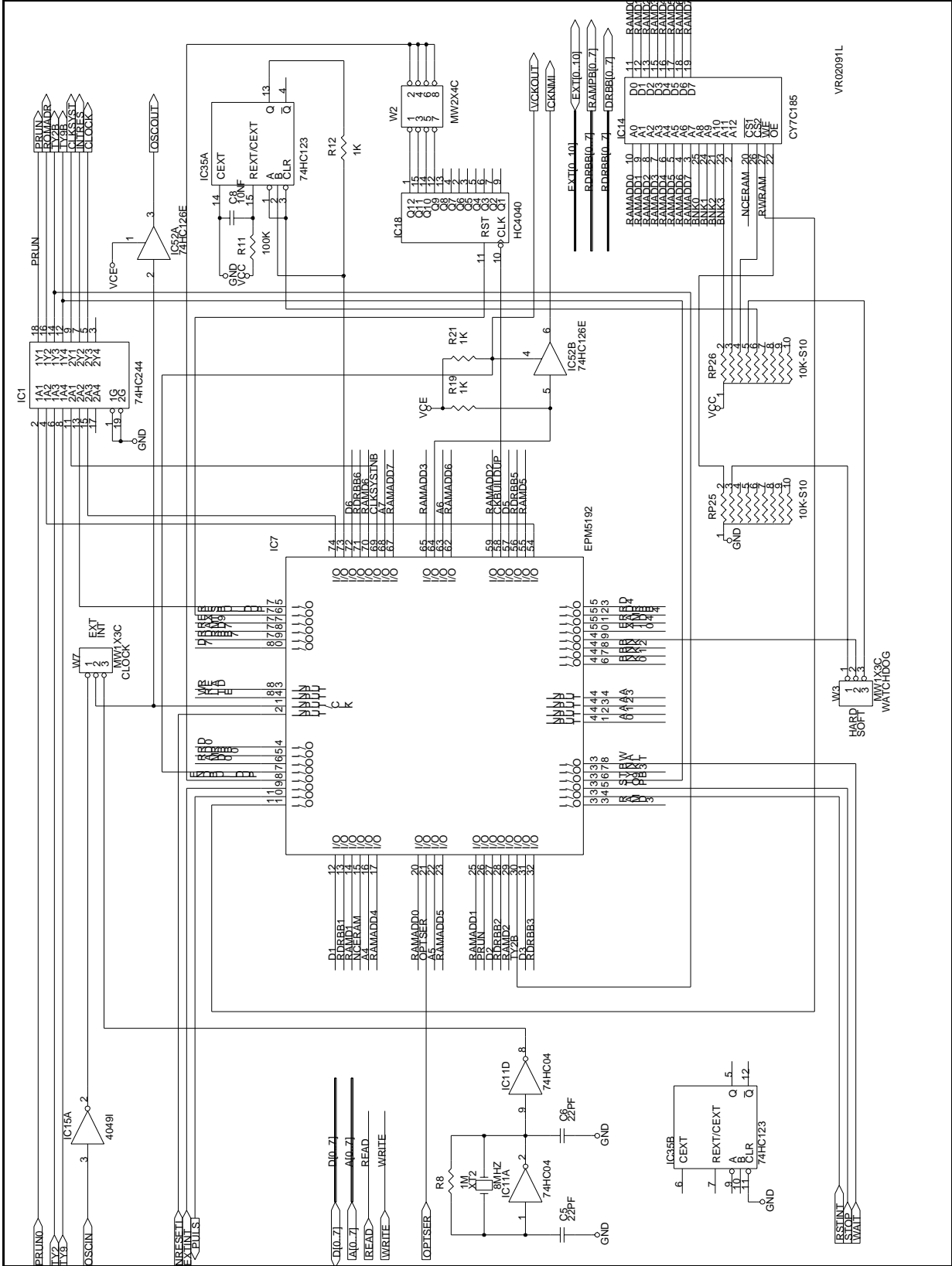
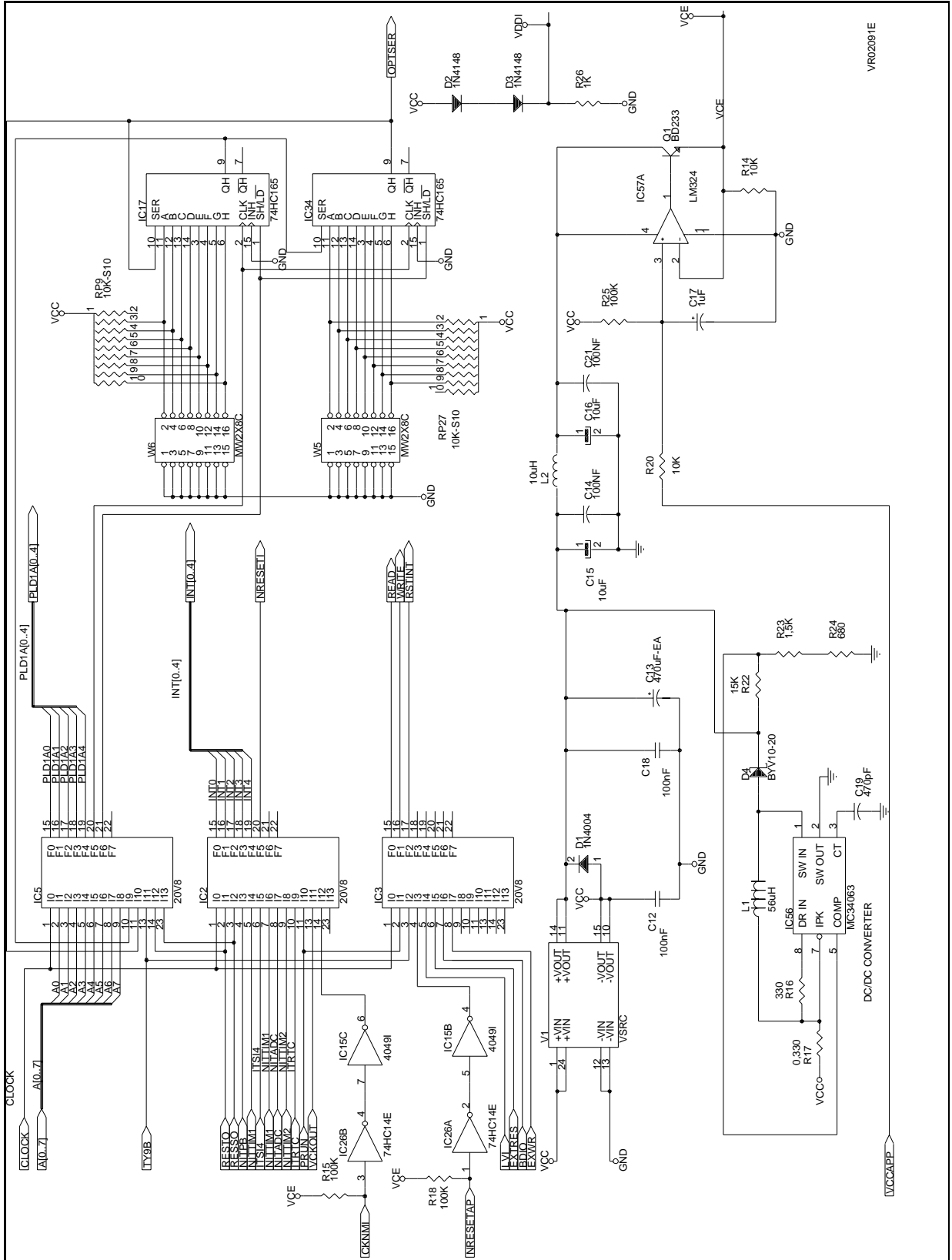


Figure 9. Control and interface power



VR02091E



Figure 10. Analog To Digital Converter

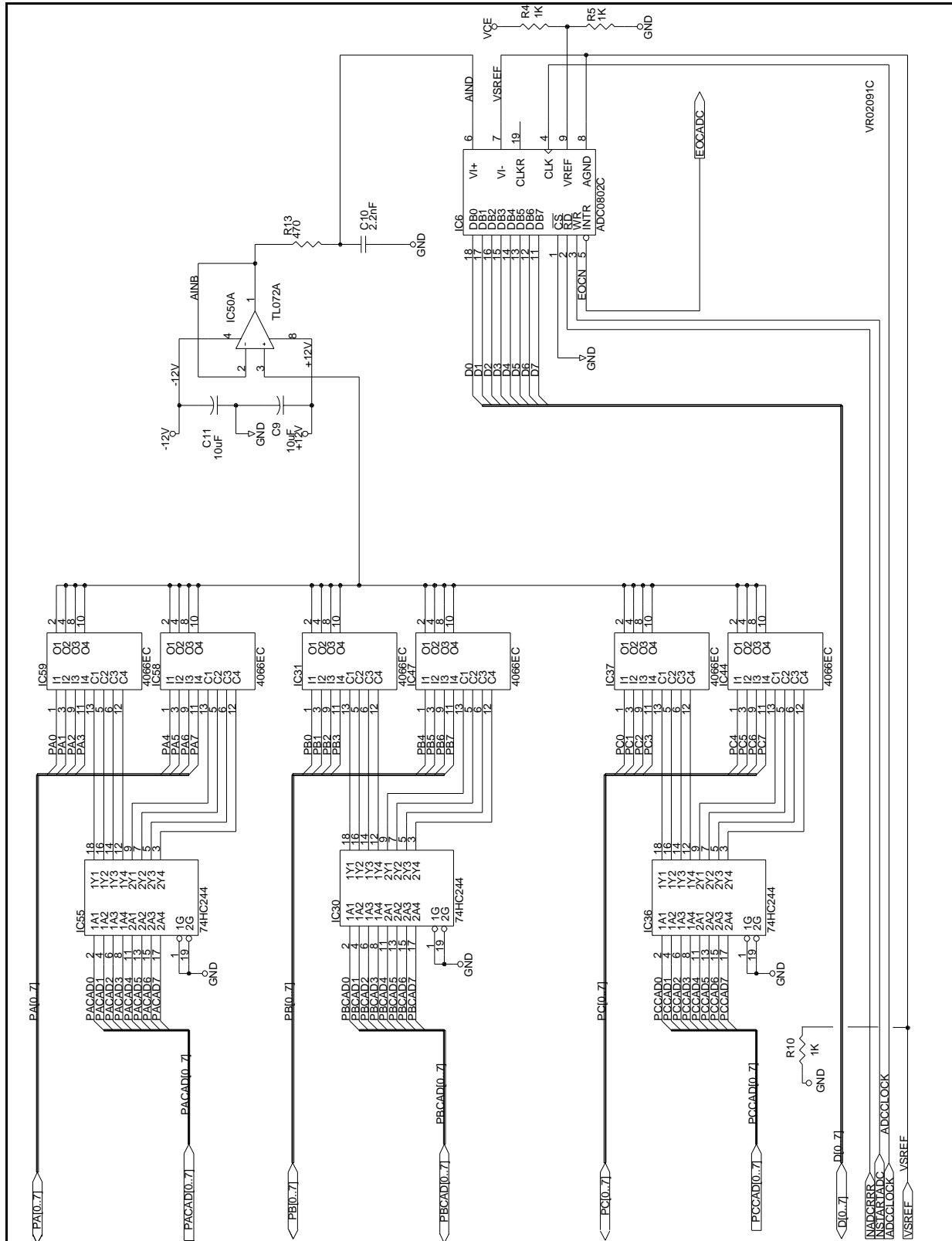
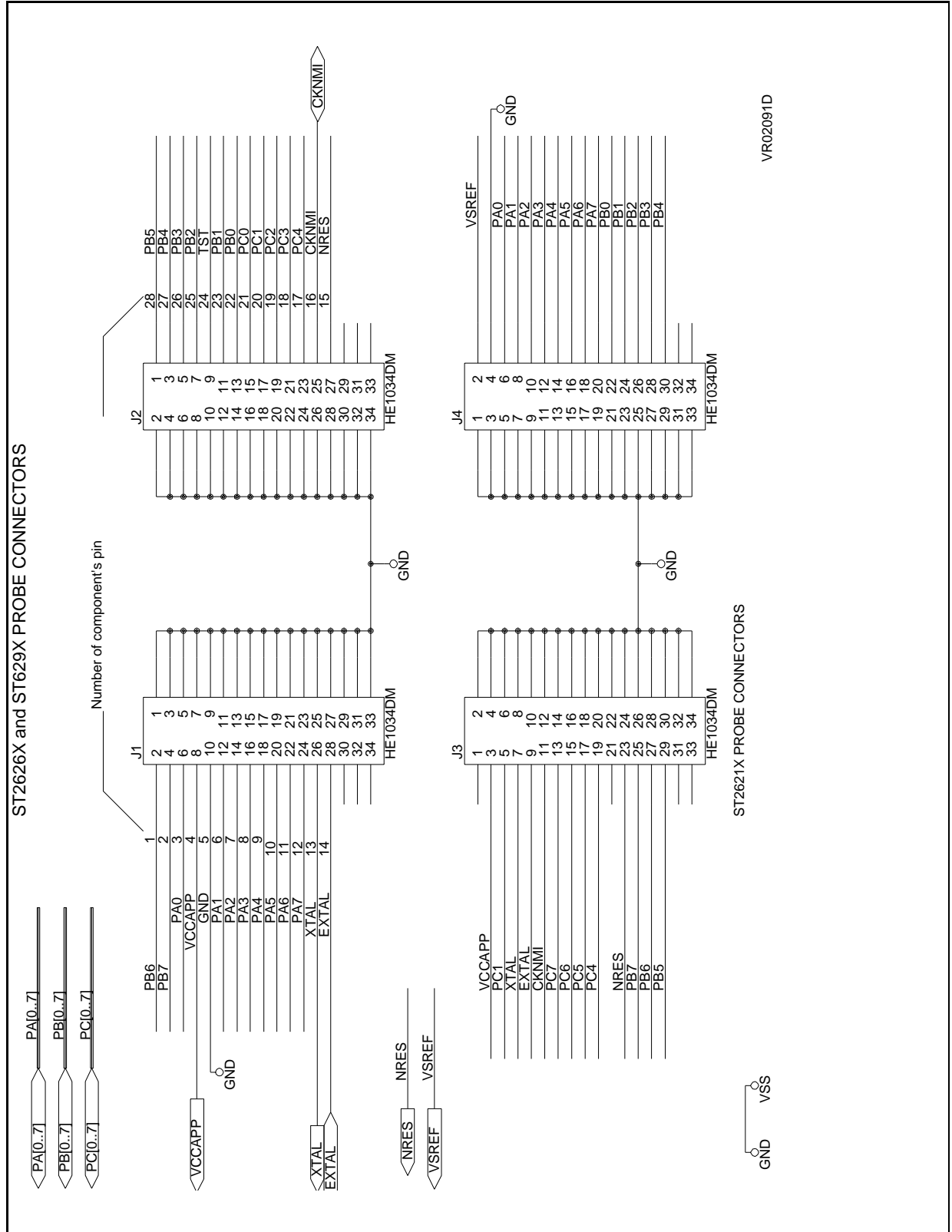


Figure 11. Application connectors



6.3 PROBE

Figure 12. Probe for ST620x, ST621x, ST622x

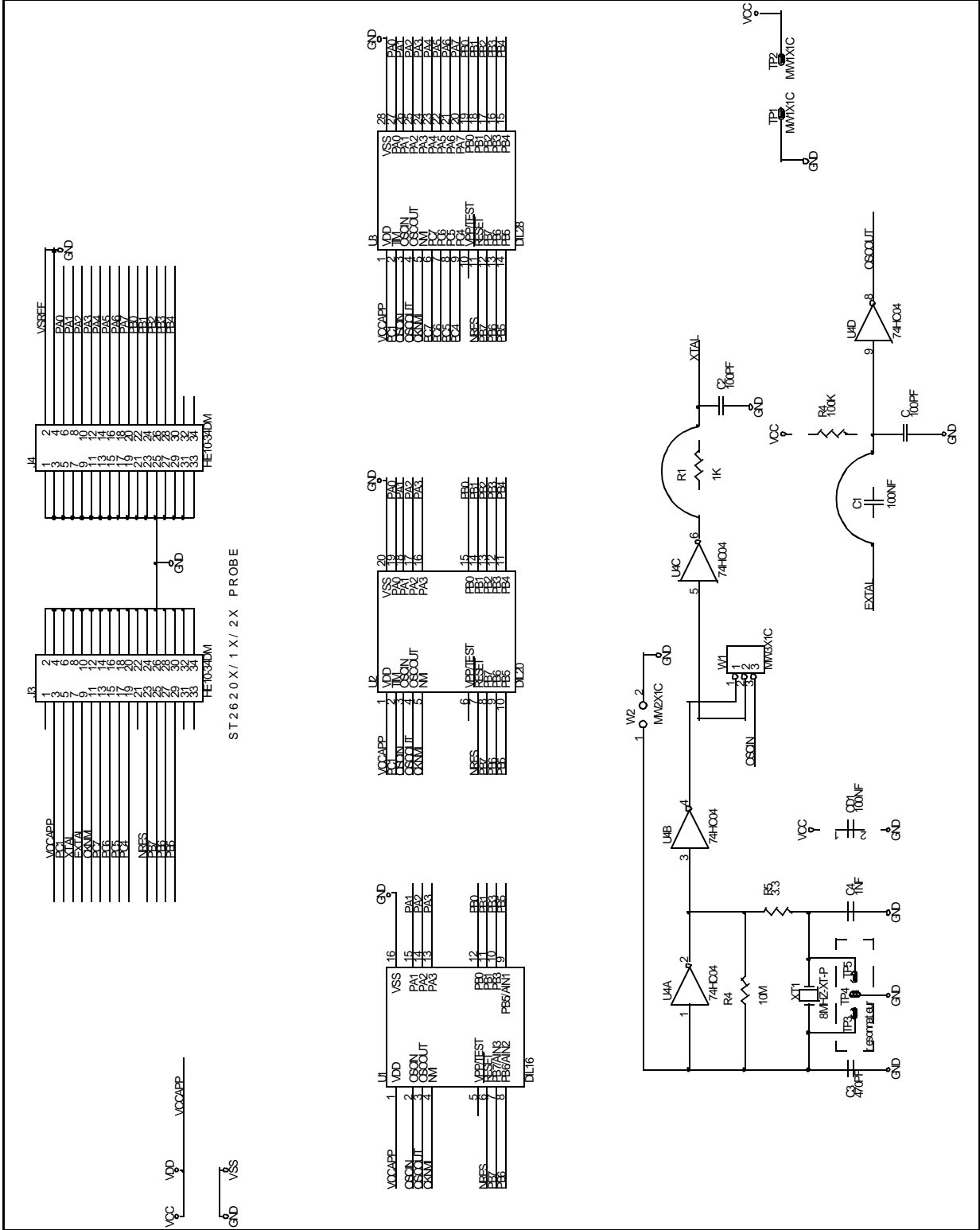
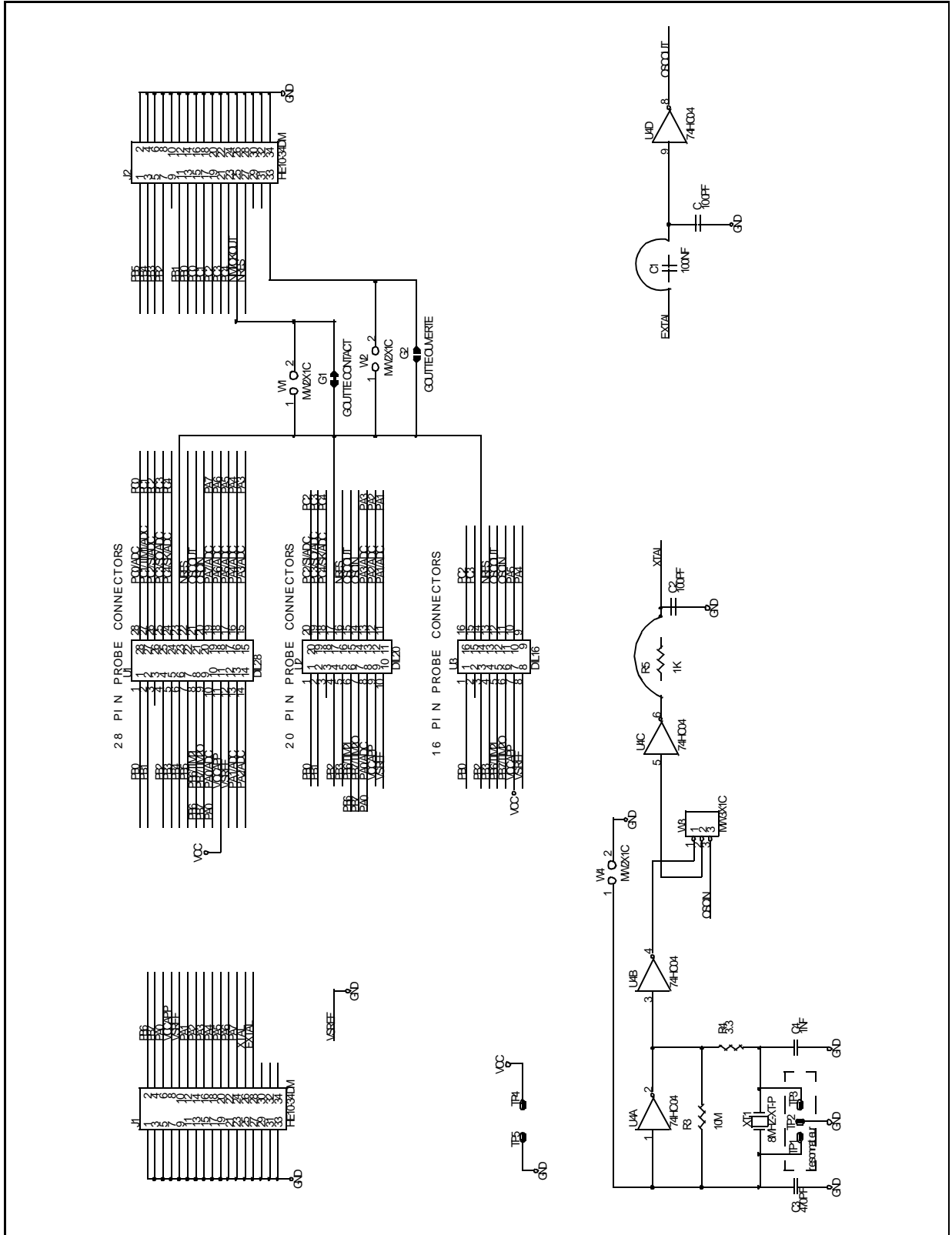


Figure 13. Probe for ST625x, ST626x, ST629x



Notes:

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