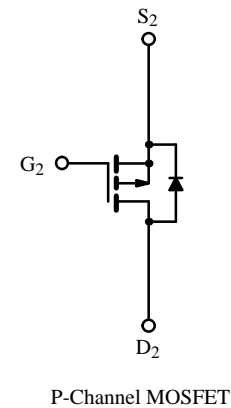
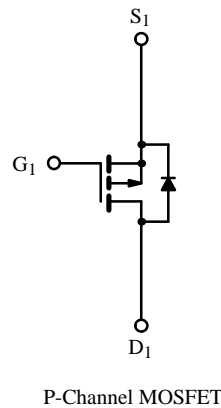
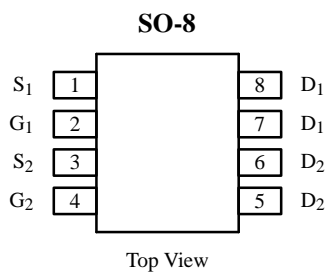


**Dual P-Channel Enhancement-Mode MOSFET**

**Product Summary**

V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
-30	0.085 @ V <sub>GS</sub> = -10 V	± 3.5
	0.19 @ V <sub>GS</sub> = -4.5 V	± 2.5



**Absolute Maximum Ratings (T<sub>A</sub> = 25°C Unless Otherwise Noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	-30	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 150°C) <sup>a</sup>	I <sub>D</sub>	T <sub>A</sub> = 25°C	± 3.5
		T <sub>A</sub> = 70°C	± 2.8
Pulsed Drain Current	I <sub>DM</sub>	± 20	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	-1.7	
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>A</sub> = 25°C	2.0
		T <sub>A</sub> = 70°C	1.3
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C

**Thermal Resistance Ratings**

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient <sup>a</sup>	R <sub>thJA</sub>	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1238. A SPICE Model data sheet is available for this product (FaxBack document #5149).

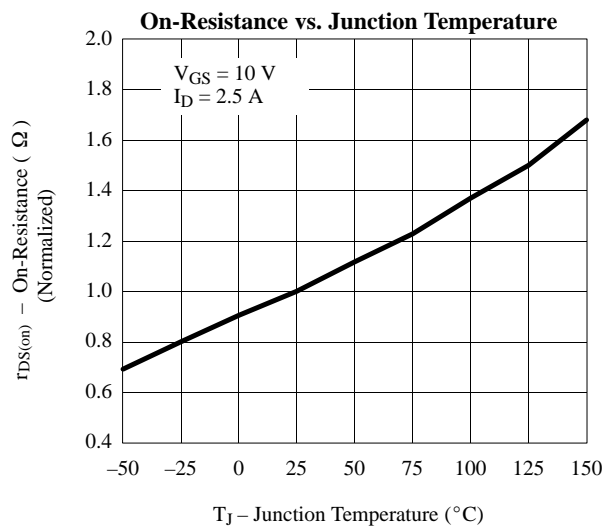
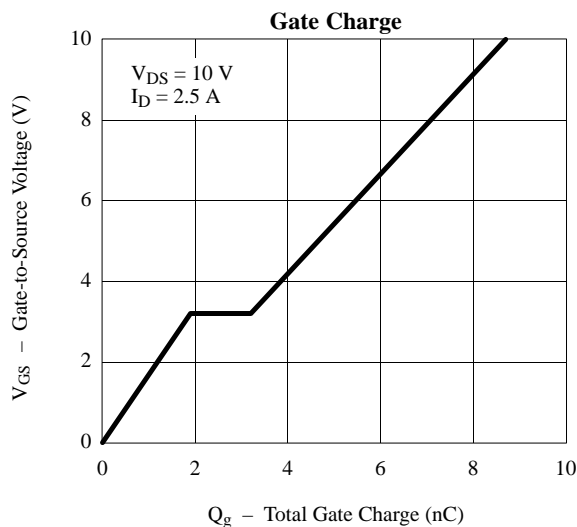
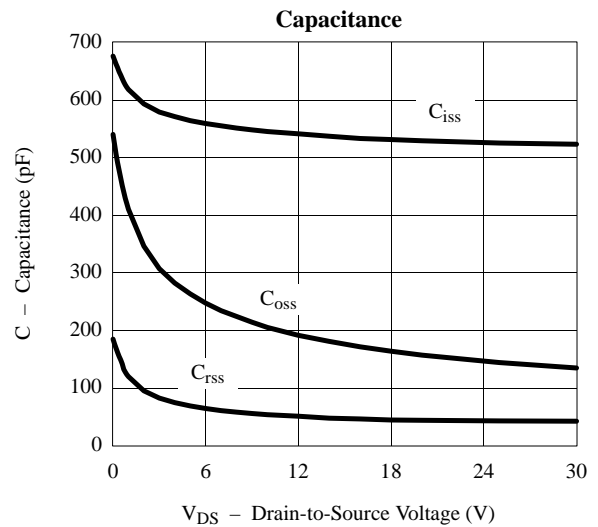
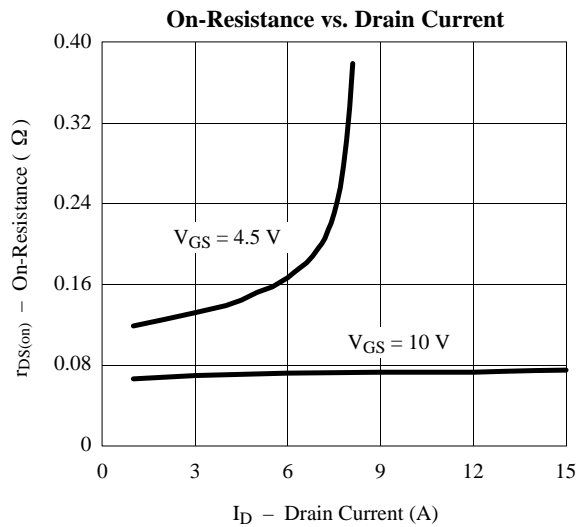
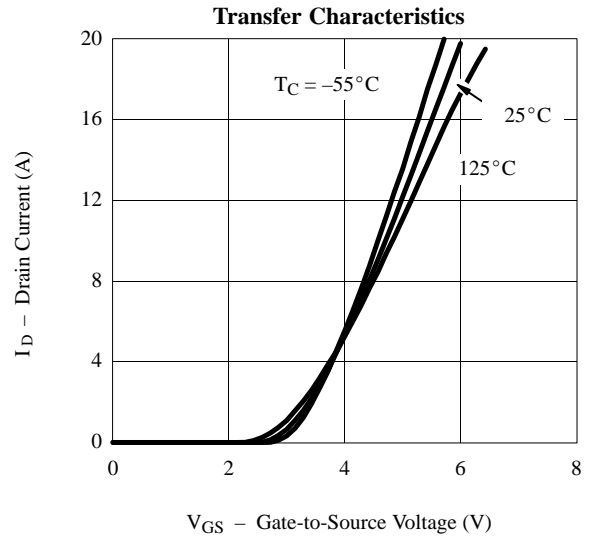
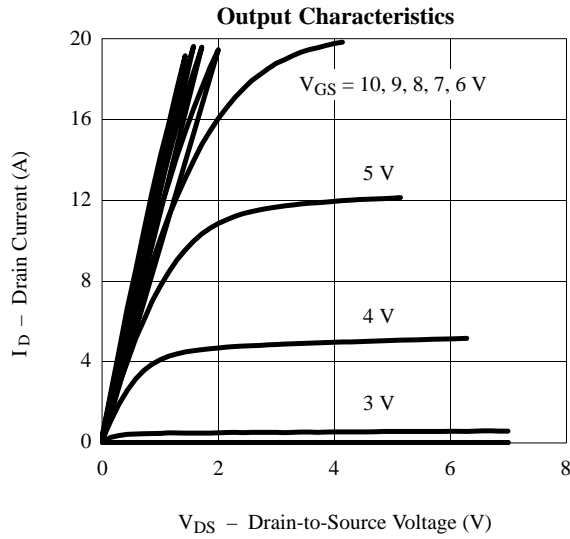
**Specifications ( $T_J = 25^\circ\text{C}$  Unless Otherwise Noted)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	1.0			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}$			-1	$\mu\text{A}$
		$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			-25	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq -5\ \text{V}, V_{GS} = -10\ \text{V}$	-15			A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}, I_D = 2.5\ \text{A}$		0.066	0.085	$\Omega$
		$V_{GS} = -4.5\ \text{V}, I_D = 1.8\ \text{A}$		0.125	0.19	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -15\ \text{V}, I_D = -2.5\ \text{A}$		5.0		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = -1.7\ \text{A}, V_{GS} = 0\ \text{V}$		-0.8	-1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = -10\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -2.5\ \text{A}$		8.7	15	nC
Gate-Source Charge	$Q_{gs}$			1.9		
Gate-Drain Charge	$Q_{gd}$			1.3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}, R_L = 10\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -10\ \text{V}, R_G = 6\ \Omega$		7	15	ns
Rise Time	$t_r$			9	18	
Turn-Off Delay Time	$t_{d(off)}$			14	27	
Fall Time	$t_f$			8	15	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = -1.7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		50	80	

## Notes

- a. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 b. Guaranteed by design, not subject to production testing.

**Typical Characteristics (25°C Unless Otherwise Noted)**



## Typical Characteristics (25°C Unless Otherwise Noted)

