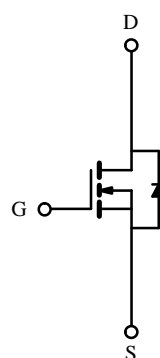
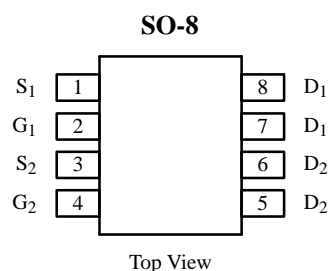


Dual N-Channel Enhancement-Mode MOSFET

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
60	0.055 @ V _{GS} = 10 V	±4.5
	0.075 @ V _{GS} = 4.5 V	±3.9

175°C Rated
Maximum Junction Temperature
TrenchFET™
Power MOSFETs



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	60	V
Gate-Source Voltage	V _{GS}	±20	
Continuous Drain Current (T _J = 175°C) ^a	I _D	T _A = 25°C	±4.5
		T _A = 70°C	±3.8
Pulsed Drain Current	I _{DM}	±30	A
Continuous Source Current (Diode Conduction) ^a	I _S	2	
Maximum Power Dissipation ^a	P _D	T _A = 25°C	2.4
		T _A = 70°C	1.7
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 175	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1239.

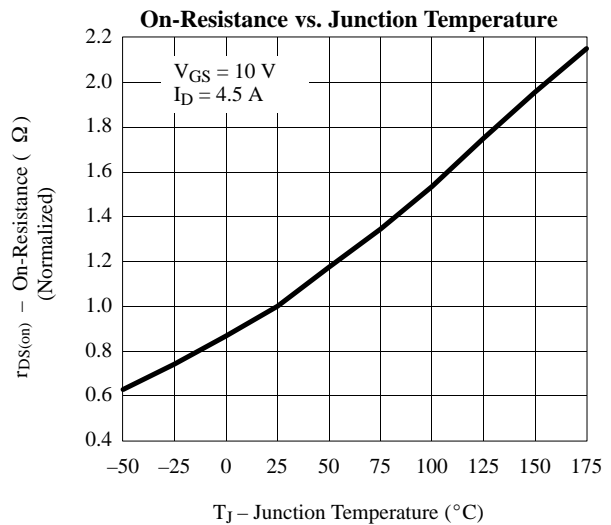
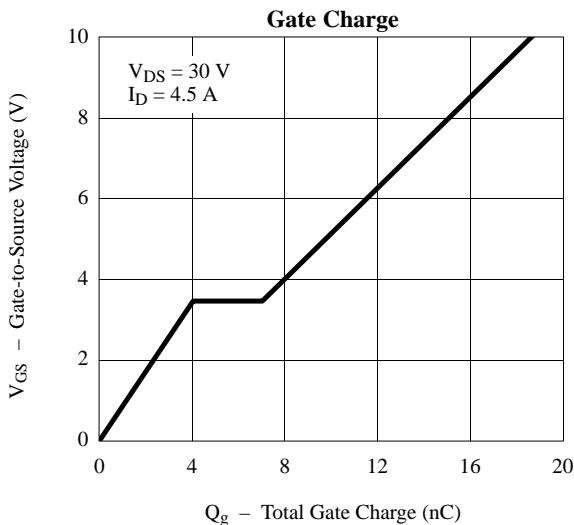
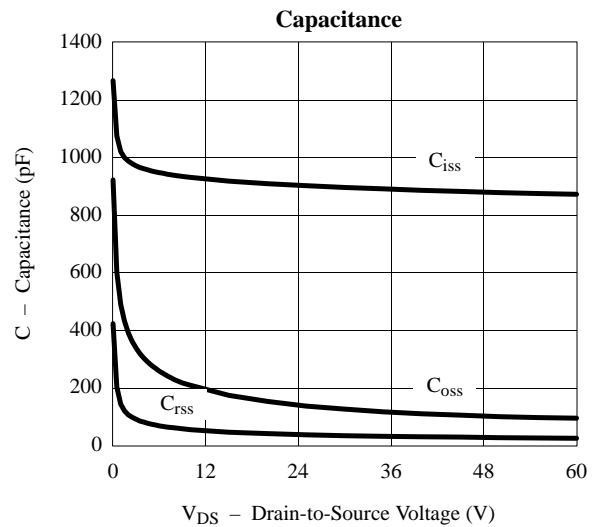
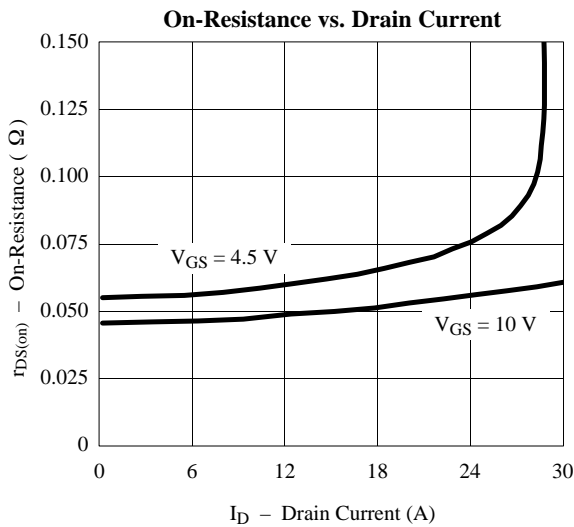
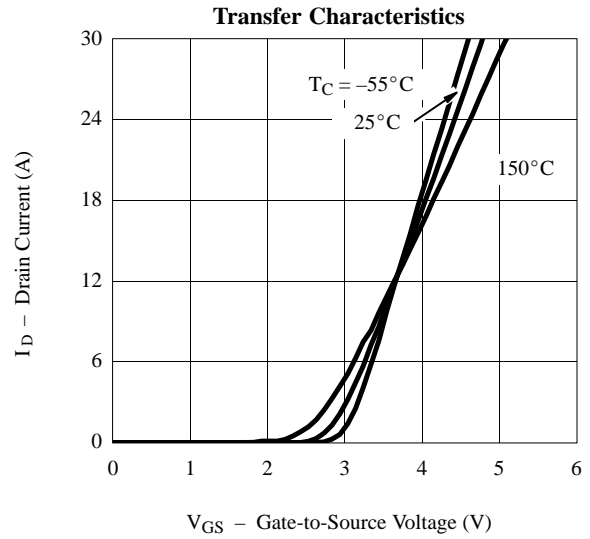
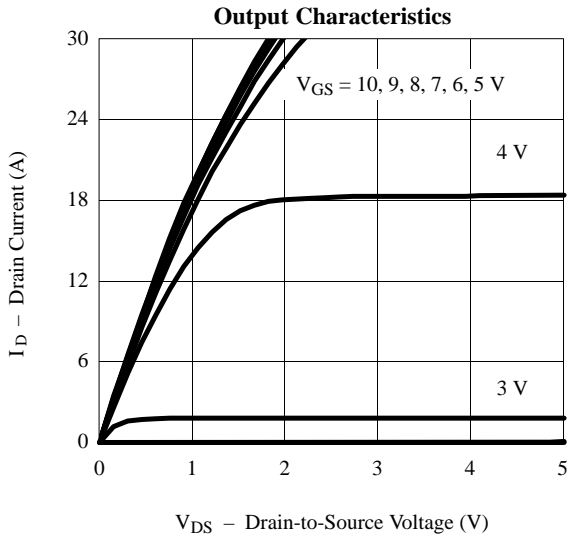
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$			2	μA
		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 4.5 \text{ A}$		0.045	0.055	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 3.9 \text{ A}$		0.055	0.075	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 4.5 \text{ A}$		13		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 2 \text{ A}, V_{GS} = 0 \text{ V}$		0.9	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 4.5 \text{ A}$		19	30	nC
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30 \text{ V}, R_L = 30 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 6 \Omega$		13	20	ns
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			36	60	
Fall Time	t_f			11	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		35	60	

Notes

- a. For design aid only; not subject to production testing.
 b. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)

