Thermal Management in On-Board DC-to-DC Power Conversion

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Abstract: Switchmode dc-to-dc power converters are frequently used as an integral part of board-mounted systems because of their ability to handle high power levels despite their small size. But the ever-increasing switching frequencies that make smaller sizes possible have been achieved only at the cost of increased switching losses and reduced thermal conductivity. Surface-mounted power MOSFETs have added heat sinking to the role of the PC board. This brings us to the point where thermal conditions become the limiting factor in size reduction.

This paper will provide guidelines for optimizing thermal layout in terms of heat transfer from the MOSFET junction to the PC board, distribution of heat in the PC board, placement of components on the PC board, concluding in the estimation of the MOSFET's $R\theta_{ja}$.

INTRODUCTION: COMPACT POWER CONVERTERS

As portable computers and phones become smaller and smaller, their power supplies and power conversion circuits must also shrink. To create compact converters, a basic necessity is high-frequency operation, which allows the physical size of the capacitors and the inductor to be reduced. Indeed, passive components occupy the majority of the board area in most converters.

The size of these components is a function of the energy storage needed. In a synchronous buck converter, for example, an equation indicating the size of passive components can be derived merely by assuming that high efficiency is desired. The maximum ripple in the converter's inductor should be approximately 50% of the converter's maximum output current. Once the inductor's size is known, the output capacitance can be determined by restricting step load response. Using this technique, the output capacitance and choke inductance of a converter with a 10-W, 3.3-V output and allowed input voltage of 4.5 to 11.8 V can be easily determined (Figure 1).

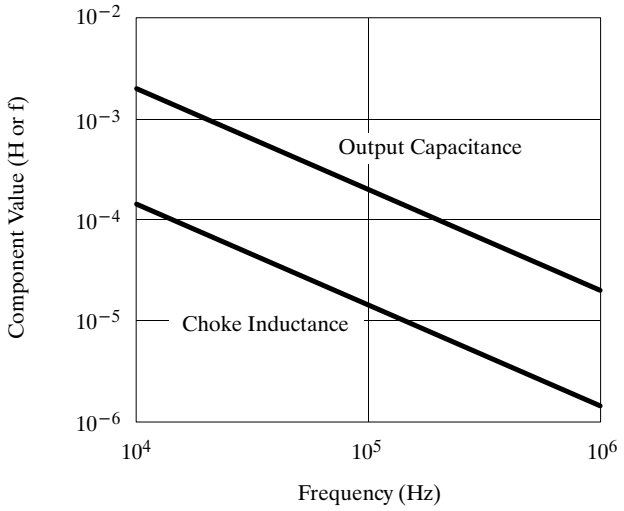

Figure 1. Output capacitance and choke inductance vs. frequency

High frequency operation does, of course, impose costs. As frequency is increased, efficiency tends to decrease. Power is consumed by the ESR of input and output capacitors, by the AC resistance of the choke, and by the switching loss of the converter's MOSFETs. Other techniques for reducing converter size, such as increasing the flux density in the choke or increasing its number of turns, also lead to waste. The waste heat generated in the choke limits its size, even in converters where efficiency is unimportant (McLimen, 1978). Heating also limits the allowed ripple current in many capacitors.

When a system's power supply is designed, its effect on the entire system must be considered. In many laptop computers, for example, system performance is constrained by the ability of the computer's base enclosure to dissipate heat. Once the system's thermal budget has been utilized, additional performance can be obtained only at the expense of other features.

One ready source of additional power is the main converter's waste heat. In a typical laptop design, an improvement in converter efficiency from 80 % to 90 % allows an additional 1 to 2 W of power for other uses.

Even in systems which are not thermally limited, however, wasted power degrades system specifications. Heat must somehow be dissipated from an inefficient converter. Unfortunately, most heat redistribution techniques are cumbersome, expensive, or both. Heat sinks and fans consume volume and increase system weight. Even in systems which consume very little power, the value of the energy wasted must also be computed. An increase in converter efficiency from 80% to 90% can

actually reduce the battery size by 11%. Or a less expensive battery technology may be used, maintaining the same size but reducing costs.

Low on-resistance surface-mount power MOSFETs are one part of the solution (Williams, 1995). They provide efficient operation, ease of assembly, and efficient use of space. They also eliminate the need for traditional, bulky heat sinks. As a result, power converters can now be designed using only surface-mount components.

Thermal Management On the PCB

Even though PCB material is a very poor thermal conductor, it provides an adequate heat sink for the state-of-the-art surface-mount power MOSFETs available for today's converters. The actual thermal system is the surface-mounted MOSFET package and the PCB. The thermal path begins at the MOSFET's junction, goes through the lead frame, into the PCB, and then into the ambient air (Figure 2). It is up to the designer, however, to maximize the effects of this system, by careful choice of the PCB material and careful layout of the board itself.

The most common approach is the use of FR-4 in a four- or -six-layer board. The four layers allow a compact layout, since the internal layers can be used for power and ground planes. Six-layer boards typically introduce two additional signal layers between the power and ground planes. If the two center signal layers are ignored, a six-layer board becomes a four-layer board with planes close to the surface. These copper planes also act as heat spreaders.

If the design shown in Figure 2 were modified from a double-sided PC board to a four-layer one, the number of thermal paths would increase and thermal resistance would drop. Then there would be three layers of FR-4 and two layers of copper.

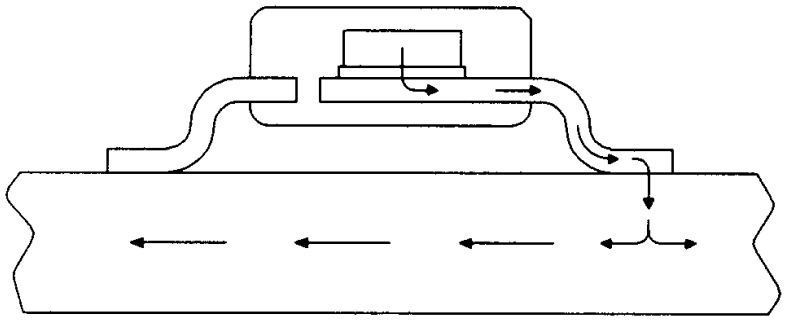

Figure 2. Thermal path in board-mounted power MOSFET

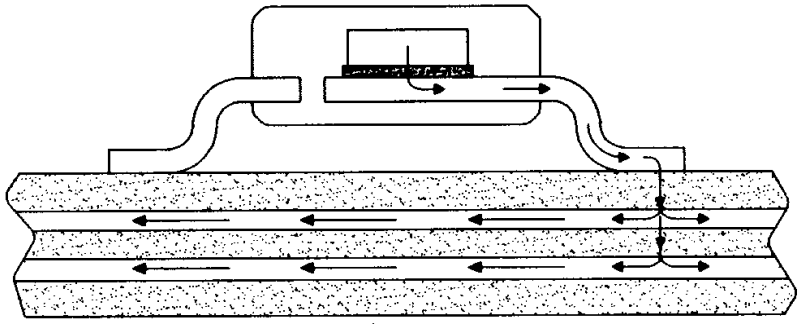

Figure 3. Thermal path with four-layer PCB

In a 0.062-in. board, the FR-4 layer thickness is 0.022 in. or less. Since heat passes through both of the inner copper planes, the thermal resistance of the PC board is significantly smaller than in a standard piece of 0.062-in. double-sided FR-4. This makes it easier for the heat to move from the device leads to inner copper layers, and to spread throughout the board.

These thermal characteristics were evident in tests characterizing LITTLE FOOT® MOSFETs mounted on an 0.062-in. FR-4 four-layer board. The baseline data is for 0.062-in. FR-4 board. At 100 seconds, the thermal resistance is 100°C/W for an SO-8 package. The boards tested were made of 0.022-in. outer layers and a 0.012-in. inner layer laminated with 1-oz. copper. Board areas tested were 3 , 2, and 1 in^2. In addition to testing this material with varying board areas, these boards were tested with copper on all sides, and with top copper removed.

Table 1.

Time (sec.)	$R_{\theta JA}$ Cu Two Sides (°C/W)			P_{MAX} Cu Two Sides (W)		
	3 sq. in.	2 sq. in.	1 sq. in.	3 sq. in.	2 sq. in.	1 sq. in.
0.005	0.7	0.7	0.7	178.57	178.57	178.57
0.010	1.1	1.1	1.1	113.64	113.64	113.64
0.100	5.0	5.0	5.0	25.00	25.00	25.00
1.000	19.0	19.0	18.9	6.58	6.58	6.61
10.000	52.4	52.3	52.1	2.39	2.39	2.40
50.000	59.7	61.8	67.3	2.63	2.09	1.86
75.000	61.9	65.3	72.2	2.09	2.02	1.73
90.000	63.1	67.6	74.3	1.98	1.85	1.68
99.000	64.1	68.3	76.3	1.95	1.83	1.64

Table 2.

Time (sec.)	$R_{\theta JA}$ No Top Cu (°C/W)			P_{MAX} No Top Cu (W)		
	3 sq. in.	2 sq. in.	1 sq. in.	3 sq. in.	2 sq. in.	1 sq. in.
0.005	0.7	0.7	0.7	178.57	178.57	178.57
0.010	1.1	1.1	1.1	113.64	113.64	113.64
0.100	5.1	5.0	5.1	24.51	25.00	24.51
1.000	20.5	20.4	20.4	6.10	6.13	6.13
10.000	58.1	58.0	57.7	2.15	2.16	2.17
50.000	67.4	69.0	73.0	1.85	1.81	1.71
75.000	70.4	70.3	78.0	1.76	1.78	1.60
90.000	71.6	71.4	80.9	1.75	1.75	1.55
99.000	72.3	73.4	81.8	1.73	1.70	1.53

The results provide an insight into two parameters affecting the power handling capability of a surface-mounted MOSFET. The first of these is board area. The thermal resistance data is the same for all boards areas and copper configurations through the first second of elapsed time. The effects of the board don't appear until 10 seconds. The reduction in thermal resistance (as the result of increasing board area) follows in inverse square function. At the extremes, enlarging the PC board area from 1 sq. in. to 3 sq. in. on a fully clad board increases the power handling capability by 0.3 W. The same enlargement of board area with top copper removed increases the power handling capability by 0.2 W. Although this absolute increase is small, it is significant as a percentage of the total power handling capability and in terms of the amount of current it represents with the low values of on-resistance available in today's state-of-the-art power MOSFETs.

The second parameter of note is the amount of copper on the top of the board. Especially in the case of the PC board measuring 3 sq. in., the design's power handling capability increases relative to the amount of copper being used. Obviously, it is worthwhile to try to maximize the copper area. Rθ is lower on boards with copper on the top. (The copper areas should be connected to the drain leads as shown in Figure 4.

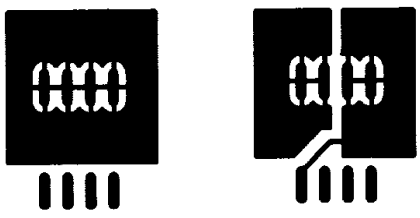

Figure 4. Power MOSFET land pads

This spreads the heat directly from the leads and facilitates the transfer of heat through the top layer of FR-4 and into the internal copper planes.) Note that the pattern shown in Figure 4 includes the area under the MOSFET package. This area is important since the heat spreads radially from the foot.

Thermal Properties of LITTLE FOOT Power MOSFETs

An actual board layout would occupy at least 3 sq. in. of board space. After adding the appropriate copper planes to the top and bottom, we would expect the power handling capability of the board to be approximately 1.8 W in a 25°C ambient. To obtain a value that is any more precise, we would need to know the device's junction-to-foot thermal resistance, $R\theta_{jf}$ (Kraus, 1983). This specification allows us to make thermal measurements in an active circuit, confirming that it is operating within acceptable limits. It also allows a thermal model to be generated and performance to be predicted.

Looking at the package cross-section again, the major thermal paths are 1) junction to lead frame to PC board, and 2) the junction through a thin section of the molding compound to the gate and source, leading to the PC board. The poor conductivity of the molding compound eliminates other paths as a consideration. Calculation of a lumped parameter $R\theta_{jf}$ requires the calculation of the $R\theta_{jf}$ for the drain leads, the gate lead, and source leads separately. Schematically, the thermal circuit is shown in Figure 5.

For a dual-die LITTLE FOOT package, the $R\theta_{jf}$ for the two paralleled drain leads was calculated as 50°C/W, and the parallel combination of the gate and source leads were calculated to be 135°C/W. To arrive at a lumped parameter value of $R\theta_{jf}$, the temperature of all feet must be the same. This approach is equivalent to measuring the $R\theta_{jf}$ on an infinite heat sink. The two values are paralleled, giving a final value of $R\theta_{jf}$ = 35.6°C/W.

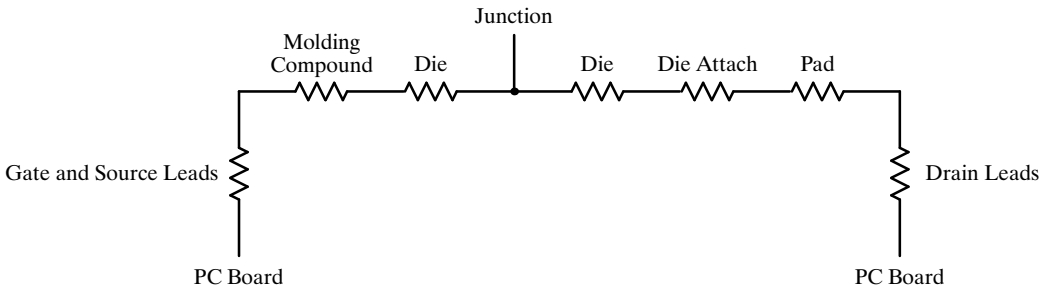

Figure 5. Power MOSFET thermal model

The measurement of $R\theta_{jf}$ follows the standard procedure of attaching the device under test to a large block of copper, i.e. an infinite heat sink. A known amount of power is dissipated in the device for a specified interval, and the junction and the drain and source foot temperatures are measured. The drain, gate, and source foot temperatures are the same since they are attached to the infinite heat sink. The thermal characteristics of the device are independent of the substrate material it is mounted on. The steady state value of Rθjf was thus measured at 37°C/W, which correlates well with the calculated value.

With the LITTLE FOOT defined thermally, the next step is to determine the steady-state junction temperature in a functional circuit by measuring the temperature of the foot.

Using the temperature of the drain lead, $R\theta_{jf}$, and the power dissipated in the MOSFET, we can calculate the approximate junction temperature. The calculated figure will be higher than the actual junction temperature. $R\theta_{jf}$ is a lumped parameter combining all the feet in parallel at the same temperature. In an actual application, the drain foot temperature is higher than the temperature of the other feet, due to the lower $R\theta_{jf}$ for the drain foot and the low conductivity of the PC board. Typically, the difference between the drain foot temperature and the temperature of the other feet is only a few degrees.

Assuming that all the feet are at the higher temperature will yield a calculated junction temperature that is higher than actual and therefore conservative.

Thermal Properties of the PC Board

Now that the MOSFET has been defined, the missing variable is the PC board, which can be found using the diffusion equation

$$\frac{\partial}{\partial t} T(x,t) = -c_v \cdot k \cdot \nabla^2 T(x,t)$$

Assuming that the system is at steady state, and that conductivity (k) is constant,

$$-k \cdot \nabla^2 T(x) = 0$$

Heat is typically removed in proportion to the difference between the board temperature and the ambient temperature,

$$\underset{\text{(Net heat thru board)}}{-k \cdot \nabla T(x)} = \underset{\text{(Heat removed by air)}}{\chi_a \cdot \left(T(x) - T_a\right)}$$

Changing to cylindrical coordinates and rewriting the equation as a hyperbolic Bessel equation yields

$$r^2 \frac{d^2}{dr} T(r) + r \frac{d}{dr} T(r) - r^2 \frac{\chi_a \cdot (T(r) - T_a)}{k} = 0$$

Solving for T(r)

$$T(r) = c \cdot K_0\left(r \cdot \sqrt{\frac{\chi_a}{k}}\right) + T_a$$

By examining heat flow close to the origin where air has little effect,

$$c = \frac{H}{2 \cdot \pi \cdot k}$$

where H is the power introduced at the origin. This approximation is valid when the heat is introduced within a radius which is less than

$$\sqrt{\frac{k}{\chi_a}}$$

Substituting for c,

$$T(r) = \frac{H}{2 \cdot \pi \cdot k} \cdot K_0\left(r \cdot \sqrt{\frac{\chi_a}{k}}\right) + T_a$$

Hence, we can calculate board temperature as a function of radius for a given amount of heat introduced to the system. This gives us a method of determining the thermal resistance of a board from a small region to the ambient air.

Up to this point, it has been assumed that the boards in question were of infinite size. For boards of finite size, the boundary condition is no longer

$$t(r) \to 0$$

when the value of r is large, but rather

$$\frac{d}{dr} t(r) = 0$$

at the edge of the board. This is because heat cannot flow past the edge of the board. This condition can be accounted for by using the general solution to the hyperbolic Bessel equation

$$R(r) = \frac{1}{2 \cdot \pi \cdot k} \cdot K_0\left(r \cdot \sqrt{\frac{\chi_a}{k}}\right) + \frac{c_3}{2 \cdot \pi \cdot k} \cdot I_0\left(r \cdot \sqrt{\frac{\chi_a}{k}}\right) + T_a.$$

The value of c_3 calculated by setting the derivative of R(r) equal to zero at the edge of the board.

This equation can be used to calculate the effect of the pins on each other by using the distance between adjacent and opposite pins. The resistance from the board under a given pin to the air is calculated by using the equivalent radius of that pin. Since the diffusion equation is linear, the total resistance is calculated by adding the effects of all pins weighted by the their respective ability to introduce heat. For a LITTLE FOOT power MOSFET, the drain pins contribute about twice as much heat as the source pins. In a single-die LITTLE FOOT, all drain pins can be weighted equally. The sum contribution of all pins yields the effective $R\theta_{ba}$ (thermal resistance board to ambient).

$$R\theta_{ba} = \frac{2 \cdot R(fp) + 4 \cdot R(sp) + 2 \cdot R(2 \cdot sp) + R(acr) + 2 \cdot R\left(\sqrt{acr^2 + sp^2}\right) + R\left(\sqrt{acr^2 + 4 \cdot sp^2}\right)}{12}$$

In this equation, fp stands for the foot's equivalent radius, sp stands for the spacing between adjacent pins, and acr stands for the distance between pins opposite one another.

Applying this equation to a four-layer PC board with the 2 inner planes only, each of 1-oz. copper, yields the curve in Figure 6. This curve shows that there is a definite limit to the effectiveness of increasing board area.

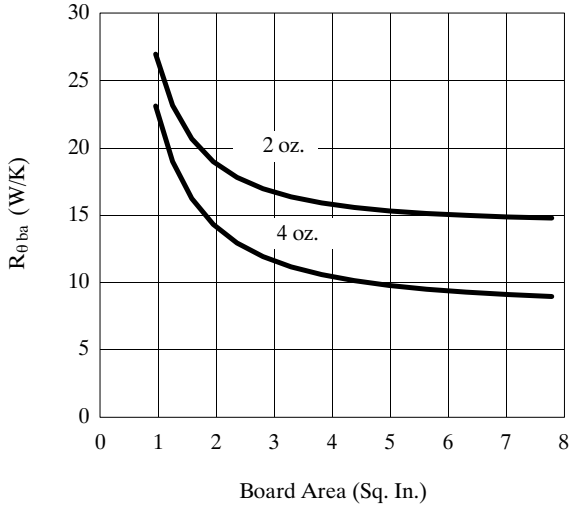

Figure 6. $R\theta_{ba}$ vs. board area

Beyond 7 sq. in., the thermal resistance levels out at approximately 15°C/W. Thermal resistance for 1, 2 and 3 sq. in. are 25.7, 18.4, and 16.3°C/W respectively. When comparing this data with the data presented earlier, the change in resistance between these board areas follows. Increasing the copper to two 2-oz. layers or four 1-oz. layers lowers the minimum resistance to 8°C/W. The curve showing the 4-oz. data is shown in Figure 6 along with the 2-oz. data. Thermal resistance for 1, 2 and 3 sq. in. have dropped to 22.1, 14, and 11.5°C/W respectively. Similar change is seen between the board areas: 2.2°C/W between 1 and 2 sq. in., and 1.3°C/W between 2 and 3 sq. in.

Thermal Properties of Pads and Traces

The values presented do not match those expected because they do not take into account $R\theta_{fb}$, the resistance encountered in the transfer of heat from the foot through the FR-4, into the inner planes. If we look at a cross-section of FR-4 directly under the foot and calculate the thermal resistance across the layer with no fringing, it comes out in excess of 8000°C/W. Obviously, this number is much too high to properly represent the foot in the thermal system. The copper pad to which the foot is soldered has a tremendous effect on the transfer of heat through the board and into the copper plane.

The first step in quantifying the effect of the top metal is to calculate the thermal resistance contributed by the pad to which the foot is soldered. The copper pad is 24 × 80 mils. This is almost five times as large as the contacting area of the foot. Taking into account the spreading that occurs as heat passes through the FR-4, the thermal resistance from the foot to the inner plane has been reduced to 910°C/W.

The next step is to quantify the effect of any traces connected to the pad. To work with traces, the diffusion equation must be solved in one dimension. The starting point is the same as for the solution in cylindrical coordinates:

$$k \cdot \nabla^2 T(x) = \chi_a \cdot \left(T(x) - T_a\right)$$

The ambient can be considered constant and ignored as long the temperature variation in the plane beneath the trace in question varies significantly less than the pad-to-plane temperature difference. Once a design reaches a point where the thermal resistance from a single foot to plane is about 40°C/W, more detailed calculations are required. In one dimension the diffusion equation becomes

$$k_{trace} \cdot \frac{\delta^2}{\delta^2 x} T(x) = \chi_{trace} \cdot T(x)$$

which we can solve as

$$T(x) = T_{Pad} \cdot e^{-x \cdot \sqrt{\frac{\chi_{trace}}{k_{trace}}}}$$

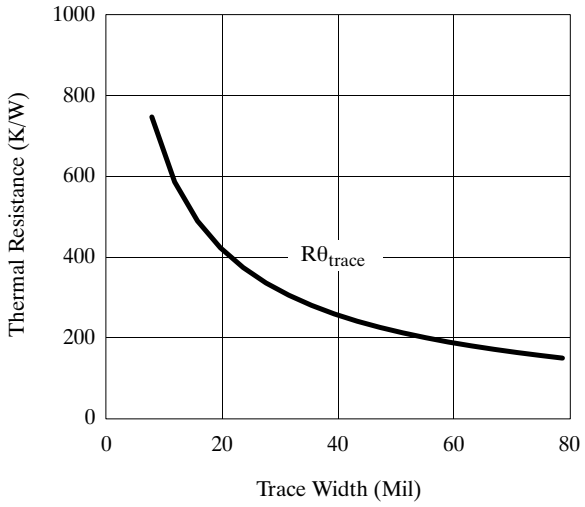

Figure 7. Trace thermal resistance vs. trace width

The heat drawn from the pad by this trace is the trace's conductivity times the derivative of the trace's temperature at the origin. Dividing the pad's temperature by the heat leaving via the trace gives the trace's thermal resistance:

$$R_{\theta trace} = \frac{1}{\sqrt{k_{trace} \cdot \chi_{trace}}}$$

As long as the lead's foot-to-plane thermal resistance is greater than 40°C/W, $R\theta_{fb}$ is approximately the parallel combination of the pad's resistance and the trace's resistance. Figure 7 shows a trace's thermal resistance with respect to its width. These calculations assume that there is a 2-oz. plane or two 1-oz. planes 22 mils beneath the top metal. The top metal is 1-oz. copper.

The Complete Thermal System

Moving on to the full thermal system, solving for the MOSFET and the PC board,

$$R\theta_{ja}(w_{trace}) = \frac{R\theta_{air} \cdot \left(R\theta_{ba} + R\theta_{jf} + \frac{R\theta_{fb}(w_{trace})}{8}\right)}{R\theta_{air} + \left(R\theta_{ba} + R\theta_{jf} + \frac{R\theta_{fb}(w_{trace})}{8}\right)}$$

where $R\theta_{air}$ is twice the $R\theta_{ja}$ of an SO-8 package unmounted in still air and $R_{fb(Wtrace)}$ is the thermal resistance from the MOSFET foot to the board. Rair is twice R_{ja} suspended in still air because the PC board covers the underside of the LITTLE FOOT package. Thus the surface area of the LITTLE FOOT package is cut in half. Figure 8 shows the effect that the width of the traces coming off the feet

have on $R\theta_{ja}$ while mounted on a large PC board. Equivalent curves for other board areas and types can be generated by recalculating the $R\theta_{ba}$ and substituting in the equation above.

This defines the thermal system of a MOSFET and a PC board. However, most circuits have more than one heat-generating component. Just as the equation

$$R(r) = \frac{1}{2 \cdot \pi \cdot k} \cdot K_0\left(r \cdot \sqrt{\frac{\chi_a}{k}}\right) + \frac{c_3}{2 \cdot \pi \cdot k} \cdot I_0\left(r \cdot \sqrt{\frac{\chi_a}{k}}\right) + T_a$$

can be used to calculate the effect of one pin on another, it can also be used to calculate the effect of another heat-generating component on the PC board. The increase in temperature at the MOSFET caused by this second component is defined by

$$\Delta T\left(P_{source2}\right) = P_{source2} \cdot R\theta_{ba}(dist)$$

This temperature rise is then added to the ambient temperature, making the MOSFET's junction temperature

$$T_j = R\theta_{ja} \cdot P_{MOSFET} + T_a + \Delta T\left(P_{source2}\right)$$

Another issue arises when the MOSFET is not mounted in the center of the PC board. In this case, image charges can be used to predict $R\theta_{ba}$ (Jackson 1975). This technique predicts that $R\theta_{ba}$ will double if the MOSFET is mounted near a free-standing edge. If the edge is connected thermally, $R\theta_{ba}$ will be greatly reduced. With this in mind, designers should connect any thermally conductive hardware next to the edge.

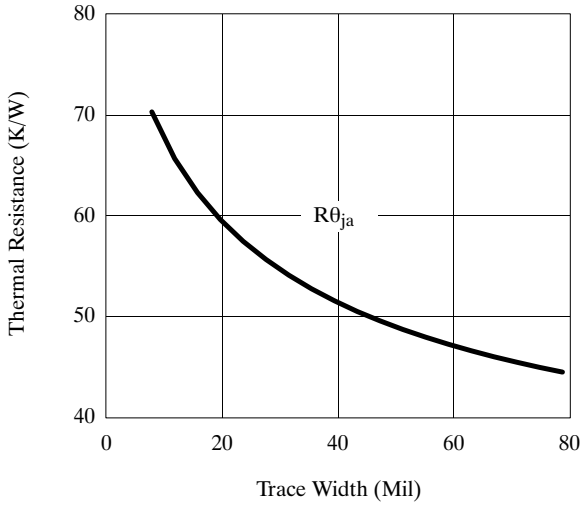

Figure 8. LITTLE FOOT thermal resistance vs. trace width

CONCLUSION

The MOSFET and the PC board can be separated into two entities definable in terms of $R\theta_{jf}$ and $R\theta_{fa}$. This allows measurement of the junction temperature using $R\theta_{jf}$ and modeling of the thermal system using both $R\theta_{jf}$ and $R\theta_{fa}$. If possible, designers should mount the MOSFET to the center of the PC board or near thermally conducting mechanical supports for the best heat distribution and thus lower thermal resistance.

If a MOSFET is mounted next to an edge of the PC board, it is preferable to have the drain feet positioned away from the edge of the board to maximize the board's heat sinking effects. Large mounting pads, large traces, and large copper areas connected to the MOSFET's feet increase the transfer of heat into the inner copper planes, therefore reducing the thermal resistance from the foot to the inner copper planes. Designers should use a minimum trace width of 0.020 in. for a minimum distance of 0.1 in. from the pad. It is important to maintain this aspect of the layout. As Figure 7 shows, the effect of trace width on the MOSFET's power handling capability is dramatic.

Secondary heat sources on the PC board increase the value of ambient temperature used to calculate the junction temperature. $R\theta_{ja}$ is unaffected. The increase in ambient temperature is a function of the power dissipated by the secondary source and of the distance between the MOSFET and the secondary source. Beyond 7 sq. in., however, increases in the area of the PC board will do little to reduce thermal resistance.

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