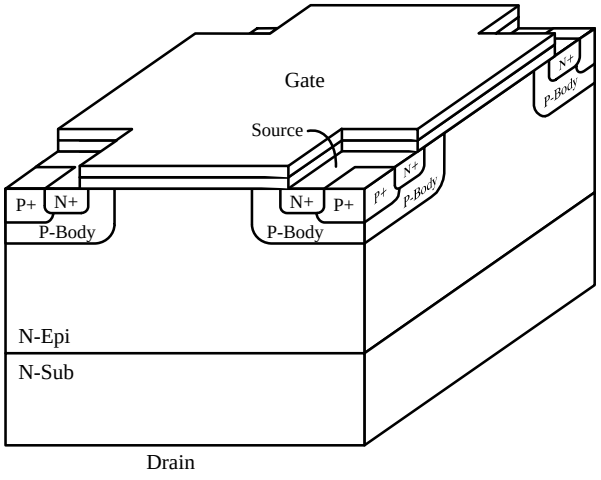
Siliconix Technology Backgrounder: TrenchFET™ Power MOSFETs

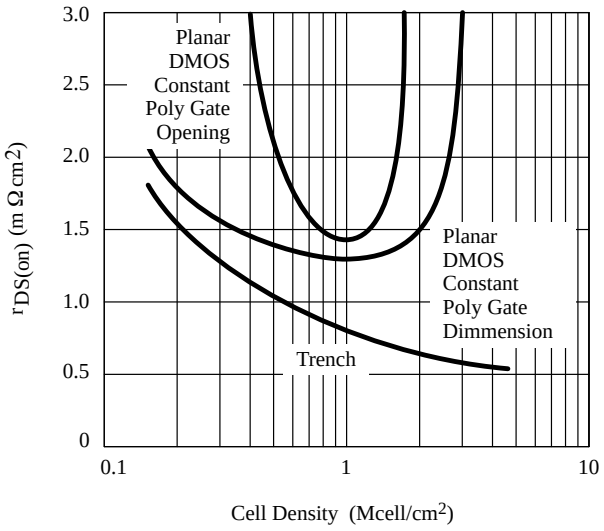
TrenchFETs from Siliconix offer greatly reduced on-resistance compared with any other power MOSFETs in the same package size. The result of many years of development, TrenchFETs offer unparalleled performance in applications from automotive airbags to uninterruptible power supplies.

Most commercially available vertical discrete power MOSFETs are referred to as “planar” because the MOSFET channel formed in the double-diffused region under the gate occurs along the surface of the silicon.



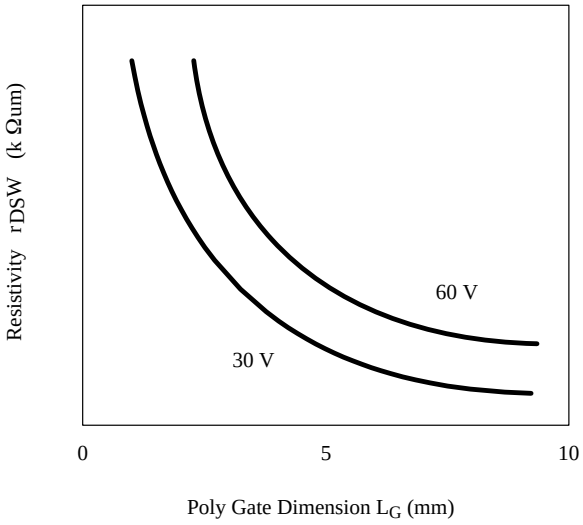
Vertical Planar DMOS Cross Section

The net current flow is vertical because current emanating from the channel must turn and flow *vertically* to the wafer’s backside. While voltage scaling has achieved remarkable performance improvements in planar DMOS devices, their maximum beneficial cell density is fundamentally limited.



Specific On-resistance vs. Packing Density

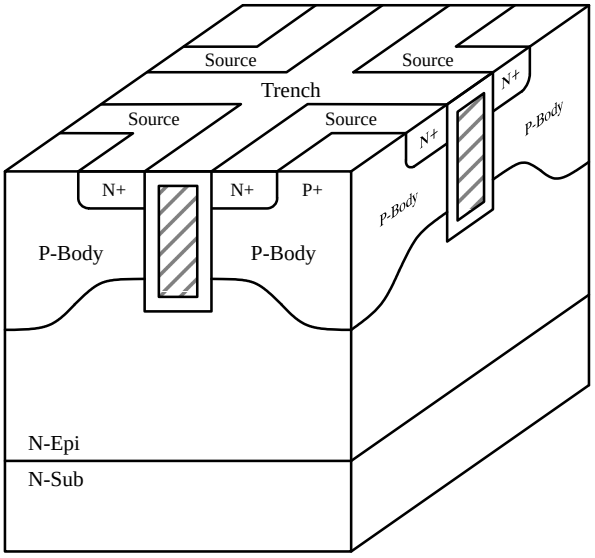
Beyond a certain density, a parasitic junction FET intrinsic to the construction of a vertical DMOS produces a per-cell increase in resistance in proportion to cell density, negating any beneficial effects of a smaller cell size. This phenomenon places an upper bound on cell density, thereby essentially limiting the lowest value of on-resistance achievable by the planar DMOS device type.



Electrical Limit to Scaling

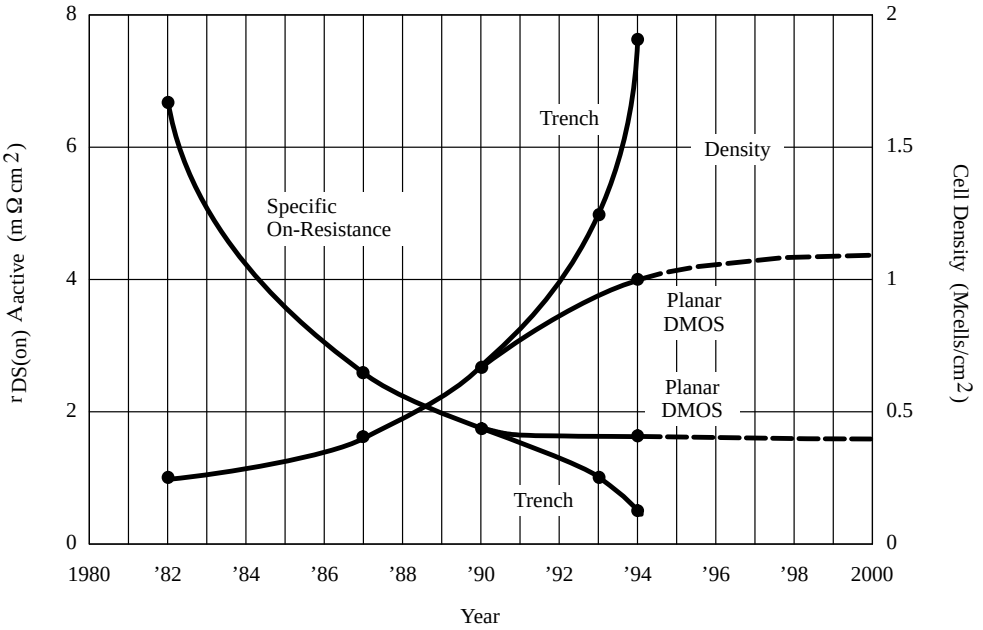
To overcome this restriction, the current flow in the channel of the device must be redirected vertically, in a direct path between the topside source and the backside drain contact. A well-known power device type capable of avoiding the parasitic series JFET problem is the trench or *U-groove* vertical power MOSFET.

While this device has been discussed in the literature for well over a decade, its commercial introduction was delayed by a number of difficult technical and manufacturing challenges.



TrenchFET Power MOSFET Cross Section

In 1994, Siliconix introduced its first generation of TrenchFETs, a family of 60-V power MOSFETs built on an 8 million cells per square inch technology. At 12 million cells per square inch, the newest 30-V TrenchFETs developed at Siliconix have surpassed the 100,000 transistor per chip criterion generally regarded as the minimal definition of VLSI. This transistor count has been achieved in a die assembled in a small-footprint SO-8 (LITTLE FOOT®) package.



TrenchFET Power MOSFET Cross Section

Building on its 60-V TrenchFET expertise, Siliconix has developed a double-diffused 30-V product while effecting yet another 50% increase in cell density. These second generation Trench densities were made possible by optimizing the device for 30-V operation and through a commitment to continuous improvement in manufacturing. At such densities, a DPAK or TO-220 sized die has a transistor count comparable to a 32-bit microprocessor—over 400,000 transistors.