Power Supply Control ICs for Pentium Microprocessor Applications

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Abstract: The growing popularity of Pentium microprocessors requires an equally innovative solution to power supply design. The Pentium requires a converter capable of responding to nanosecond load transients and featuring both a large closed-loop bandwidth and minimal propagation delay times. PWM controllers built on an ultra-fast CBiC/D process are an example of devices that can handle the exacting environment of the Pentium processor while reducing inductance, capacitor size, and cost, without compromising the quality of output voltage regulation. Such devices promise to play a significant role in redefining the capabilities of today's Pentium-based computers, by providing propagation delays below 30 ns, high-frequency operation up to 1 MHz, and closed-loop bandwidths of 100 kHz or more.

I. INTRODUCTION

The demands on CPU microprocessors for faster and more efficient operation are overwhelming today's conventional PC power supply designs. Microprocessor manufacturers have begun to require specific output voltage levels with tight voltage regulations to obtain higher clock speeds and enhance manufacturing yields. On top of this problem, manufacturers have implemented start/stop features into their CPU clock to save power, requiring an ultra-fast response from the power supply.

Intel's Pentium processor gives a perfect example of this new situation. P54C-VR and P54C-VRE processors require respective static and transient regulations of $3.3825V \pm 0.0825$ and $3.525V \pm 0.075$ for all load conditions.[1] No overshoot or undershoot are permitted, irrespective of their duration. VR series Pentium processors are designed to operate at 75 MHz, while VRE series are geared for 100-MHz operation. Current demand for the P54C family can vary from 0.2 A to 7 A with current transient of 4 A within the minimum to maximum current range. The 4-A transient occurs in approximately two clock cycles or 20 ns.

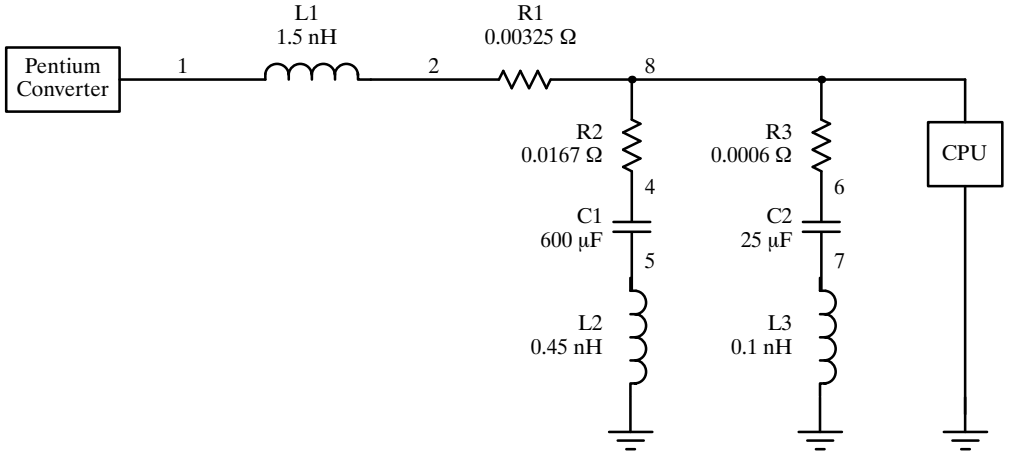

Figure 1. Pentium converter decoupling network

There are many ways to design a converter to meet the requirements of the Pentium processor. Given the range of options, it may be difficult to pinpoint the exact specifications necessary to meet the processor's requirements. Obviously, the greater the decoupling capacitance, the easier it is to provide adequate transient regulation. Cost and space constraints limit the usefulness of capacitance beyond a certain point. The Pentium's manufacturer has recommended the use of six 100-µF low-ESR tantalum capacitors and 25 1-µF ceramic capacitors. Figure 1 shows the typical test set-up of the Pentium converter. There is a direct relationship in any such design between output capacitance and transient response. The greater the output capacitance, the less bandwidth required to provide adequate transient regulation. A simple simulation with output capacitance characteristics of 800 µF and 0.0125 Ω reveals that a converter with 12-µs response time will provide adequate transient voltage regulation for the VRE Pentium processor (Figure 2).

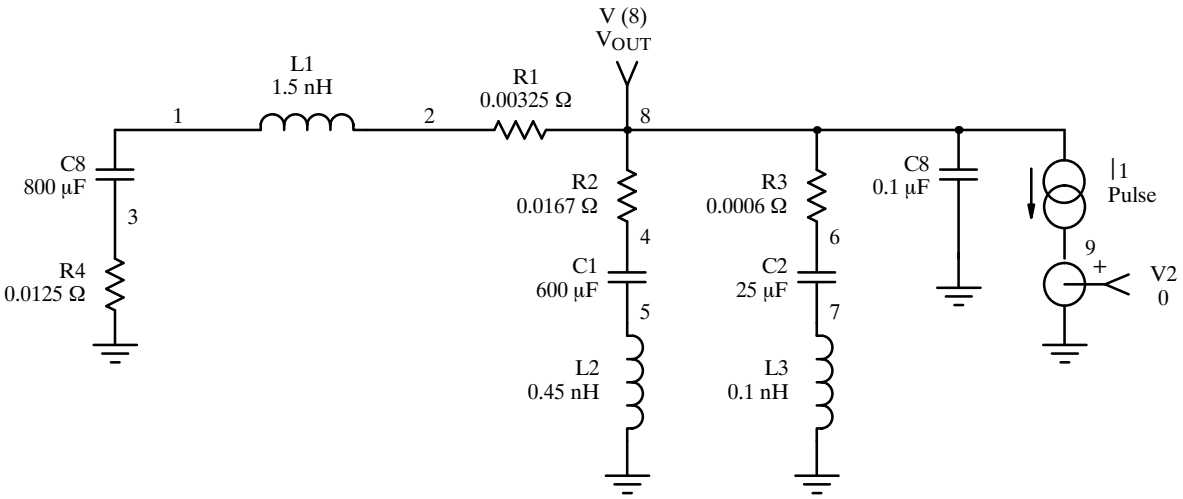

Figure 2. 4-A transient test

Figure 3 shows the response to a 4-A transient. Assuming a second-order response converter with a damping coefficient of 0.9, the result is a unity gain bandwidth of about 40 kHz. In reality, approximately 25% of the requisite regulation limit will accommodate variations in the reference voltage and resistor devices. Furthermore, to increase power supply manufacturing yields, it is wise to allow an additional voltage regulation tolerance of 10% or more, which in turn will increase the bandwidth requirement. If remote sensing is not available, further drops will result from delayed sensing of the processor voltage.

Together, these constraints reduce the regulation limit from ±75 mV to ±45 mV. To meet a ±45-mV regulation limit requires a converter unity gain bandwidth of 100 kHz or greater. Obtaining bandwidth of 100 kHz typically requires a converter switching frequency of 375 kHz or greater. It also requires an ultra-fast error amplifier. Typically, a minimum error amplifier bandwidth of 10 to 20 times the switching frequency is required for the amplifier to respond correctly to the stimuli. In the case of the Pentium converter, large bulk capacitors at the output of the converter and at the microprocessor require even greater bandwidth.

In the past, linear regulators were the ideal solution for low-power, 5-V/3-V conversion. Linear regulators provided an inherently quiet power system, eliminating EMI/EMC problems. Stability and compensation issues were also minimal, making the application and analysis as simple as possible. The advantages of linear regulators remained significant until power demands increased. Under these new conditions, their disadvantages become obvious. With a 7-A output current, a VRE converter will dissipate over 10 W of power into an already blazing hot system, requiring cumbersome heat sinks. These increase manufacturing difficulties and labor costs, which could easily offset the price advantage of the linear regulator solution. Meanwhile, the physical dimension requirements—2.60 × 1.81 × 0.8 inches—could be easily exceeded with a large heat sink. And finally, the 35-W input power violates the popular progression towards Energy Star compliance.

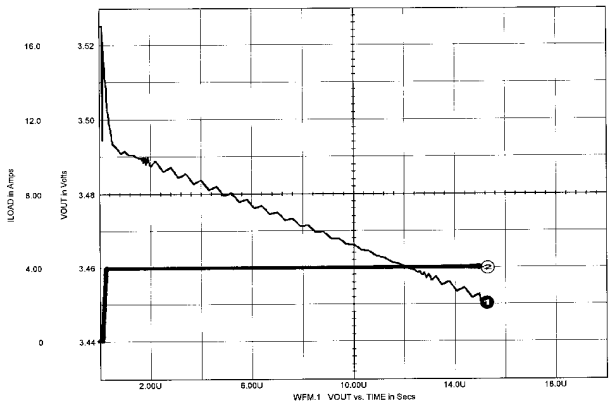

Figure 3. Transient response

Unable to fit the linear regulator designs into the dimensional outline of the Pentium power module, power supply designers have been forced to use a switching regulator solution. Even with switching power supply designs, however, designers haven't had much success in meeting the Pentium's tight transient requirements. Conventional current mode switching power supplies with operating frequencies of 250 kHz and below are unable to produce the necessary bandwidth to provide adequate transient voltage regulation.

The need for PWM controllers with high switching frequencies and error amplifier bandwidths has become more evident as designers seek to meet the voltage regulation requirements of Pentium microprocessors.

II. PWM CONTROLLER IC

A. Current Mode vs. Voltage Mode

The Pentium's exacting dynamic load requirements makes it crucial for the designers to choose an optimal control method to provide voltage regulation during the transients. There are two modes of control for a buck converter operating in fixed frequency: voltage mode or current mode. In voltage mode, an output voltage is controlled by comparing error voltage to an artificially generated ramp signal. In current mode, output voltage is controlled by comparing error voltage to the peak inductor current. Therefore, in current mode, there are two loops which control the output voltage. The inner loop senses the peak inductor current and outer loop senses the output voltage (as in conventional voltage mode). Both modes of operation have their advantages, so one should choose carefully to fit design needs.

Current Mode Control

Current mode control offers the advantage of monitoring the inductor current. The transfer function of the current mode converter's small signal loop gain from output to control voltage operating in continuous inductor current has been derived using the state space averaging model stated below.

$$V_{OC} = \left(\frac{R_L}{R_{cs}}\right) \times \left[\frac{1}{\left(1 + S \times C_O \times R_L\right)}\right]$$

R_L = load resistance
R_{cs} = current sense resistance
C_O = output capacitance

As the above equation shows, current mode control has inherently good input line regulation since the transfer function is unaffected by the input voltage. The slope of the inductor current changes instantaneously to compensate for intput voltage variations.

Unfortunately, loop gain is load dependent. As the output load varies from minimum to maximum, as in the case of the Pentium, R_L ranges from 0.5 Ω to 17.6 Ω, and the loop gain varies by approximately 31 dB. This could cause the power supply to oscillate, if the loop is not compensated correctly for all load conditions. Typically the power supply is compensated for the maximum load resistance and the design must somehow accommodate the loop bandwidth reduction during the minimum load resistance. With -1 slope, loop bandwidth can decrease by more than 1.5 decades in frequency. This decrease in bandwidth could have catastrophic effects on the dynamic transient response of the Pentium. If the required output voltage level is violated, the results can be devastating, ranging from an obvious, flagged software/hardware error to insidious, subtle, and unpredictable computational errors.

A current mode converter provides automatic pulse-by-pulse current limiting by detecting the inductor current. It also eliminates inductance from the loop gain and reduces the system characteristic order from double-pole to single-pole. The Q-ing of the LC filter is eliminated and replaced with a simple RC filter. This allows a simpler feedback compensation network to be utilized.

Current mode conversion may reduce noise immunity, particularly if the slope of the inductor current is too small to increase efficiency. Since the ramp voltage always close to the error voltage, even a small noise injection into the current ramp could cause large variations in the duty cycle.

Current mode conversion also requires a slope compensation for duty cycles greater than 50%, to cancel the instability introduced by detecting the peak inductor current. For 5-V to 3.525-V conversion, the duty cycle exceeds 70% without counting FET and parasitic losses. Both poor noise immunity and operation above 50% duty cycle can be corrected at the same time with slope compensation, which can be easily implemented with only a few discrete components.

Voltage Mode Control

The voltage mode control buck converter's small signal loop gain equation from output voltage to control voltage operating in a continuous inductor current is stated below.

$$V_{OC} = \left(\frac{V_{IN}}{V_S}\right) \times \left[\frac{1}{\left(1 + S \times \left(\frac{L}{R_L}\right) + S^2 \times L \times C_O\right)}\right]$$

V_{IN} = input voltage
V_S = ramp voltage
L = inductance

In the voltage mode control converter, loop gain is function of input voltage instead of load resistance. Load resistance affects the Q-ing of the converter. Since the input voltage of the Pentium converter is virtually fixed, loop gain is considered constant. Input voltage for the Pentium varies

from 4.75 V to 5.25 V, less than 1 dB variation. With the loop gain constant, the converter's bandwidth can be maximized and that same wide bandwidth can be maintained, irrespective of load changes. Therefore, the voltage mode controlled converter is an ideal control method for Pentium converter. With virtually fixed input voltages and a wide load variation, bandwidth can be maximized and transient response times minimized.

Voltage mode control does have a disadvantage. As revealed in the above equation, its double pole filter is generally more complicated to compensate than the single pole filter of current mode control. This means the addition of a pole-zero pair compensation network. Even with this small disadvantage, the advantages of voltage mode control far outweigh its drawbacks for the Pentium application.

B. Ultra-Fast CBiC/D Process

To implement a high-speed PWM control IC capable of maintaining a precise output voltage under both static and dynamic load conditions, a low propagation delay comparator and a wide bandwidth error amplifier are mandatory. Historically, these analog subcircuits were designed using all-bipolar or all-MOSFET based process technologies. Even more recent BiCMOS technologies are generally limited to NPN devices. Without a high-speed PNP, the variety and flexibility of analog subcircuits is compromised. Moreover, most bipolar and BiCMOS technologies are optimized for digital applications. But one effect of this optimization is to sacrifice the bipolar's small signal output impedance (i.e. Early voltage) in exchange for a high unity gain frequency (ft). This tradeoff makes present-day CMOS or bipolar technologies poor candidates for analog and mixed-signal circuit implementations at high operating frequencies.

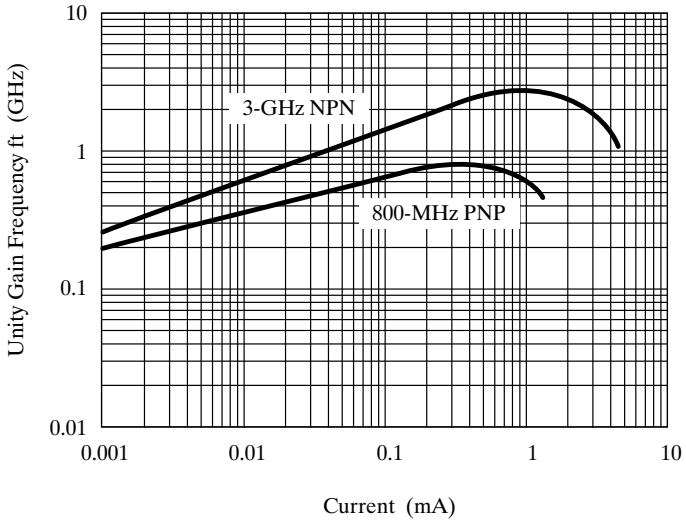

Figure 4. Bipolar fts as a function of collector (drain) current

To avoid such tradeoffs, Siliconix developed an innovative mixed-signal fabrication technology combining CMOS, complementary bipolars, and double diffused (DMOS) power transistors. This CBiC/D process is one of the first IC technologies targeted for low-voltage high-speed power conversion applications. The process is truly complementary, since both NPN and PNP device types are fully isolated three-terminal components employing dedicated base diffusions. They are optimized for a high Early voltage, current gain, and ft. Figure 4 illustrates the measured current dependence of ft for both polarity bipolars available in this process. The NPN's peak ft approaches 3 GHz while the PNP exceeds 800 MHz. This performance is more than 10 times that of conventional analog bipolar devices. These ultra-fast bipolars are integrated to produce 25-MHz unity gain bandwidth error amplifiers (Figure 5). The 25-MHz E/A provides more than ample bandwidth to minimize converter response time. Beyond their high-speed capability, the complementary bipolars are particulalry advantageous when minimizing the influence of process perturbations on temperature compensated circuits operating at low supply voltages. This is an important feature when maintaining extremely tight regulation tolerances. Aside from their application in a switcher's main control loop, the bipolars are useful in current mirrors and in a bandgap voltage reference.

To maintain good transient load regulation in a high-speed PWM controller, it is important to minimize the total loop propagation delay from the error amplifier input to the gate of the power MOSFET. Within this control loop, CMOS facilitates gating and logic functions, the most critical of which is the inverter cascade driving the gate of the external power MOSFET. Starting with a minimum size gate, each inverter in the chain drives another inverter of increasing size, incrementally increasing the output current stage-by-stage.

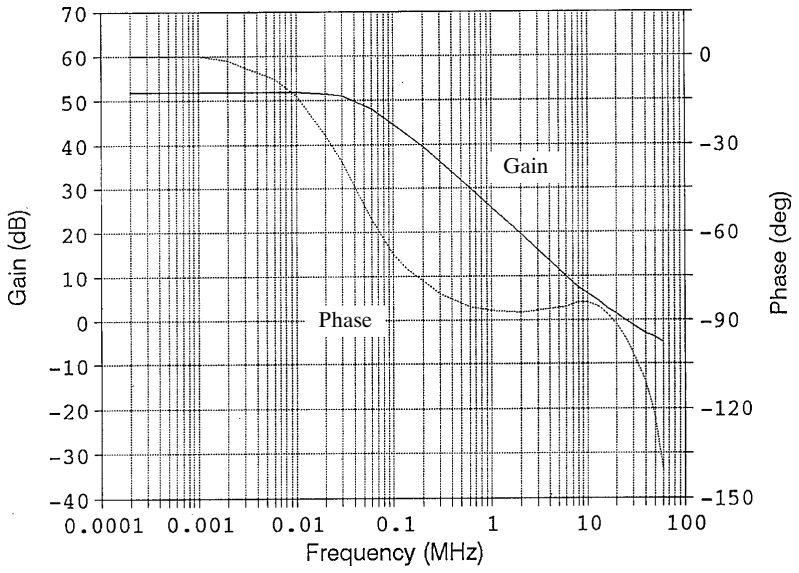

Figure 5. Bode plot of error amplifier

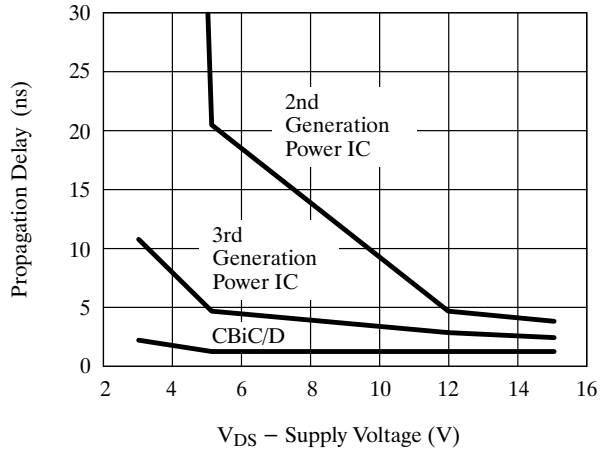

Figure 6. Supply voltage dependence of CMOS propagation delay for three generations of mixed signal technology

Since any given inverter can only drive a certain amount of capacitance at high speeds, the size increment between any two inverters is limited, thereby mandating this multi-stage approach. Unfortunately, the addition of each stage adversely contributes to the total loop propagation delay of the converter. By using a fully self-aligned 2-µm CMOS technology in the CBiC/D process [4], the per stage propagation delay is reduced to around 2 ns at 4.5 V, significantly better than its technological predecessors (Figure 6). Total propagation delay time from the enable pin to the output in the Si9145 is less than 35 ns, providing almost error-free transient response.

The last inverter must be capable of driving the MOSFET's input capacitance, a value which scales inversely with on-resistance. For power levels consistent with the Pentium converter, the total MOSFET capacitance of the buck switch can be nearly 10 nF, making a high output current capability

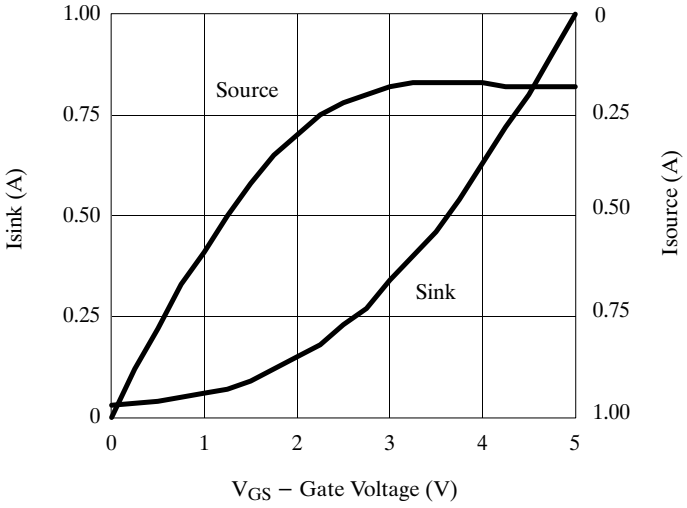

Figure 7. Sink and Source Current

capability mandatory. In Siliconix' CBiC/D process, the output stage can be sized to sink and source transients over 800 mV at 5 V with minimal silicon real estate (Figure 7). Even with this drive capability it is desirable to minimize the input capacitance of the power MOSFETs for any given on-resistance.

III. HIGH DENSITY COMPLEMENTARY TRENCHFETS

Siliconix is the world's first supplier of the trench gated power MOSFET or TrenchFET [5]. Unlike conventional vertical DMOS power transistors whose channel is formed along the silicon surface, the trench power MOSFET has its channel region located on the sidewall of a silicon etched trench (Figure 8). This trench is lined with gate oxide and filled with heavily doped polysilicon gate electrode. Because the current flow is purely vertical with its top-side source, back-side drain, and sidewall channel, the TrenchFET achieves a higher cell density than that possible with other technologies. At 30 V and below, Siliconix TrenchFETs utilize a cell density of 12 million cells per square inch, nearly four times that of industry standard devices. Even including parasitic resistances such as the package, bond wire, and metallization, these 30-V n-channel TrenchFETs exhibit on-resistances from a half to a third comparable area conventional devices. The relative improvement offered by p-channel TrenchFETs is even more substantial.

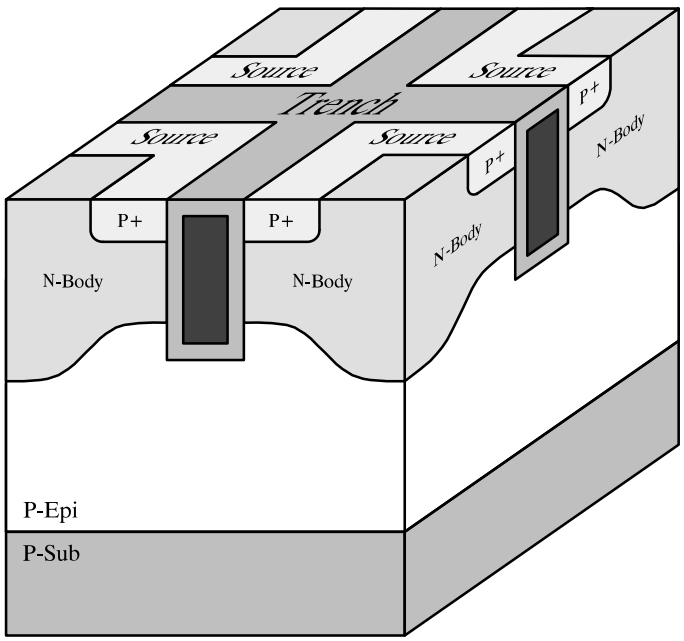

Figure 8. Trench DMOS power MOSFET cross section

For the Pentium converter, Siliconix' 30-V TrenchFET technology offers unprecedented switch performance in small-footprint surface-mount packages. The Si4410DY, an n-channel LITTLE FOOT device, has an on-resistance of only 17 m at 4.5 V of gate drive in a SO-8 package. The comparable area p-channel device, the Si4435DY, exhibits a typical resistance of 26 mΩ. By paralleling two p-channel Si4435DYs as the buck switch and employing one Si4410DY as the synchronous rectifier, the Pentium converter can deliver a continuous 7 A at 3.525V, i.e. 24.675 W to the microprocessor while dissipating only 0.86 W during conduction. In other words, TrenchFET technology virtually eliminates conduction losses in dc-to-dc conversion.

Surprisingly, the TrenchFET also reduces the gate drive losses in a high-speed switcher. Although its per-area input capacitance is slightly higher than the planar MOSFET, its drive requirements are 40% lower for a given on-resistance. The significant equivalent input capacitance is not, however, the value of Ciss as specified on the data sheet. Instead, in the Pentium converter, the value of gate charge at Vgs = 5 V is the critical parameter. Using the relation Ceq = Qgate/Vgs, the input capacitance is increased predominately due to the Miller effect (a phenomenon where the gate-to-drain capacitance is amplified by voltage gain during switching). Since the TrenchFET has a smaller drain-to-gate overlap area, its feedback capacitance, and hence input capacitance, is reduced. Figure 9 compares the equivalent input capacitance of N- and P-channel TrenchFETs to conventional MOSFETs at Vgs = 5 V after normalizing all data for a 17 mΩ switch resistance. Clearly, the TrenchFET offers lower gate drive losses in addition to lower conduction losses. Complementary 30-V LITTLE FOOT devices built on trench technology are well matched to the output drive capability of the Si9145 in implementing a Pentium converter.

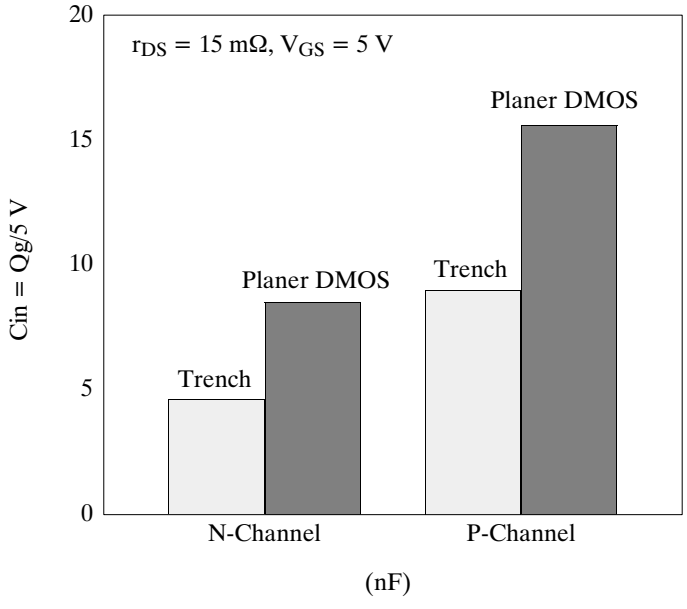

Figure 9. Total gate capacitance of Trench vs. Planer MOSFET

IV. CONVERTER PERFORMANCE

A. The Advantages of Higher Switching Frequencies

Maintaining the output voltage regulation within the ±45-mV range during a 4-A current transition is hardly a trivial matter. Power supply designers are realizing that conventional PWM ICs operating at 100-200 kHz cannot generate sufficient bandwidth to maintain sufficient regulation. Without a voltage mode PWM IC capable of operating down to 4.5 V and switching at 375 kHz or above, designs are forced to operate at much lower switching frequencies. This may provide greater efficiency, but much greater inductance and capacitance will be required to maintain the same ripple voltage. Design size and cost increase as well. The increase in inductance also has a detrimental effect during dynamic load transients. During the transition from maximum to minimum load, energy stored in the inductor makes a forced discharge into the output capacitance. This phenomenon is illustrated by the following energy equation:

$$E = \frac{1}{2} \times L \times \left(Ip_2{}^2 - Ip_1{}^2\right) = \frac{1}{2} \times C_O \times \left(V_{O2}{}^2 - V_{O1}{}^2\right)$$

The larger the inductor, the more energy is stored, causing larger overshoot on the output voltage during the unloading transition. During the minimum to maximum current transition, larger inductors delay the ramping of current demanded by the load, further sagging the output voltage.

Two separate converters were built to demonstrate the advantages of higher switching frequencies, with the following specifications:

	Converter 1	Converter 2
Switching frequency	125 kHz	375 kHz
Bandwidth	33 kHz	100 kHz

The inductance and capacitance of the 375-kHz converter were increased by a factor of three to maintain the same ripple current. Schematics of the two converters are shown in Figures 10 and 11 respectively. Figures 12 and 13 show the dynamic response to 4-A transients. Figures 14 and 15 show the bode plots of the two converters. Notice that settling times are faster for the 375-kHz converter by a factor of three. Amplitude regulation was almost identical for both converters. But the 125-kHz converter's output capacitor, inductor size, and inductor value had to be increased by a factor of three to maintain this level of consistency. Its +45-mV transient regulation reaffirms the need for a bandwidth of 100 kHz or more to meet the VRE regulation needs of the Pentium processor.

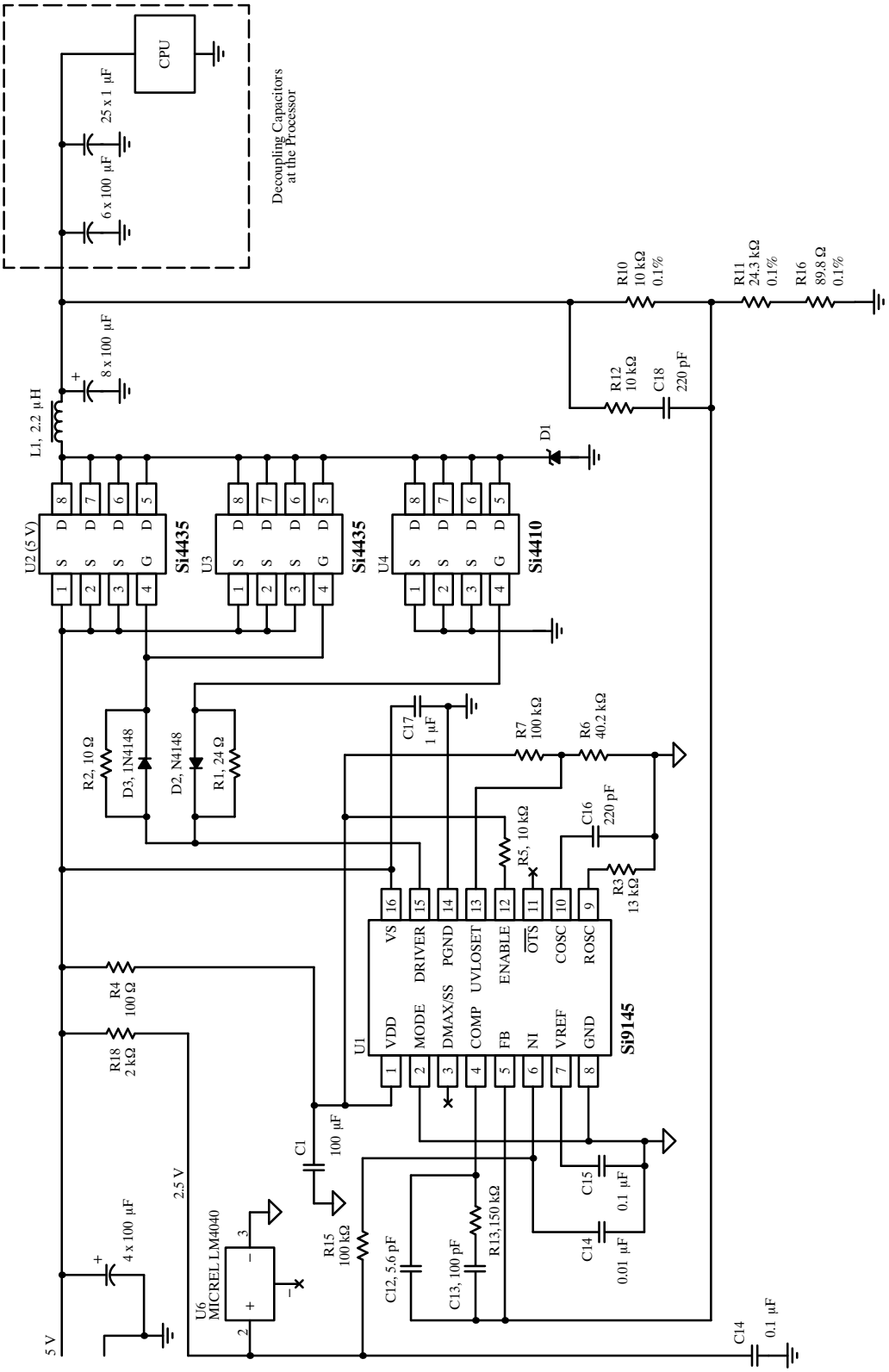

Figure 10. 100-kHz bandwidth

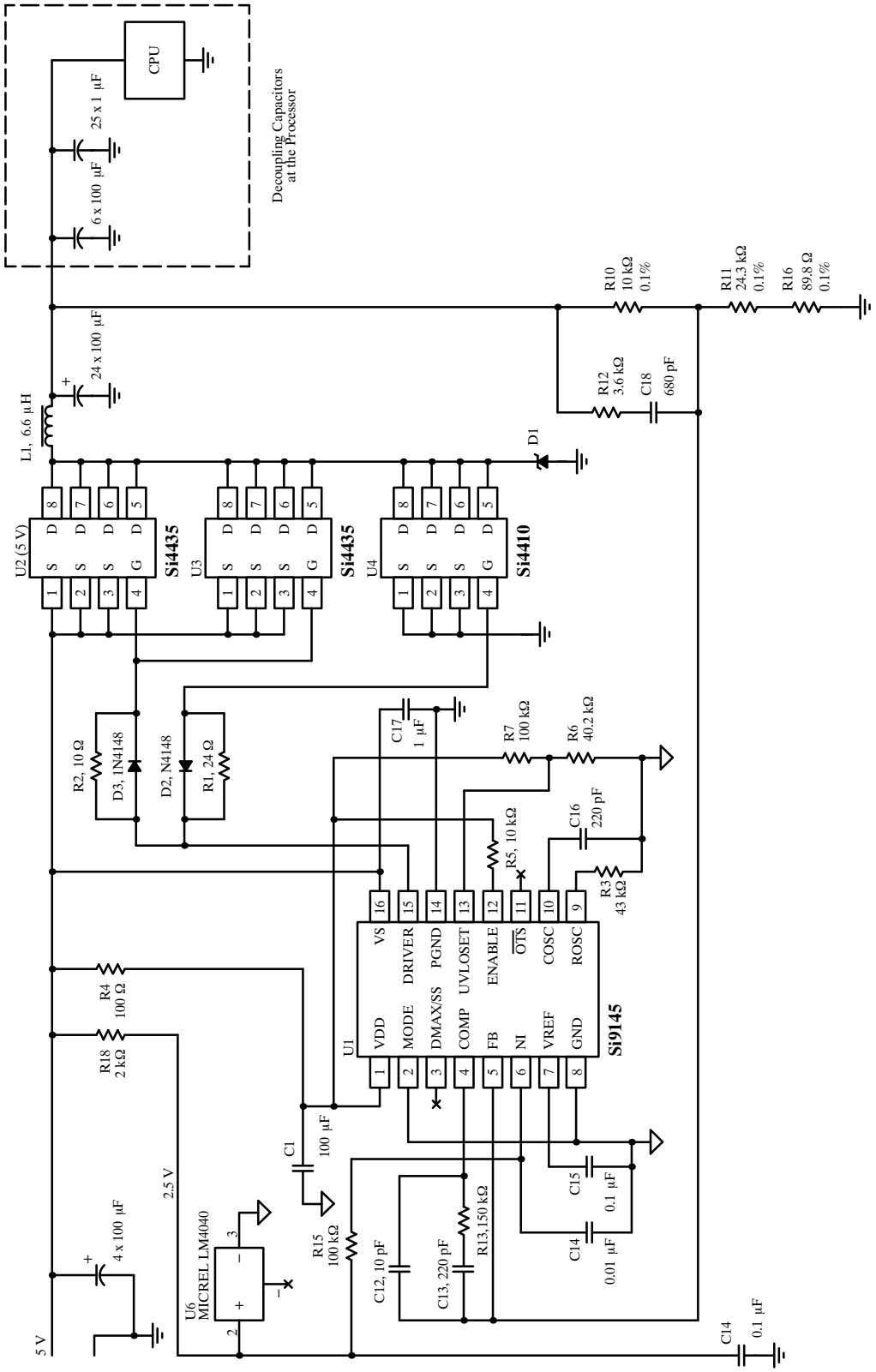

Figure 11. 33-kHz bandwidth

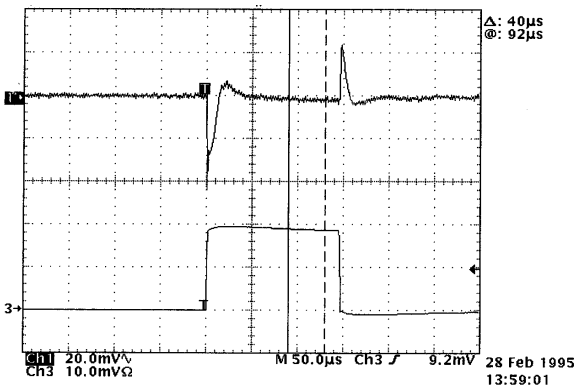

Figure 12. 100-kHz BW transient response

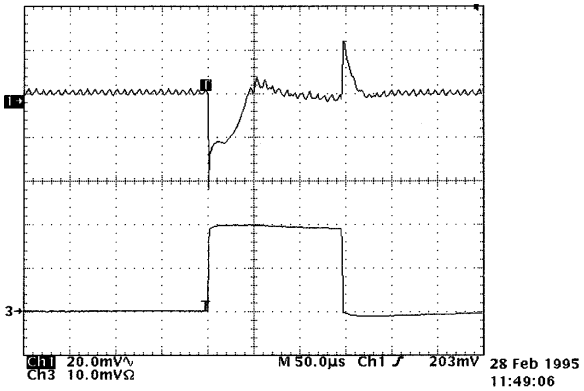

Figure 13. 33-kHz BW transient response

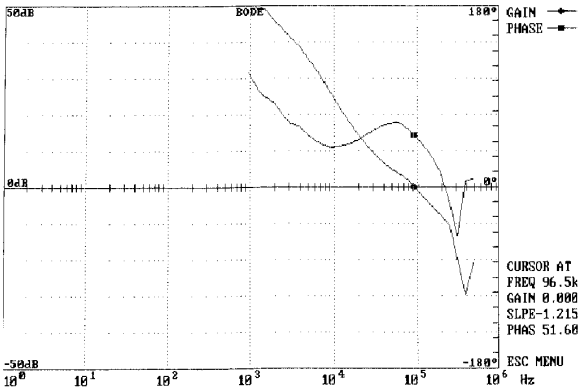

Figure 14. 100-kHz BW Bode plot

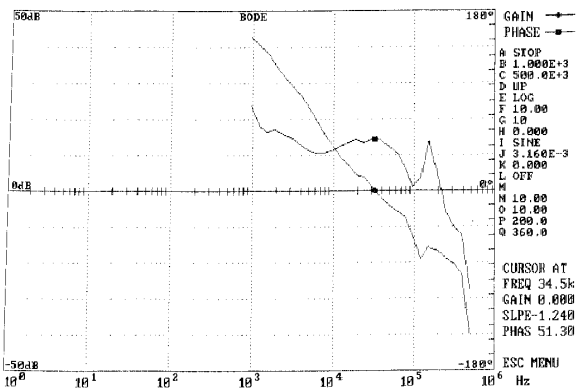

Figure 15. 33-kHz BW Bode plot

B. Synchronous Rectification

A continuous inductor current mode is necessary to sustain the converter's large bandwidth, irrespective of control method (voltage or current). If the mode of operation changes from continuous to discontinuous inductor current mode, the transfer function of the converter will change drastically. If the feedback network was not adequately compensated to handle both modes of operation, the converter is likely to oscillate. The change from continuous to discontinuous mode is also likely decrease converter bandwidth. This is precisely why the synchronous rectification should be utilized.

Synchronous rectification ensures that the converter always operates with a continuous inductor current, regardless of output current. Indeed, even with an output current of virtually zero amps, the inductor current will continue to operate in continuous mode. By maintaining continuous inductor current, the transfer function remains constant and the converter is able to maintain its large bandwidth.

The 375-kHz converter was modified to operate in non-synchronous rectification. Figures 16 and 17 show the bode plots of synchronous and non-synchronous converters operating with a 0.4-A output current. Notice the drastic change in the loop gain characteristics of the non-synchronous converter. Because of the transition into discontinuous inductor mode, the bandwidth of the converter has decreased from 62.5 kHz to 4.2 kHz. A slight decrease in the synchronous converter's bandwidth was also observed when output current was changed from 7 A to 0.4 A. The degradation in performance was caused mainly by extra parasitic losses and inductance change. The decrease in inductor DC biasing caused the inductance value to increase, thus lowering the open loop double-pole frequency.

Synchronous rectification also buys greater efficiency compared with using a Schottky diode, particularly when used in conjunction with low-on-resistance power MOSFETs built on an innovative Trench technology. For example, the Si4410DY TrenchFET™ from Siliconix offers $r_{DS(on)}$ of 0.017 Ω at V_{GS} = 4.5 V. At a 7-A output current, the MOSFET drops only 0.12 V, compared with a typical voltage drop of 0.60 V across the Schottky diode. Efficiency can be increased considerably, since the synchronous rectifier conducts for approximately 30% of the period.

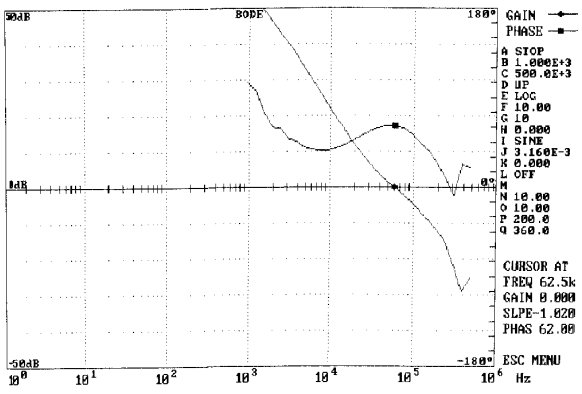

Figure 16. Synchronous rectification Bode plot

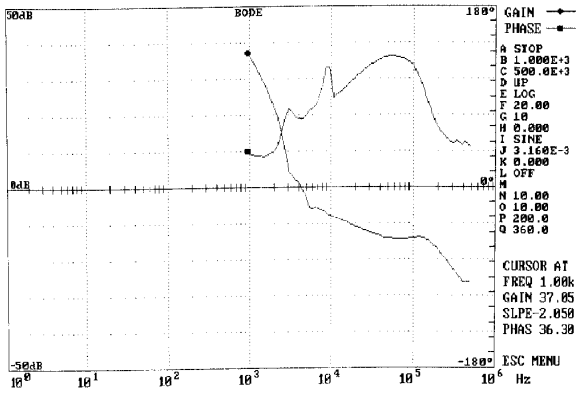

Figure 17. Non-synchronous Bode plot

V. CONCLUSION

The input and output voltage characteristics of the Pentium converter require the use of voltage mode controlled PWM rather than a current mode controller to maintain a wide bandwidth. The Pentium requires a controller IC capable of operating above 375 kHz and with an error amplifier bandwidth in the range of 10 MHz or greater to meet its tight dynamic voltage regulation specifications. Implementation of synchronous rectification allows the converter to maintain the appropriate bandwidth by preventing it from switching into discontinuous inductor current mode. Low on-resistance Trench MOSFETs complete the design, eliminating the need for heat sinks and improving efficiency.

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