# Switching (200V, 5A) 25K2459N

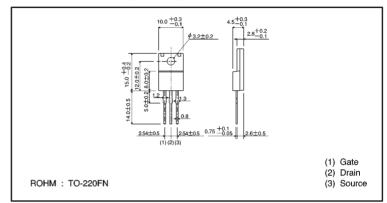
#### Features

- 1) Low on-resistance.
- 2) Fast switching speed.
- 3) Wide SOA (safe operating area).
- 4) Gate-source voltage ( $V_{GSS}$ ) guaranteed to be  $\pm 30V$ .
- 5) Easily designed drive circuits.
- 6) Easy to parallel.

## StructureSilicon N-channel

MOSFET

#### External dimensions (Units: mm)



#### ●Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		Voss	200	٧
Gate-source voltage		Vgss	±30	V
Drain current	Continuous	ΙD	5	Α
	Pulsed	ldp*	20	Α
Reverse drain current	Continuous	Idr	5	Α
	Pulsed	ldrp*	20	Α
Total power dissipation (Tc=25°C)		Po	30	W
Channel temperature		Tch	150	Ç
Storage temperature		Tstg	-55~十150	Ĉ

<sup>\*</sup> Pw≦10 μs, Duty cycle≦1%

#### Packaging specifications

	Package	Bulk
Туре	Code	_
	Basic ordering unit (pieces)	500
2SK2459N		0

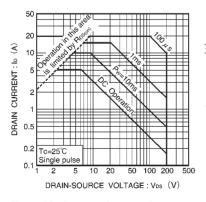


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### ●Electrical characteristics (Ta = 25°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Gate-source leakage	lgss	_	_	±100	nA	V <sub>GS</sub> =±30V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V(BR)DSS	200	_	_	٧	In=1mA, Vgs=0V
Zero gate voltage drain current	loss	_	_	100	μΑ	V <sub>DS</sub> =200V, V <sub>GS</sub> =0V
Gate threshold voltage	VGS(th)	2.0	_	4.0	٧	V <sub>DS</sub> =10V, I <sub>D</sub> =1mA
Static drain-source on-state resistance	RDS(on)	_	0.45	0.65	Ω	In=2.5A, Vgs=10V
Forward transfer admittance	Yfs	2.0	3.5	_	S	In=2.5A, Vns=10V
Input capacitance	Ciss	_	500	_	рF	V <sub>DS</sub> =10V
Output capacitance	Coss	_	150	_	рF	V <sub>GS</sub> =0V
Reverse transfer capacitance	Crss	_	35	_	рF	f=1MHz
Turn-on delay time	td(on)	_	7.0	_	ns	Io=2.5A, Voo≒100V
Rise time	tr	_	15	_	ns	V <sub>GS</sub> =10V
Turn-off delay time	td(off)	_	30	_	ns	RL=40 Ω
Fall time	<b>t</b> f	_	25	_	ns	R <sub>G</sub> =10 Ω
Reverse recovery time	trr		150		ns	IDR=5A, VGS=0V
Reverse recovery charge	Qrr	_	0.7	_	μC	di/dt=100A/ μs

#### Electrical characteristic curves



10 V<sub>De=10V</sub> Pulsed

5 Ta=125°C
75°C
25°C
-25°C
-25°C
0.1
0 1 2 3 4 5 6 7 8

GATE-SOURCE VOLTAGE: V<sub>G</sub>S (V)

Fig.1 Maximum safe operating area

Fig.2 Typical output characteristics

Fig.3 Typical transfer characteristics

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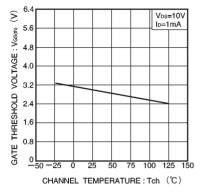


Fig.4 Gate threshold voltage vs. channel temperature

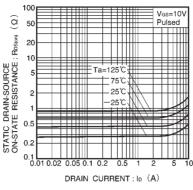


Fig.5 Static drain-source on-state resistance vs. drain current

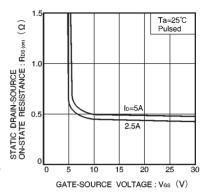


Fig.6 Static drain-source on-state resistance vs. gate-source voltage

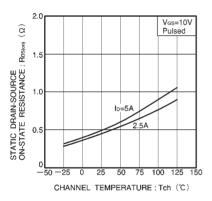


Fig.7 Static drain-source on-state resistance vs. channel temperature

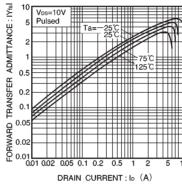


Fig.8 Forward transfer admittance vs. drain current

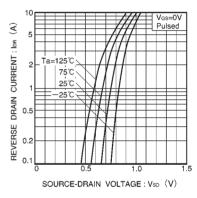


Fig.9 Reverse drain current vs. source-drain voltage

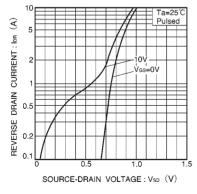


Fig.10 Reverse drain current vs. source-drain voltage

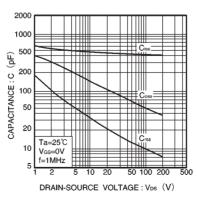


Fig.11 Typical capacitance vs. drain-source voltage

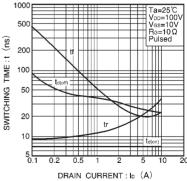
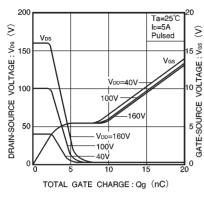


Fig.12 Switching characteristics (See Figures 16 and 17 for the measurement circuit and resultant waveforms)

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2000 Ta=25℃ (su) di/dt=100A/us 1000 Vgs=0V REVERSE RECOVERY TIME: trr Pulsed 500 200 100 50 20 10 L 0.1 0.5 REVERSE DRAIN CURRENT: IDR (A)

Fig.13 Dynamic input characteristics (See Figure 18 for measurement circuit)

Fig.14 Reverse recovery time vs. reverse drain current

Switching characteristics measurement circuit

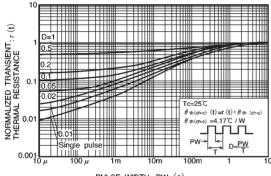


Fig.15 Normalized transient thermal resistance vs. pulse width

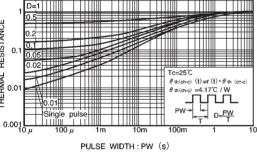


Fig.16 Switching time measurement circuit

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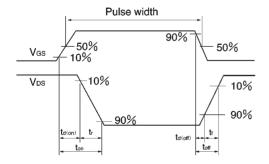


Fig.17 Switching time waveforms

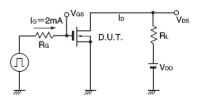


Fig.18 Gate charge measurement circuit

