

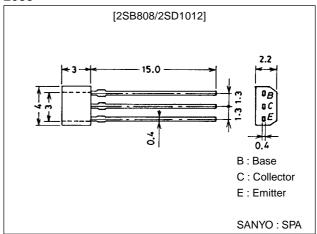
2SB808/2SD1012

Low-Voltage Large-Current Amplifier Applications

Package Dimensions

unit:mm

2033



():2SB808

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V _{CBO}		(-)20	V
Collector-to-Emitter Voltage	V _{CEO}		(–)15	V
Emitter-to-Base Voltage	V _{EBO}		(-)5	V
Collector Current	IC		(-)0.7	Α
Collector Current (Pulse)	I _{CP}		(–)1.5	Α
Collector Dissipation	PC		250	mW
Junction Temperature	Tj		125	°C
Storage Temperature	Tstg		-55 to +125	°C

Electrical Characteristics at Ta = 25°C

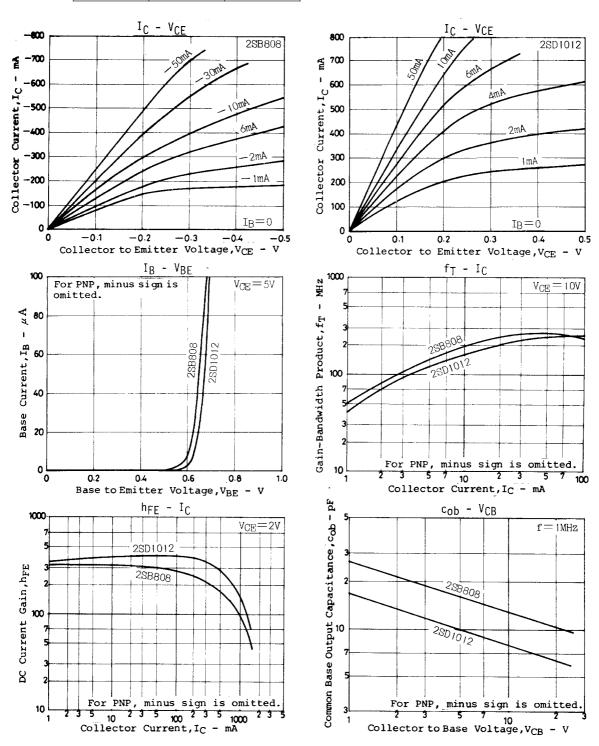
Parameter	Symbol	Conditions		Unit		
Faiametei	Symbol	Conditions	min	typ	max	Offic
Collector Cutoff Current	ICBO	V _{CB} =(-)15V, I _E =0			(–)1.0	μA
Emitter Cutoff Current	I _{EBO}	V _{EB} =(-)4V, I _C =0			(–)1.0	μA
DC Current Gain	h _{FE} 1	V _{CE} =(-)2V, I _C =(-)50mA	160*		960*	
	h _{FE} 2	V _{CE} =(-)2V, I _C =(-)500mA Pulse	80			
Gain-Bandwidth Product	fT	V _{CE} =(-)10V, I _C =(-)50mA		250		MHz
Common Base Output Capacitance	C _{ob}	V _{CB} =(-)10V, f=1MHz		(13)		pF
				8		pF

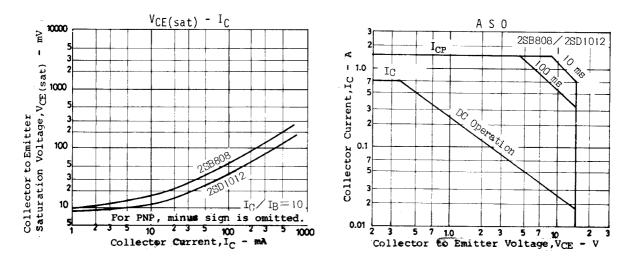
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Parameter	Symbol	Conditions		Ratings			
Farameter	Symbol	Conditions	min	typ	max	Unit	
Collector-to-Emitter Saturation Voltage	V _{CE(sat)} 1	I _C =(-)5mA, I _B =(-)0.5mA		(-15)	(–35)	mV	
				10	25	mV	
Collector-to-Emitter Saturation Voltage	V _{CE(sat)} ²	I _C =(-)100mA, I _B =(-)10mA		(-60)	(–120)	mV	
				30	80	mV	
Base-to-Emitter Saturation Voltage	V _{BE(sat)}	I _C =(-)100mA, I _B =(-)10mA		(-)0.8	(-)1.2	V	
Collector-to-Base Breakdown Voltage	V _(BR) CBO	$I_{C}=(-)10\mu A, I_{E}=0$	(–)20			V	
Collector-to-Emitter Breakdown Voltage	V _(BR) CEO	I _C =(-)1mA, R _{BE} =∞	(–)15			V	
Emitter-to-Base Breakdown Votage	V(BR)EBO	I _E =(-)10μA, I _C =0	(–)5			V	

^{* :} The 2SB808/2SD1012 are classified by 50mA h_{FE} as follows :

2SB808	160	F	320	280	G	560			
2SD1012	160	F	320	280	G	560	480	Н	960

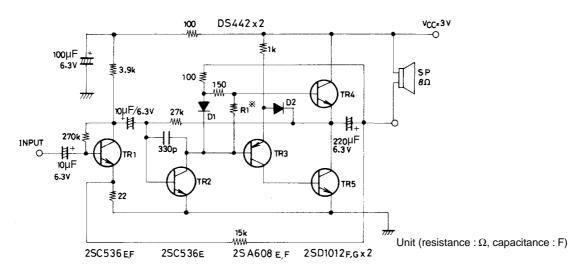




Sample Application Circuit: Low-voltage 3V (Po 120mW) ITL-OTL power amplifier.

· Circuit configuration

For obtaining an output of more than 100mW, the middle-point voltage at the output stage and the collector voltage of the driver transistor must be $V_{CC}/2$. Therefore, the output stage is of quasi complementary configuration composed of npn/npn transistors. The phase is reversed by the 2SA608 and the middle-point voltage are the output stage and the collector voltage of the driver transistor are more to be $V_{CC}/2$ so that the output can be maximized.



R₁: Used control idle current

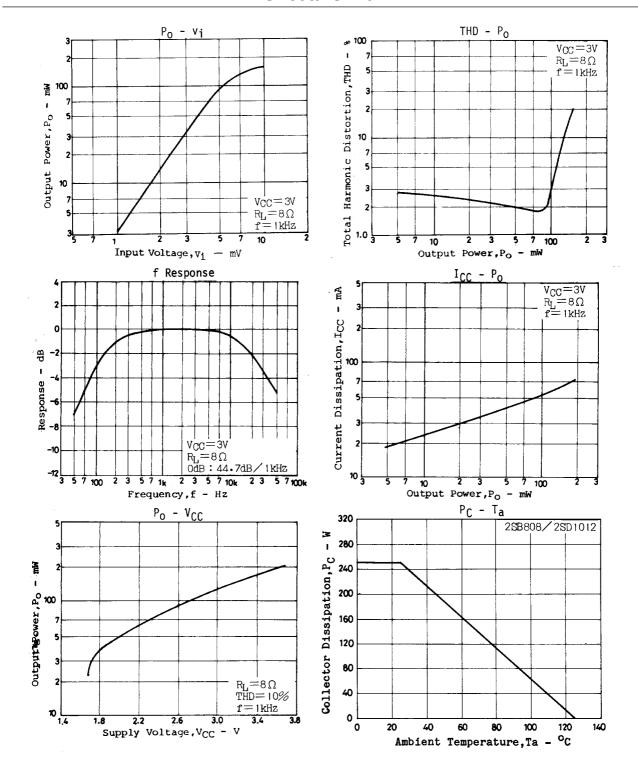
For R_1 =820 Ω , use rank F for [TR4, 5 (2SD1012)].

For R_1 =680 Ω , use rank G for [TR4, 5 (2SD1012)].

Main Specifications

Characteristic	Conditions	f=400Hz	f=1kHz	Unit				
Current dissipation	Quiescent, total current dissipation	11.0 to 15.5	11.0 to 15.5	mA				
Output power	THD=10%	120 to 125	127 to 130	mW				
Votlage gain	P _O =10mW	43.3 to 45.5	43.5 to 45.7	dB				
Total harmonic distortion	P _O =50mW	1.4 to 2.6	1.3 to 2.5	%				
Input resistance	P _O =10mW	10.4 to 20.5	11.0 to 21.0	kΩ				

Note: for above-mentioned h_{FE} rank.



2SB808/2SD1012

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