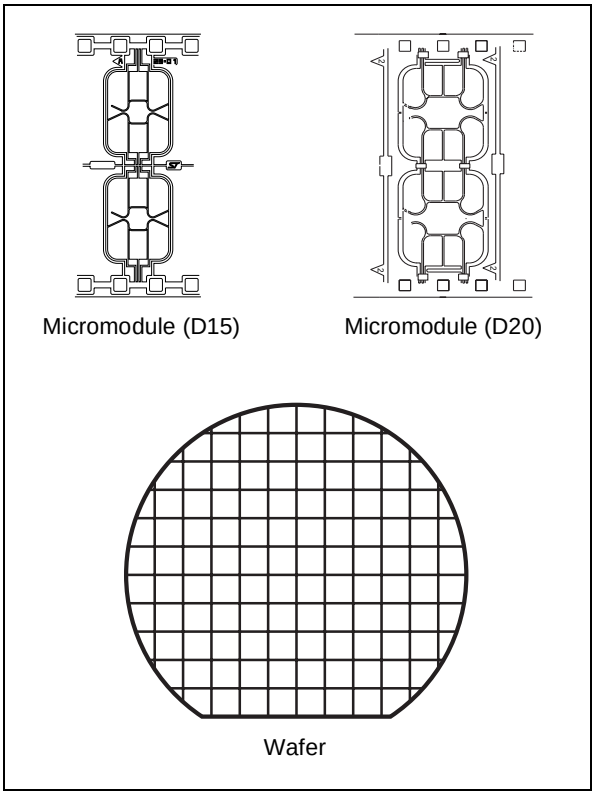
ST14C02C

Memory Card IC
2 Kbit (256 x 8) Serial I^2C Bus EEPROM

DATA BRIEFING

- Single Supply Voltage (3 V to 5.5 V)
- Two Wire I^2C Serial Interface
- BYTE and MULTBYTE WRITE (up to 4 Bytes)
- PAGE WRITE (up to 8 Bytes)
- BYTE, RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behaviour
- 1 Million Erase/Write Cycles (minimum)
- 10 Year Data Retention (minimum)



DESCRIPTION

This device is an electrically erasable programmable memory (EEPROM) fabricated with STMicroelectronics's High Endurance, Advanced Polysilicon, CMOS technology. This guarantees an endurance typically well above one million Erase/Write cycles, with a data retention of 10 years. The memory operates with a power supply as low as 3 V.

The device is available in wafer form (either sawn or unsawn) and in micromodule form (on film).

Each memory is compatible with the I^2C standard. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The memory carries a built-in 7-bit unique Device Type Identifier code (1010000) in accordance with the I^2C bus

Table 1. Signal Names

SDA	Serial Data/Address Input/ Output
SCL	Serial Clock
MODE	Write Mode
V_{CC}	Supply Voltage
GND	Ground

Figure 1. Logic Diagram

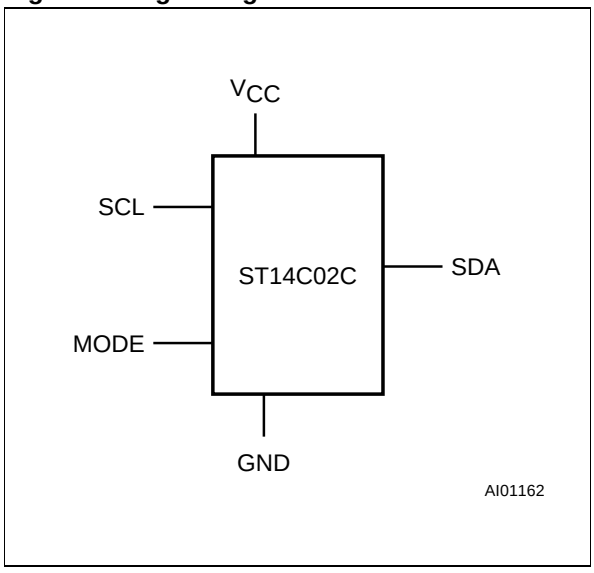


Figure 2. D15 Contact Connections

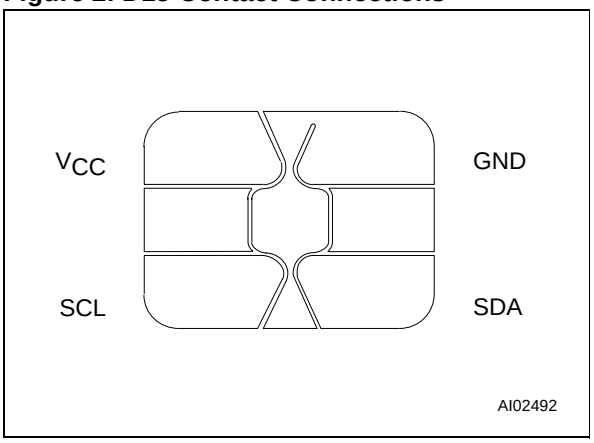
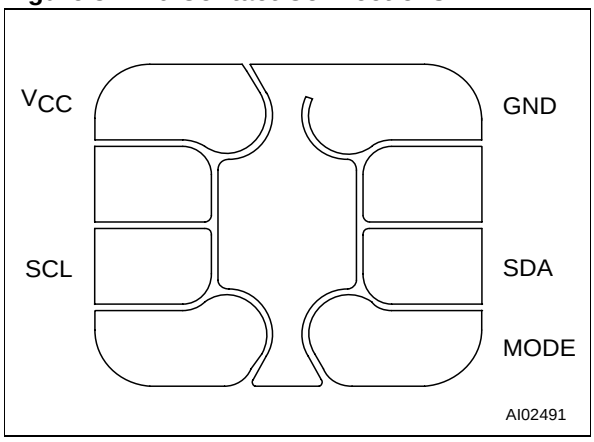


Figure 3. D20 Contact Connections



definition. Only one memory can be attached to each I^2C bus.

The memory behaves as a slave device in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition, generated by the bus master. The START condition is followed by the Device Select Code which is composed of a stream of 7 bits (1010000), plus one read/write bit ($R/\overline{W}$) and is terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a STOP condition after an Ack for WRITE, and after a NoAck for READ.

ORDERING INFORMATION

Devices are shipped from the factory with the memory content set at all '1's (FFh).

The notation used for the device number is as shown in Table 2. For a list of available options (speed, package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Sawn wafers are scribed and mounted in a frame on adhesive tape. The orientation is defined by the position of the GND pad on the die, viewed with active area of product visible, relative to the notches of the frame (as shown in Figure 4). The orientation of the die with respect to the plastic frame notches is specified by the Customer.

One further concern, when specifying devices to be delivered in this form, is that wafers mounted on adhesive tape must be used within a limited period from the mounting date:

– two months, if wafers are stored at 25°C, 55% relative humidity
– six months, if wafers are stored at 4°C, 55% relative humidity

Table 2. Ordering Information Scheme

Example: ST14C02C - D20

Delivery Form	
D15	Module on Super 35 mm film
D20	Module on Super 35 mm film
W2	Unsawn wafer (275 µm ± 25 µm thickness)
W4	Unsawn wafer (180 µm ± 15 µm thickness)
S2x	Sawn wafer (275 µm ± 25 µm thickness)
S4x	Sawn wafer (180 µm ± 15 µm thickness)

where “x” indicates the sawing orientation, as follows (and as shown in Figure 4)

1	GND at top right
2	GND at bottom right
3	GND at bottom left
4	GND at top left

Figure 4. Sawing Orientation