TEMIC

Siliconix

J/SST108 Series

N-Channel JFETs

J108 SST108
J109 SST109
J110 SST110

Product Summary

Part Number	$V_{GS(off)}$ (V)	$r_{DS(on)}$ Max (Ω)	$I_{D(off)}$ Typ (pA)	t_{ON} Typ (ns)
J/SST108	−3 to −10	8	20	4
J/SST109	−2 to −6	12	20	4
J/SST110	−0.5 to −4	18	20	4

Features

- Low On-Resistance: J108 <8 Ω
- Fast Switching—t_{ON}: 4 ns
- Low Leakage: 20 pA
- Low Capacitance: 11 pF
- Low Insertion Loss

Benefits

- Low Error Voltage
- High-Speed Analog Circuit Performance
- Negligible "Off-Error," Excellent Accuracy
- Good Frequency Response
- Eliminates Additional Buffering

Applications

- Analog Switches
- Choppers
- Sample-and-Hold
- Normally "On" Switches
- Current Limiters

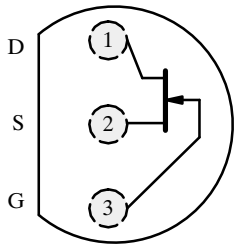
Description

The J/SST108 series is designed with high-performance analog switching applications in mind. It features low on-resistance, good off-isolation, and fast switching.

The SST108 series is comprised of surface-mount devices featuring the lowest $r_{DS(on)}$ of any TO-236 (SOT-23) JFET device.

The TO-226AA (TO-92) plastic package provides a low-cost option. Both the J and SST series are available in tape-and-reel for automated assembly (see Packaging Information). For similar products packaged in TO-206AC (TO-52), see the 2N5432/5433/5434 data sheet.

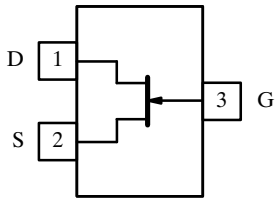
TO-226AA
(TO-92)



Top View

J108, J109, J110

TO-236
(SOT-23)



Top View

SST108 (I8)*
SST109 (I9)*
SST110 (I0)*

*Marking Code for TO-236

Absolute Maximum Ratings

Gate-Drain, Gate-Source Voltage . . . . . −25 V
Gate Current . . . . . 50 mA
Lead Temperature ($^1/_{16}$" from case for 10 sec.) . . . . . 300°C
Storage Temperature . . . . . −55 to 150°C
Operating Junction Temperature . . . . . −55 to 150°C
Power Dissipation[a] . . . . . 350 mW

Notes
a. Derate 2.8 mW/°C above 25°C

J/SST108 Series

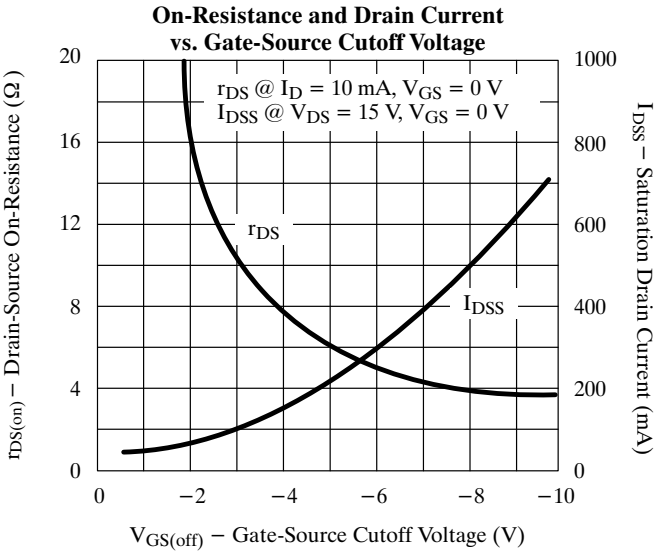
Specifications[a]

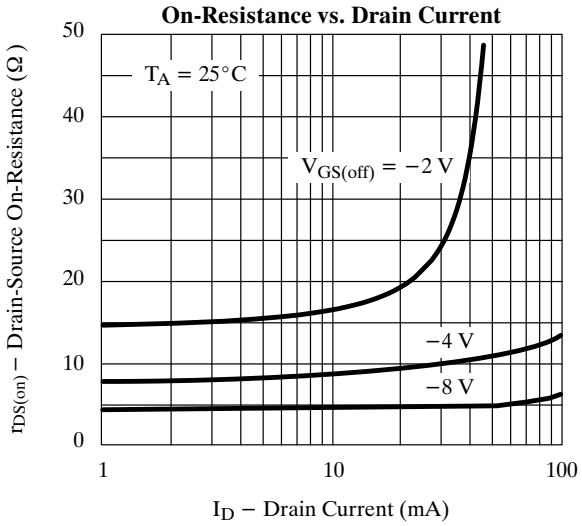
Parameter	Symbol	Test Conditions		Typ[b]	Limits J/SST108 Min	J/SST108 Max	J/SST109 Min	J/SST109 Max	J/SST110 Min	J/SST110 Max	Unit
Static											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1$ µA , $V_{DS} = 0$ V		−32	−25		−25		−25		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 5$ V, $I_D = 1$ µA			−3	−10	−2	−6	−0.5	−4	
Saturation Drain Current[c]	I_{DSS}	$V_{DS} = 15$ V, $V_{GS} = 0$ V			80		40		10		mA
Gate Reverse Current	I_{GSS}	$V_{GS} = -15$ V, $V_{DS} = 0$ V		−0.01		−3		−3		−3	nA
			$T_A = 125°C$	−5							
Gate Operating Current	I_G	$V_{DG} = 10$ V, $I_D = 10$ mA		−0.01							
Drain Cutoff Current	$I_{D(off)}$	$V_{DS} = 5$ V, $V_{GS} = -10$ V		0.02		3		3		3	
			$T_A = 125°C$	1.0							
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{GS} = 0$ V, $V_{DS} \leq 0.1$ V				8		12		18	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	$I_G = 1$ mA , $V_{DS} = 0$ V		0.7							V
Dynamic											
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 5$ V, $I_D = 10$ mA, f = 1 kHz		17							mS
Common-Source Output Conductance	g_{os}			0 . 6							
Drain-Source On-Resistance	$r_{ds(on)}$	$V_{GS} = 0$ V, $I_D = 0$ mA , f = 1 kHz				8		12		18	Ω
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 0$ V, $V_{GS} = 0$ V, f = 1 MHz	SST	60							pF
			J Series	60		85		85		85	
Common-Source Reverse Transfer Capacitance	C_{rss}	$V_{DS} = 0$ V, $V_{GS} = -10$ V, f = 1 MHz	SST	11							
			J Series	11		15		15		15	
Equivalent Input Noise Voltage	$\overline{e}_n$	$V_{DG} = 5$ V, $I_D = 10$ mA, f = 1 kHz		3.5							$\frac{nV}{\sqrt{Hz}}$
Switching											
Turn-On Time	$t_{d(on)}$	$V_{DD} = 1.5$ V, $V_{GS(H)} = 0$ V, See Switching Diagram		3							ns
	t_r			1							
Turn-Off Time	$t_{d(off)}$			4							
	t_f			18							

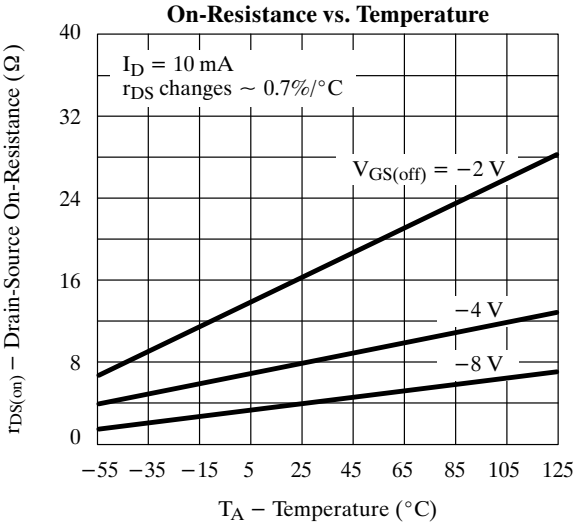
Notes
a. $T_A = 25°C$ unless otherwise noted.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Pulse test: PW ≤ 300 µs duty cycle ≤ 3%.

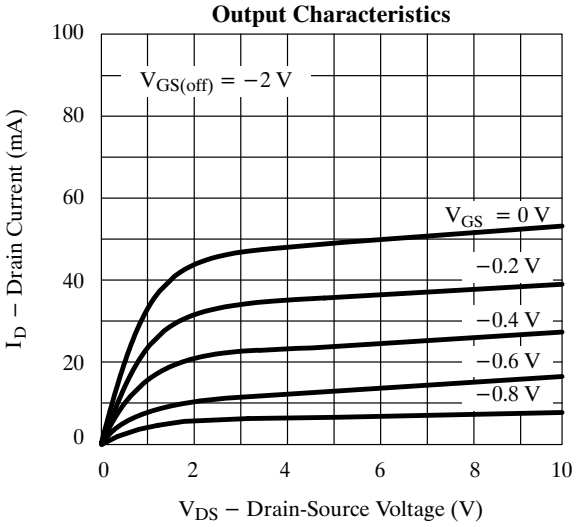
NIP

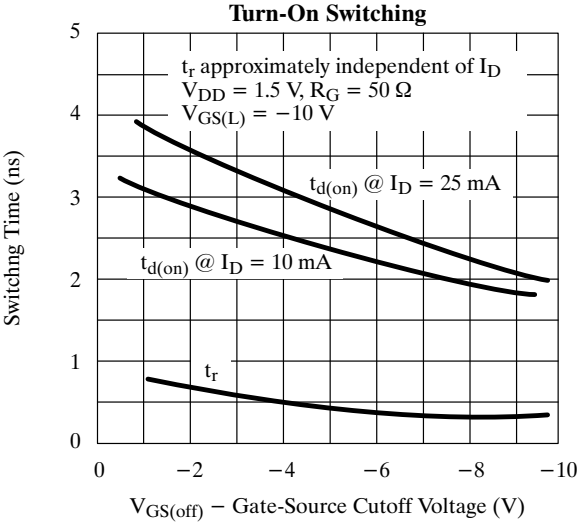
Typical Characteristics

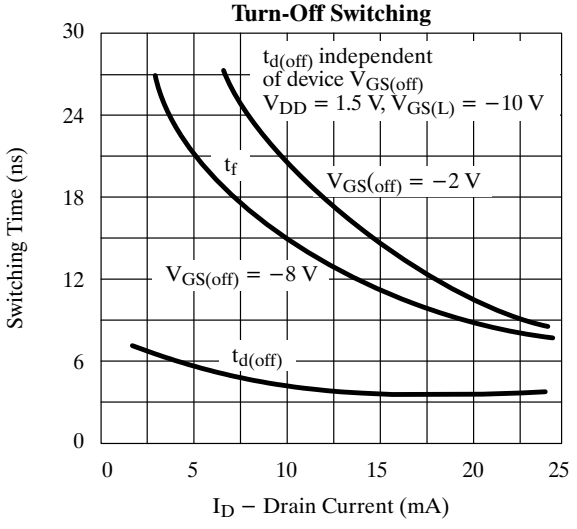








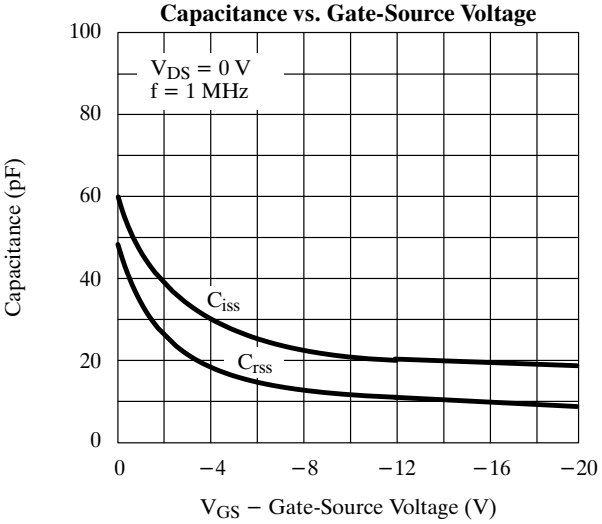




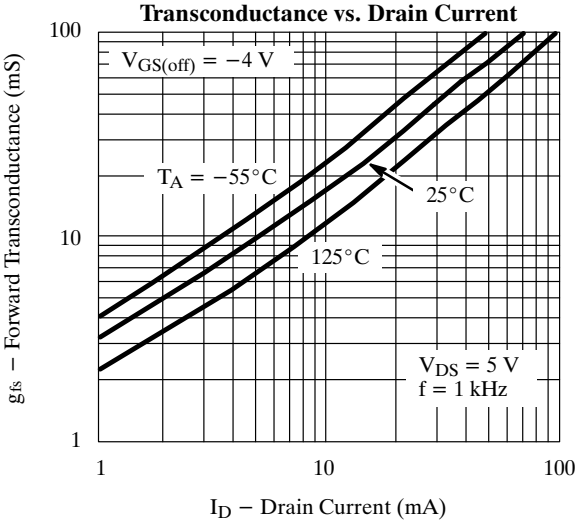
J/SST108 Series

Typical Characteristics (Cont'd)

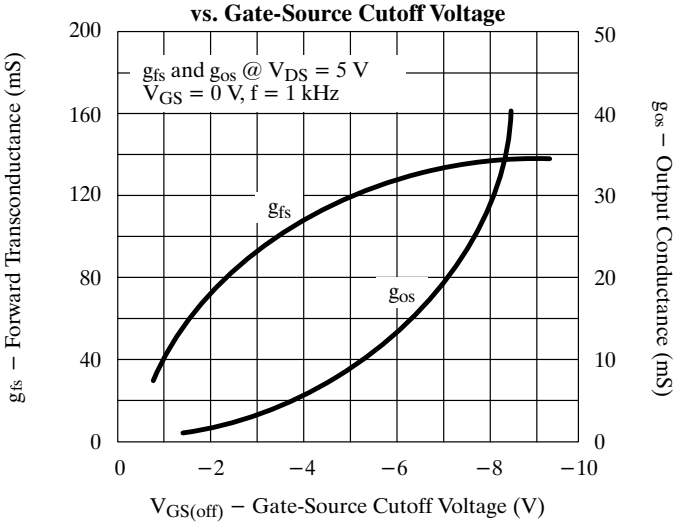
Capacitance vs. Gate-Source Voltage



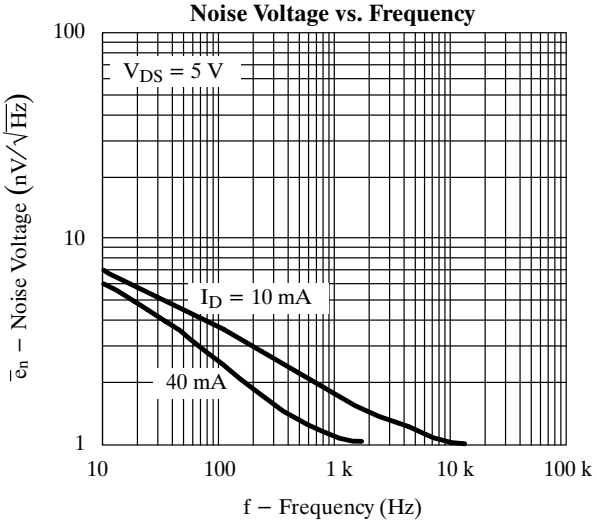
Transconductance vs. Drain Current



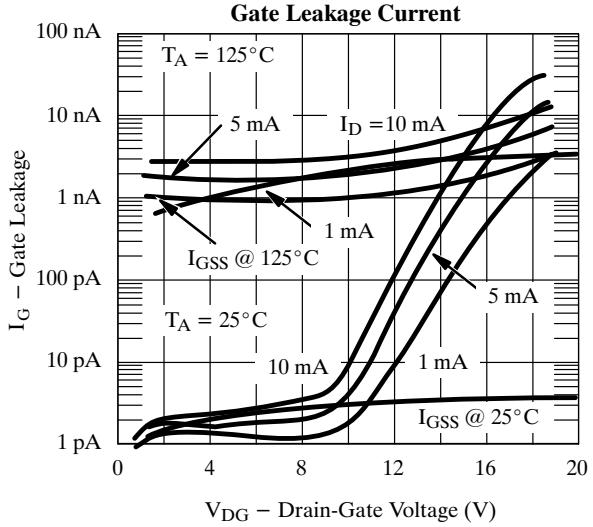
Forward Transconductance and Output Conductance vs. Gate-Source Cutoff Voltage



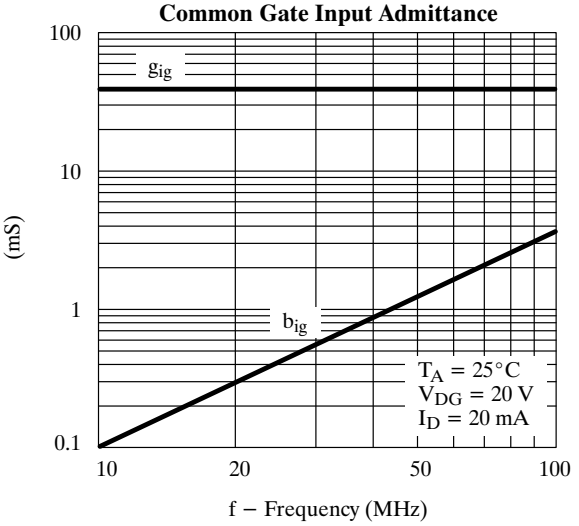
Noise Voltage vs. Frequency



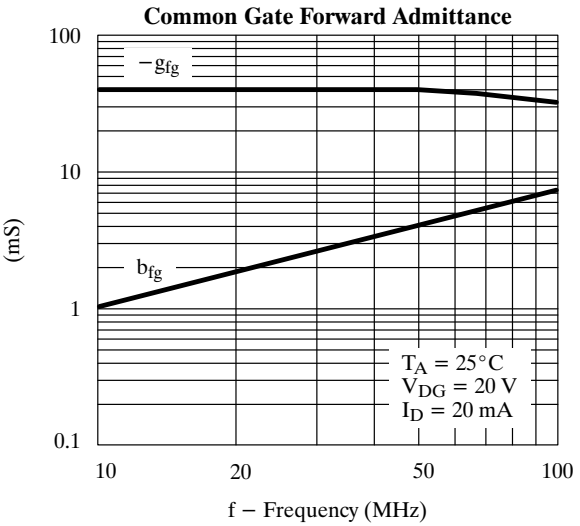
Gate Leakage Current

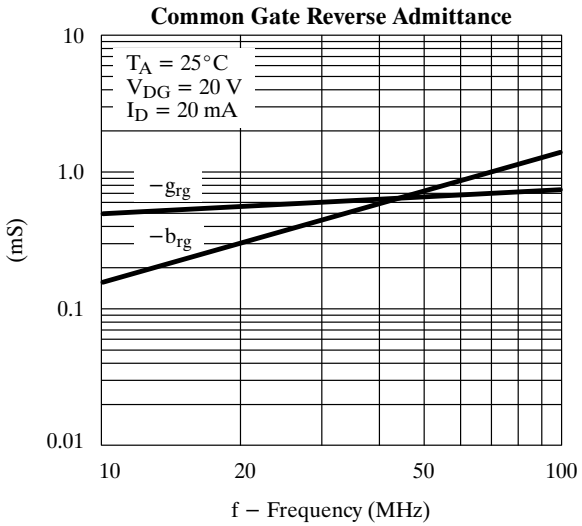


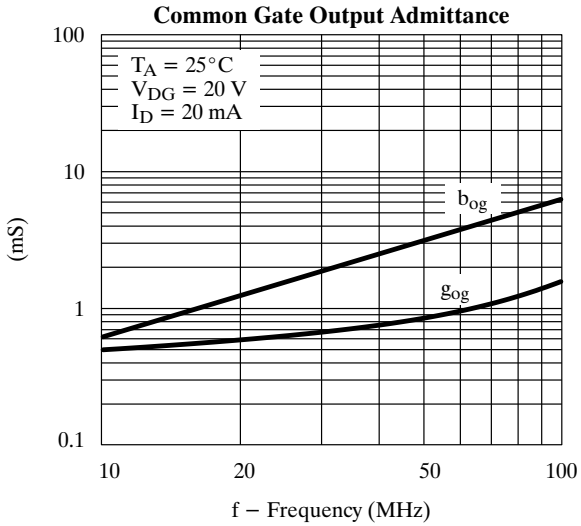
Common Gate Input Admittance



Typical Characteristics (Cont'd)







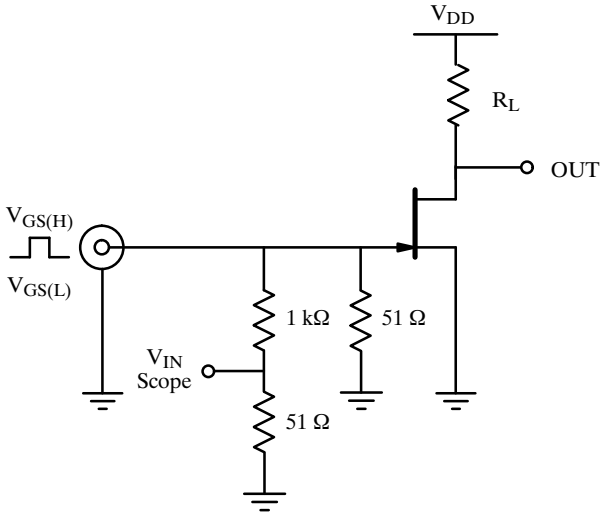
Switching Time Test Circuit

	J/SST108	J/SST109	J/SST110
$V_{GS(L)}$	−12 V	−7 V	−5 V
R_L*	150 Ω	150 Ω	150 Ω
$I_{D(on)}$	10 mA	10 mA	10 mA

*Non-inductive

Input Pulse

Rise Time < 1 ns
Fall Time < 1 ns
Pulse Width 100 ns
PRF 1 MHz

Sampling Scope

Rise Time 0.4 ns
Input Resistance 10 MΩ
Input Capacitance 1.5 pF