Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package
				TO-92
350V	10Ω	1.0A	1.8V	TN0635N3
400V	10Ω	1.0A	1.8V	TN0640N3

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Features

- ☐ Low threshold —1.8V max.
- ☐ High input impedance
- ☐ Low input capacitance — 85pF typical
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Low Threshold DMOS Technology

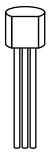
These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Logic level interfaces – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drives
- ☐ Analog switches
- ☐ General purpose line drivers
- ☐ Telecom switches

Package Options



S G D
TO-92

Note: See Package Outline section for dimensions.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	200mA	1.5A	1.0W	125	170	200mA	1.5A

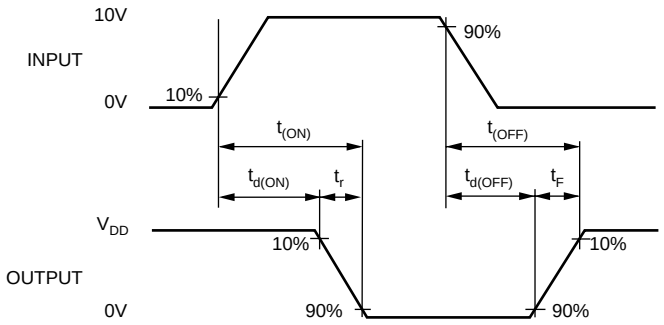
* I_D (continuous) is limited by max rated T_j.

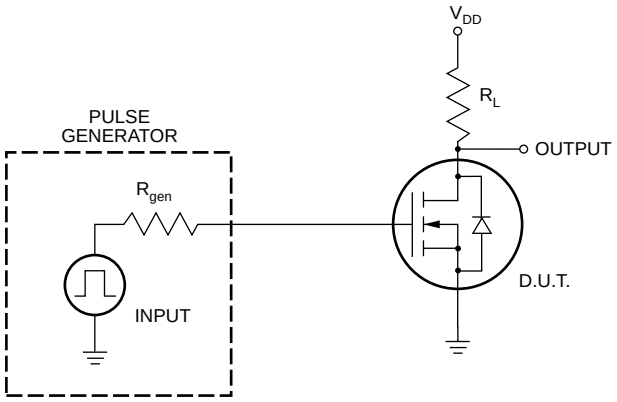
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0640	400			V	V_{GS} = 0V, I_D = 100µA
		TN0635	350				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.8	V	V_{GS} = V_{DS}, I_D= 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-2.5	-4.0	mV/°C	V_{GS} = V_{DS}, I_D= 1mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	V_{GS} = 0V, V_{DS} = Max Rating
					1.0	mA	V_{GS} = 0V, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		0.3	1.5		A	V_{GS} = 5V, V_{DS} = 25V
			1.0	1.8			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			8.0	10	Ω	V_{GS} = 4.5V, I_D = 150mA
				7.0	10		V_{GS} = 10V, I_D = 500mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	V_{GS} = 10V, I_D = 500mA
G_{FS}	Forward Transconductance		125	350		m℧	V_{DS} = 25V, I_D = 100mA
C_{ISS}	Input Capacitance			85	130	pF	V_{GS} = 0V, V_{DS} = 25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance			30	75		
C_{RSS}	Reverse Transfer Capacitance			10	20		
$t_{d(ON)}$	Turn-ON Delay Time				20	ns	V_{DD} = 25V, I_D = 1.0A, R_{GEN} = 25Ω
t_r	Rise Time				15		
$t_{d(OFF)}$	Turn-OFF Delay Time				25		
t_f	Fall Time				20		
V_{SD}	Diode Forward Voltage Drop				1.8	V	V_{GS} = 0V, I_{SD} = 200mA
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0V, I_{SD} = 1.0A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

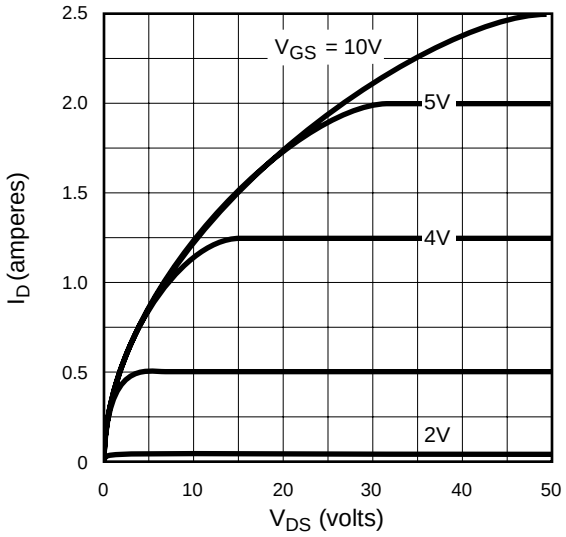
Switching Waveforms and Test Circuit



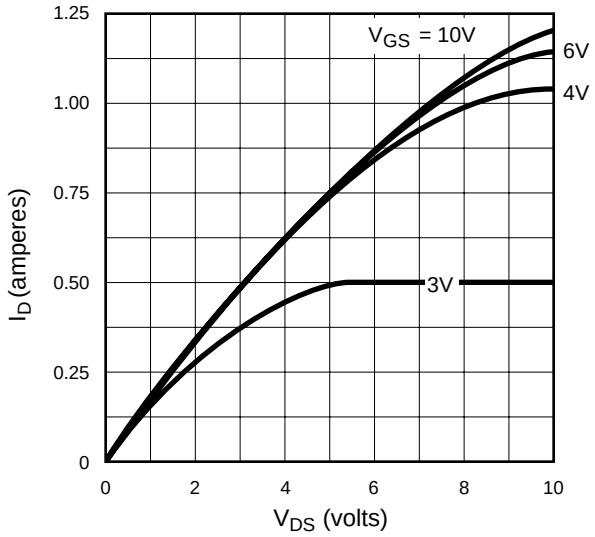


Typical Performance Curves

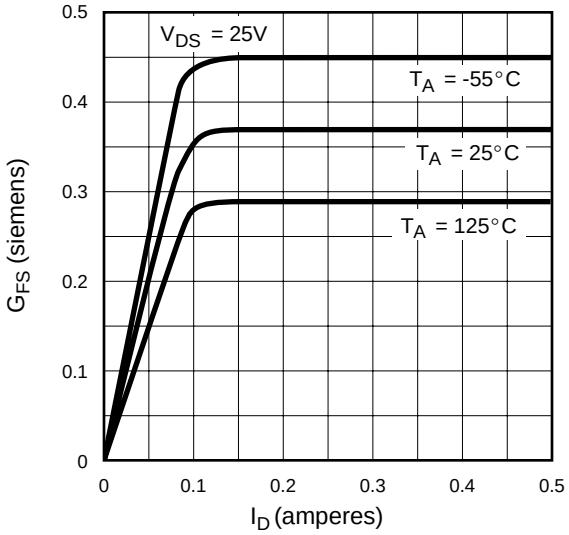
Output Characteristics



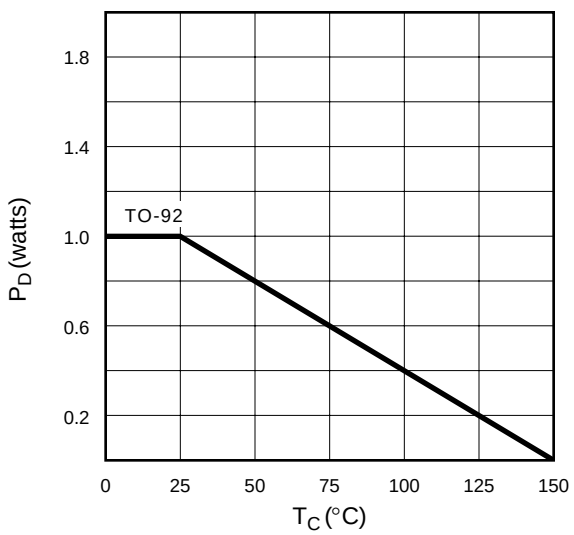
Saturation Characteristics



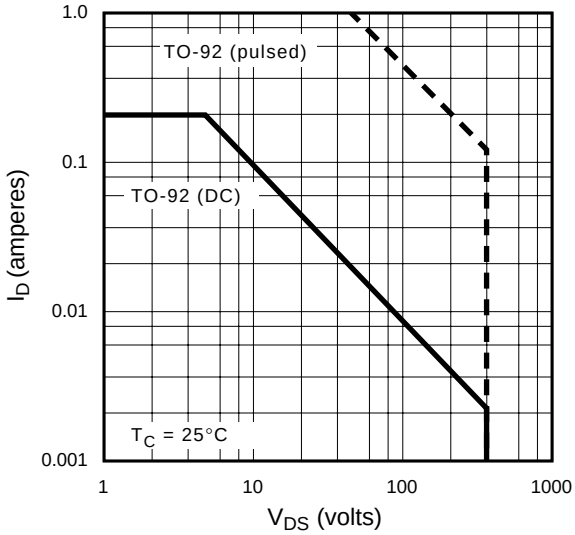
Transconductance vs. Drain Current



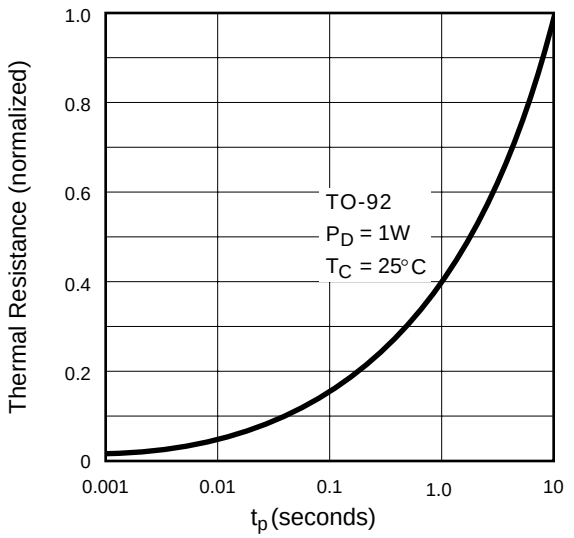
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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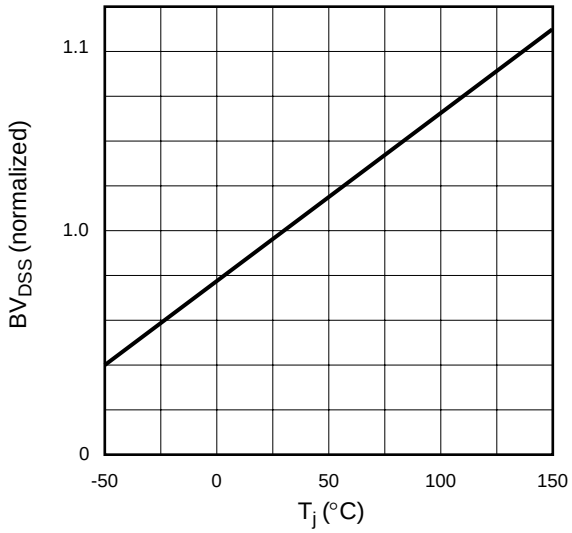
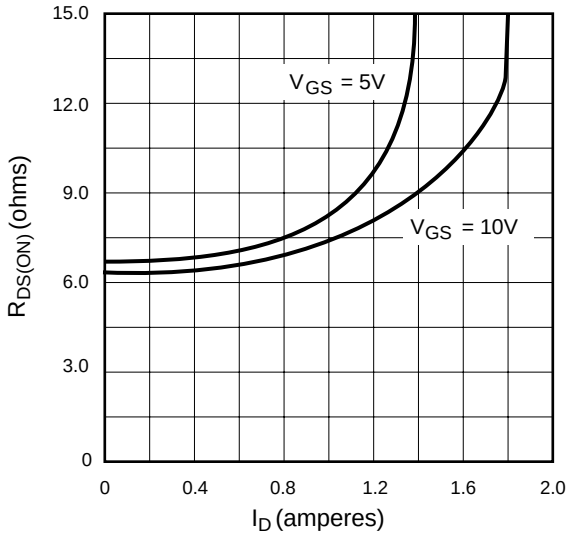
Typical Performance Curves

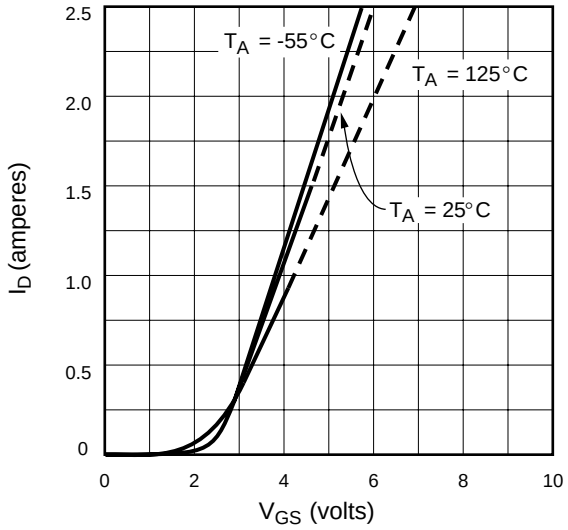
BV$_{DSS}$ Variation with Temperature



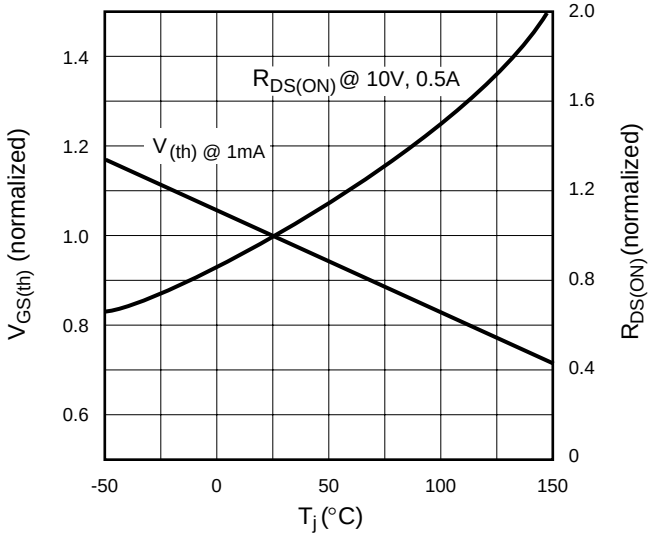
On-Resistance vs. Drain Current



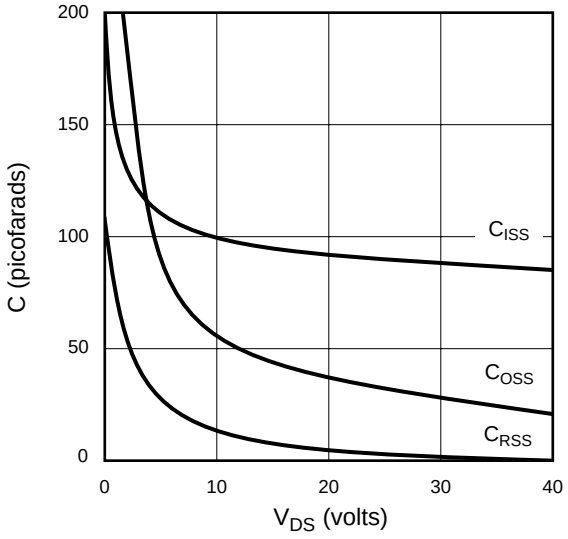
Transfer Characteristics



V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics