

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

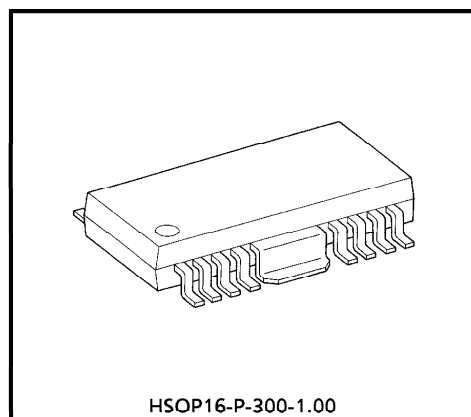
TA8430AF

STEPPING MOTOR DRIVER IC

The TA8430AF is 2 Phase Bipolar Stepping Motor Driver IC designed especially for low operating voltage use FDD and other portable equipments.

FEATURES

- 2 Phase Bipolar Stepping Motor Driver
- Low Voltage Use : $V_{CC\text{ opr}} = 4V$ (Min.)
- Power Save and Stand-by Mode available
 $I_{CC\text{ stand-by}} \leq 100\mu A$
- Built-in Punch Through Current Restriction Circuit
- 1, 2 and 1-2 Phase Excitation Drive available
- C-MOS Compatible Inputs (INA, INB, PS, ST)
- Output Current up to 400mA (AVE) and 600mA (PEAK)
- Sealed in PFP 16 SM Package
- HEAT SINK is connected with GND with low impedance.

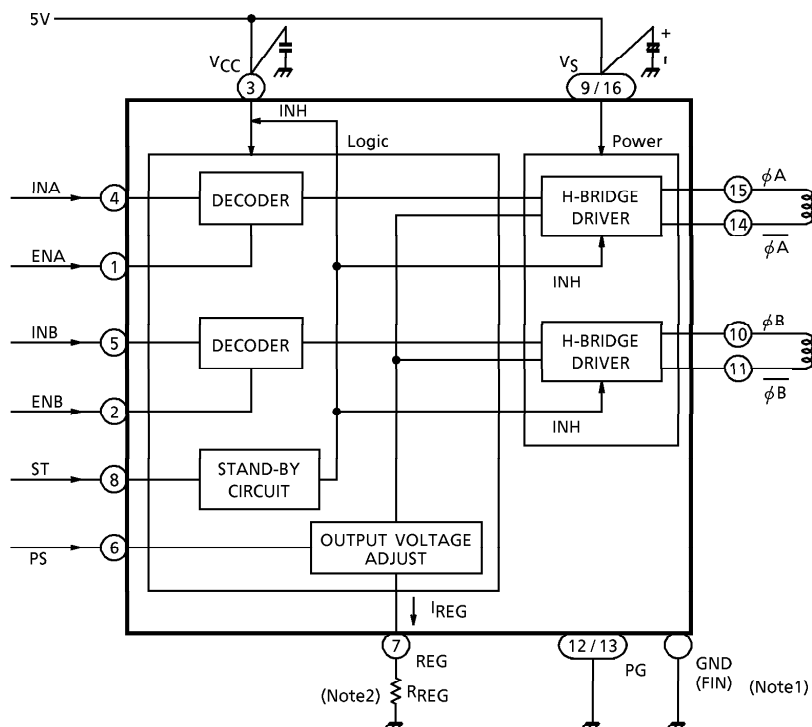


Weight : 0.50g (Typ.)

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BLOCK DIAGRAM



(Note 1) GND terminal of 12 / 13 connect to FIN.

(Note 2) Output Voltages, appeared at ϕA , $\overline{\phi A}$, ϕB and $\overline{\phi B}$, are adjusted by R_{reg} when Power Save function is selected.

(Note 3) Utmost care is necessary in the design of the output line, V_{CC} , V_S and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

PIN FUNCTION

PIN No.	SYMBOL	FUNCTION
1	ENA	A channel enable
2	ENB	B channel enable
3	V_{CC}	Supply voltage
4	INA	A channel reciprocal switching
5	INB	B channel reciprocal switching
6	PS	Energy-saving signal input
7	REG	Output voltage setting
8	ST	Stand-by signal input
9	V_S	Supply voltage
10	ϕB	B output
11	$\overline{\phi B}$	B output
12	PG	Power supply GND connection
13	PG	Power supply GND connection
14	$\overline{\phi A}$	A output
15	ϕA	A output
16	V_S	Supply voltage
FIN	GND	GND connection

FUNCTION

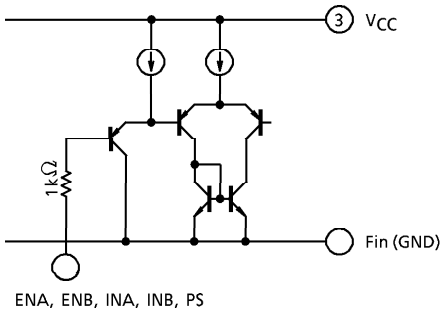
INPUT				OUTPUT		
ST	EN	PS	IN	ϕ	$\overline{\phi}$	UPPER SIDE SATURATION VOLTAGE
H	H	L	L	L	H	$V_S - V_{CE(SAT)} U$
H	H	L	H	H	L	$V_S - V_{CE(SAT)} U$
H	H	H	L	L	H	V_{REG} (Note)
H	H	H	H	H	L	V_{REG} (Note)

(Note) V_{REG} is a voltage appeared at PIN⑦ and its value becomes approximately equal to V_{OUT} in power operation period.

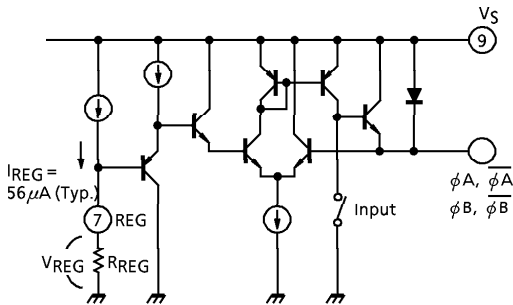
ST	ENA	ENB	$\phi A, \overline{\phi A}$	$\phi B, \overline{\phi B}$	MODE
H	L	H	∞	ENABLE	OPERATION
H	H	L	ENABLE	∞	OPERATION
H	H	H	ENABLE	ENABLE	OPERATION
L	X	X	∞	∞	STAND-BY

X : Don't Care
 ∞ : High Impedance

INPUT STEP CIRCUIT DIAGRAM



V_{REG} OUTPUT CIRCUIT DIAGRAM

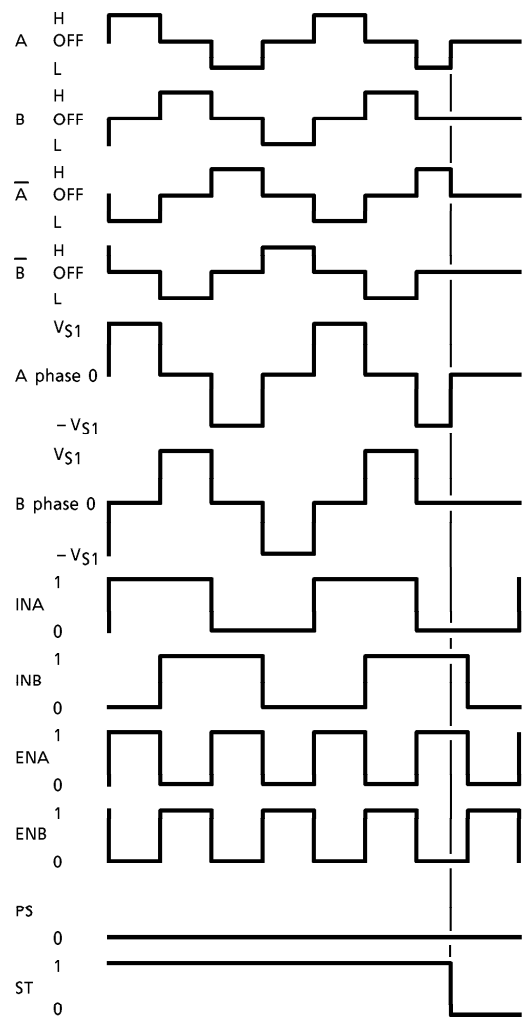


V_{REG} output voltage can be selected with R_{REG} exterior resistance.
If V_{REG} is not used (as in the case of double-phase magnetization), use pin⑦ in the open position.
(Do not connect to V_{CC} or GND pins.)
Use the following formula to obtain the output voltage.

$$V_{OUT} \cong V_{REG} \cong R_{REG} \times 56 \times 10^{-6}$$

[illegible]

Single-phase magnetization



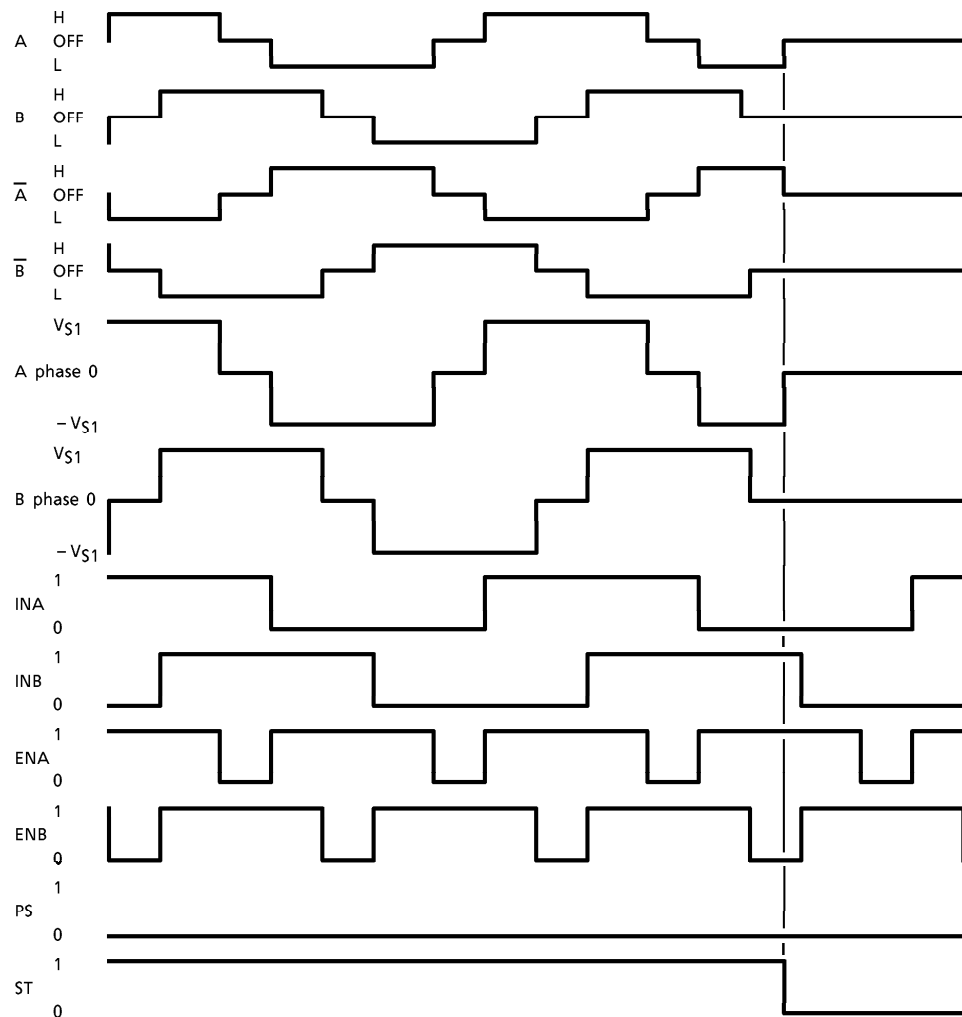
$$* \quad V_{S1} = V_S - (V_{SATU} + V_{SATL})$$

The timing diagram illustrates the logic levels for the 74VHC04B over time. The signals shown are:

- A**: Input A, with levels H (High), OFF (High-Z), and L (Low).
- B**: Input B, with levels H (High), OFF (High-Z), and L (Low).
- \overline{A}** : Inverted input A, with levels H (High), OFF (High-Z), and L (Low).
- \overline{B}** : Inverted input B, with levels H (High), OFF (High-Z), and L (Low).
- V_{S1}** : Supply voltage, switching between H and L.
- A phase 0**: Phase 0 of input A, switching between H and L.
- $-V_{S1}$** : Negative supply voltage, switching between H and L.
- B phase 0**: Phase 0 of input B, switching between H and L.
- $-V_{S1}$** : Negative supply voltage, switching between H and L.
- INA**: Inverted input A, with levels 1 (High) and 0 (Low).
- INB**: Inverted input B, with levels 1 (High) and 0 (Low).
- ENA**: Enable input A, with levels 1 (High) and 0 (Low).
- ENB**: Enable input B, with levels 1 (High) and 0 (Low).
- PS**: Power supply, with levels 0 (Low) and 1 (High).
- ST**: Status input, with levels 0 (Low) and 1 (High).

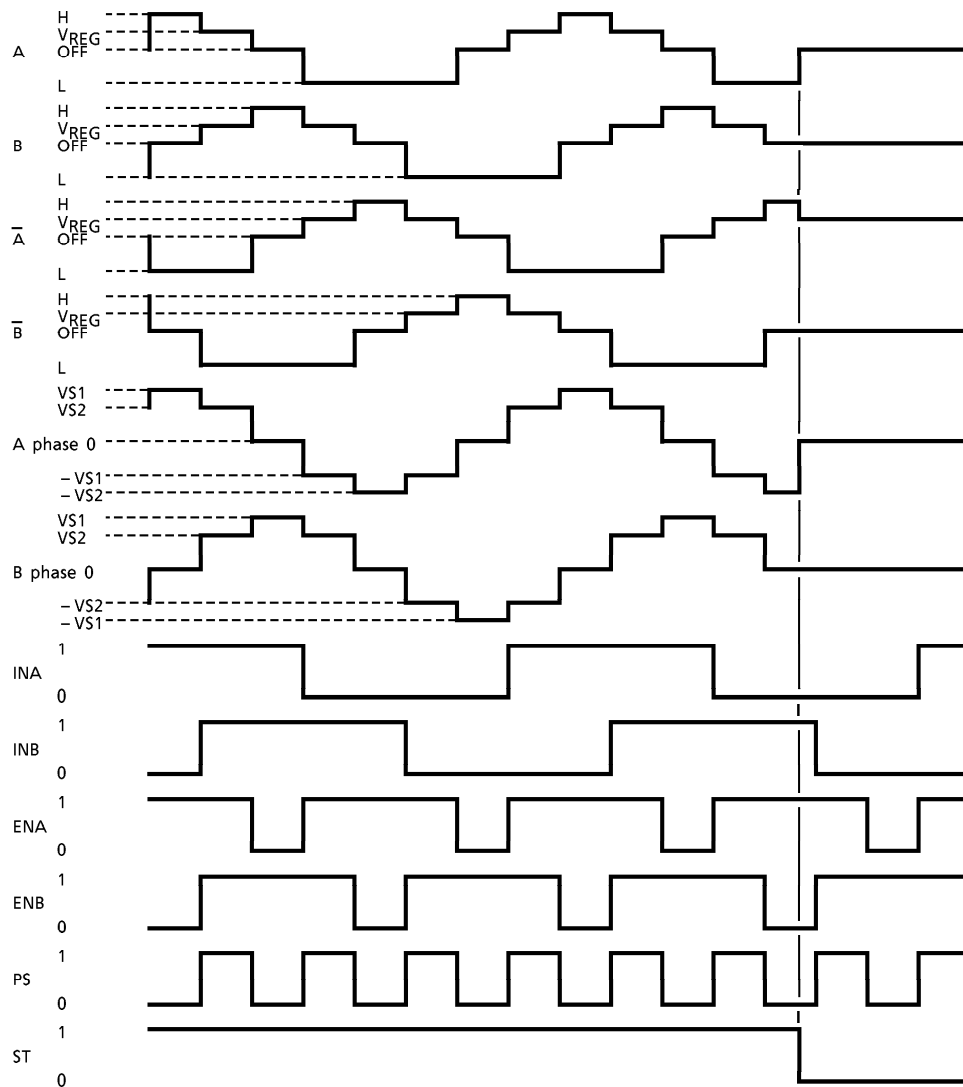
$$* \quad V_{S1} = V_S - (V_{SATU} + V_{SATL})$$

Single- / double-phase magnetization



$$* V_{S1} = V_S - (V_{SAT\ U} + V_{SAT\ L})$$

Single- /double-phase magnetization (with energy-saving function)



$$V_{S1} = V_S - (V_{SAT U} + V_{SAT L})$$

$$V_{S2} = V_{REG} - V_{SAT L}$$

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC}	8.0	V
	V _S	8.0	
Output Current	I _O (MAX.)	± 600	mA
	I _O (AVE.)	± 400	
Input Voltage	V _{IN} , V _{PS} V _{ST} , V _{EN}	GND – 0.4~V _{CC} + 0.4	V
Power Dissipation	P _D (Note)	1.4	W
Operating Temperature	T _{opr}	– 40~85	°C
Storage Temperature	T _{stg}	– 55~150	°C

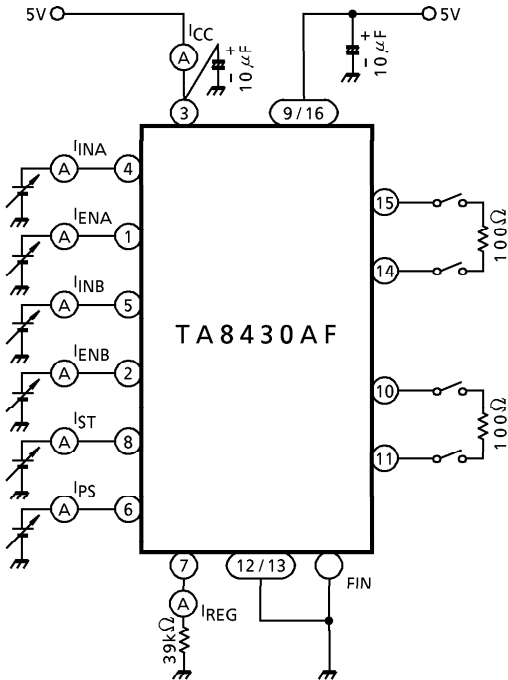
(Note) 60×30×1.6mm PCB occupied in excess of 50% of copper area, mounting.

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 5V, V_S = 5V, ST = 5V, PS = 0V, EN = 5V)

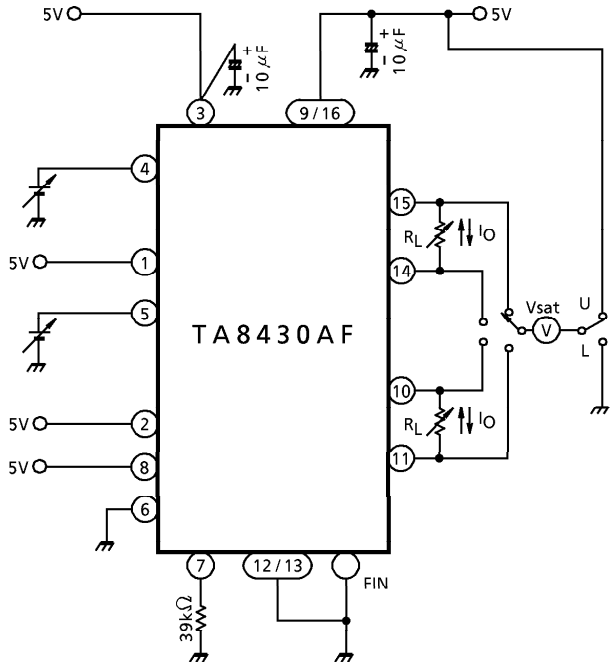
CHARACTERISTIC	SYMBOL	TEST CIR- CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Supply Current	I _{CC1}	1	Output open		—	14	20	mA
	I _{CC2}		Output open, PS = 5V		—	14	20	
	I _{CC3}		Output open	ENA = 0V, ENB = 5V	—	9	15	
				ENA = 5V, ENB = 0V				
	I _{CC4}		Output open, PS = 5V	ENA = 0V, ENB = 5V	—	9	15	
				ENA = 5V, ENB = 0V				
I _{CC5}	ST = 0V		20	65	110	μA		
Input Voltage	V _{INH}	1	④, ⑤ pin Source type		3.5	—	V _{CC}	V
	V _{INL}				GND	—	1.7	
	V _{ENH} , V _{PSH}		①, ②, ⑥, ⑧ pin Source type		3.5	—	V _{CC}	
	V _{STH}				GND	—	1.7	
	V _{ENL} , V _{PSL}				GND	—	1.7	
	V _{STL}				GND	—	1.7	
Input Current	I _{INH}	1	V _{IN} = 3.5V	④, ⑤ pin	—	0	0.1	μA
	I _{INL}		V _{IN} = 0V		—	0.25	5.0	
	I _{ENH} , I _{PSH}		V _{EN} = V _{PS} = 3.5V	①, ②, ⑥ pin	—	0	0.1	
	I _{ENL} , I _{PSL}		V _{EN} = V _{PS} = 0V		—	0.25	5.0	
	I _{STH}		V _{ST} = 3.5V	⑧ pin	—	0	0.1	
	I _{STL}		V _{ST} = 0V		—	65	110	

CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Saturation Voltage		V _{SAT U1}	2	—	I _{OUT} = 100mA	—	0.8	—	V
		V _{SAT U2}			I _{OUT} = 400mA	—	0.9	1.2	
		V _{SAT L1}			I _{OUT} = 100mA	—	0.1	—	
		V _{SAT L2}			I _{OUT} = 400mA	—	0.2	0.4	
Output Control Upper Voltage		V _{REG1}	—	R _{REG} = 39kΩ	I _{OUT} = 100mA	—	2.0	—	V
		V _{REG2}			I _{OUT} = 400mA	—	1.9	—	
Control Circuit Output Current		I _{REG}	1	—		41	56	71	μA
Diode Forward Voltage		V _{FU}	3	I _F = 400mA	—	1.5	2.0	V	
		V _{FL}			—	1.0	2.0		
Operating Supply Voltage Range		V _{CC (opr.)}	—	—		4.0	—	6.0	V
Propagation Delay Time	IN-φ	t _{pLH}	—	R _L = 8.2Ω C _L = 15pF	—	4.5	—	μs	
	EN-φ				—	3	—		
	PS-φ				—	4.5	—		
	ST-φ				—	10	—		
	IN-φ	t _{pHL}			—	0.1	—		
	EN-φ				—	10	—		
	PS-φ				—	0.2	—		
	ST-φ				—	5	—		

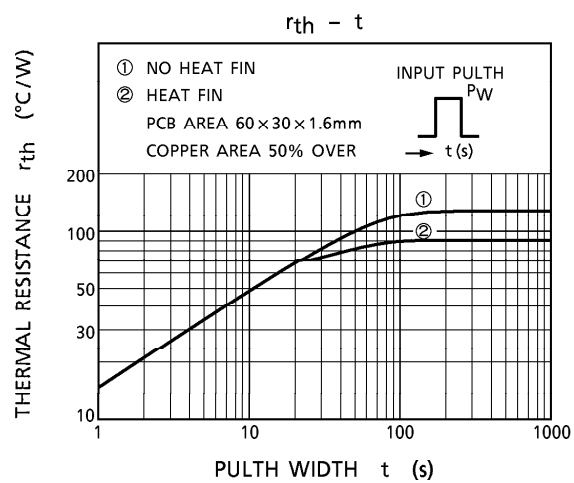
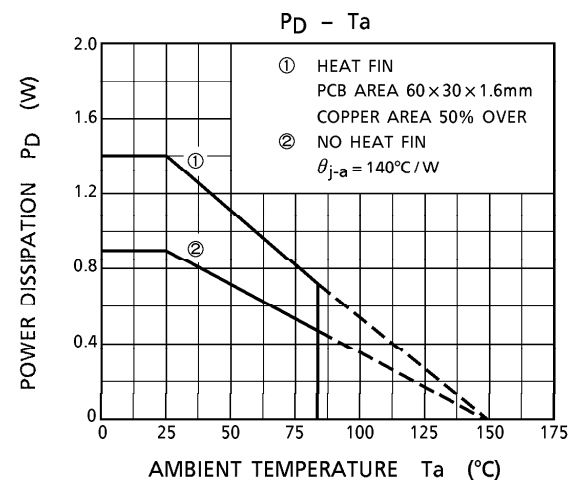
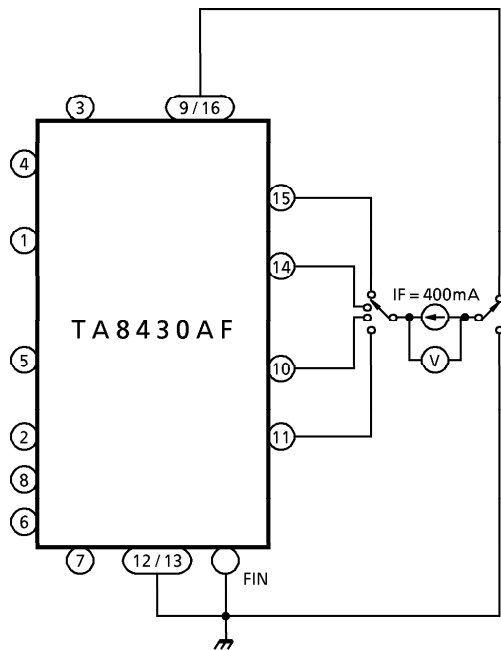
TEST CIRCUIT 1



TEST CIRCUIT 2

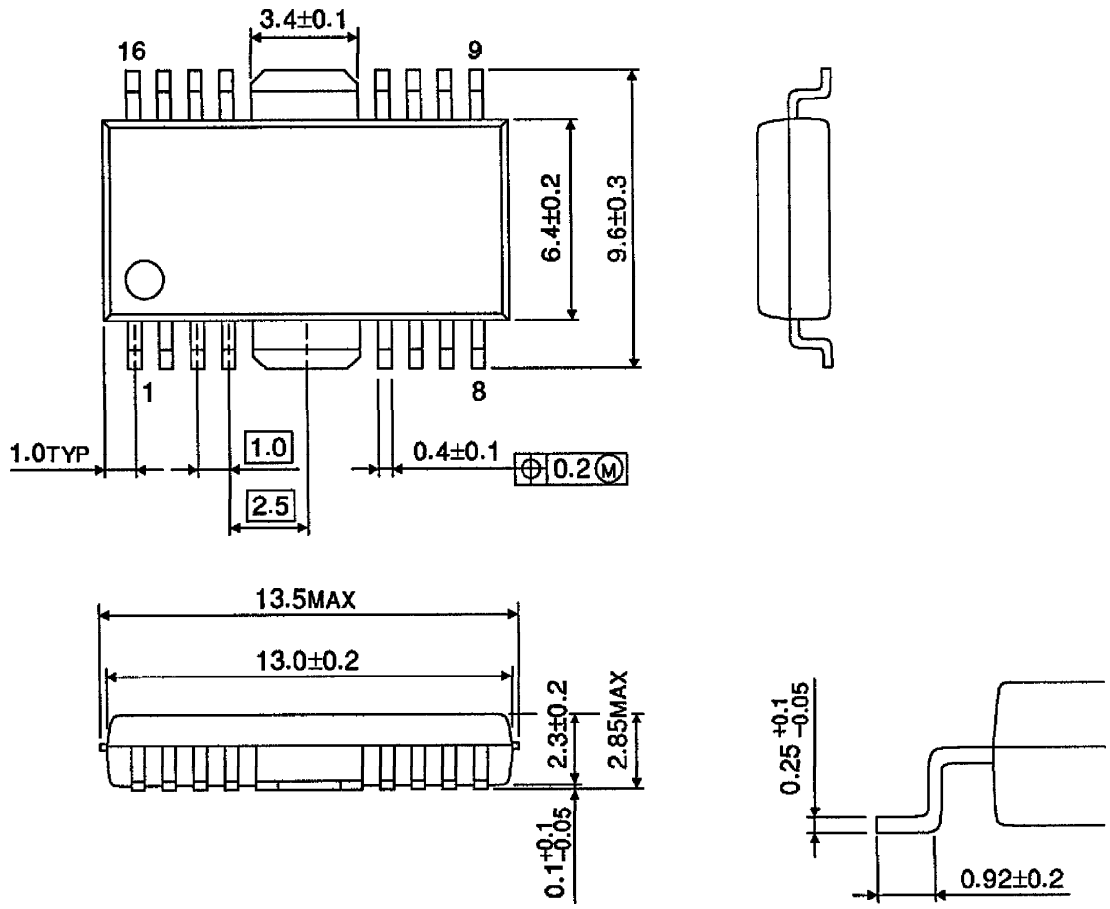


TEST CIRCUIT 3



OUTLINE DRAWING
HSOP16-P-300-1.00

Unit : mm



Weight : 0.50g (Typ.)