1795 DS5 Tuner

Digital Satellite

DVB / DSS Tuner
Single Input

TARGET SPECIFICATION ELECTRICAL DATA

APPLICATIONS

- Set-Top Box applications for DVB-S and DSS
- PC cards for high speed Internet and data transfer
- Professional satellite data modems

FEATURES

- Baseband I & Q outputs
- Extended tuning range: 920 to 2150 MHz
- SAW resonator stabilized LO for I/Q demodulation
- Suitable for MCPC and SCPC applications
- Excellent phase noise performance allows from 1 to 45 Mbaud operation
- Wide selection of fixed and switchable IF bandwidths
- Internal AGC monitor output
- I2C-bus control of tuning functions and bandwidth selection
- Horizontal and vertical mounting available
- DiSEqC compatible

ORDERING INFORMATION

	8 MHz	36MHz	32 MHz	27MHz	55 MHz	7/14 MHz	27/36 MHz	27/55 MHz
vertical	tbd	3x7411	tbd	tbd	tbd	tbd	tbd	tbd
horizontal	tbd	3x7245	tbd	tbd	tbd	tbd	3x7735	3x7737

Contents

1. Working Data

1.1. Power supply

	Min.	Typ.	Max.	[...]	
5 V Supply Voltage	4.75	5	5.25	V	Pin 10
5 V Supply Current		250	320	mA	Pin 10
Tuning Voltage	28		33	V	Pin 13
Tuning Current		1.25	2	mA	Pin 13
LNB Voltage (to LNB, RF input)			25	V	Pin 1
LNB Supply Current			500	mA	Pin 1

1.2. Ambient Conditions

Operating Temperature (in slowly moved air)	0		+ 60	° C	
Storage Temperature	- 20		+ 70	° C	
Operating Humidity			80	%	@ 40° C
Storage Humidity			95	%	@ 40° C

1.3. Antenna terminal

RF Input: F-Connector		75		Ω

1.4. Input Frequency Range

	920	-	2150	MHz

Oscillator operates above received frequency.

1.5. IF frequency:

479.5		MHz	Center

1.6. IF bandwidth:

Tuner Id-No.	3 dB	1 dB	BW	
Tbd	8	6	MHz	
3x7245, 3x7411	36	31.5	MHz	
Tbd	27	21.6	MHz	
Tbd	32	27.5	MHz	
Tbd	55	51.7	MHz	
Tbd	7 / 14	tbd	MHz	switchable
Tbd	27/36	22.6 / 32.7	MHz	switchable

1.7. I/Q Conversion:

Direct conversion of QPSK signals into I and Q components.

Nyquist filtering externally.

1.8. Tuning circuit:

GEC Plessey SP5659

2. Test conditions

If not otherwise noted, all working data measured under the following conditions:

frequency range :	920 MHz - 2150 MHz
test frequency:	1640 MHz
ambient temperature:	+ 25 °C ± 3 °C
supply voltages:	+ 5 V ± 0.1 V
	+ 28 V + 0.1 V

All values are referred to the antenna input terminal.

3. Tuner data

3.1. RF Input:

	Min.	Typ.	Max.	[...]	
Input Impedance		75		Ω	
Input Frequency Range	920	-	2150	MHz	
Input Level	- 65		- 25	dBm	
VSWR		2	2.5		
Noise Figure (measured at I/Q out)		10		dB	gain red.: 0 dB
IF Rejection	40	80		dB	gain red.: 0 dB
Image Rejection	35	45		dB	gain red.: 0 dB
Intermodulation Rejection RF2 = RF1 + 30 MHz RF3 = RF1 + 60 MHz measured at I/Q outputs	40	60		dBc	3 tones - 25 dBm each
Group Delay (over +/- 10 MHz band centered at 480 MHz. RF input to I/Q input) for 32 MHz SAW					
Local pk-pk (Aperture = 100 KHz)		<+/- 20		ns	
Parabolic end-end (Aperture = 3.1 MHz)		< 10		ns	

3.2. Oscillator characteristics

3.2.1 1st VCO

Tuning Frequency Range	1399.5		2629.5	MHz	
Spurious signal and oscillator leakage		-70	-63	dBm	920-2150MHz
		-70	-50	dBm	2150-2630MHz
Settling Time (920 to 2150 MHz)		30		ms	CP = 130 uA
PLL reference divider ratio = 8		10		ms	CP = 600 uA

3.2.2 2nd VCO

Center Frequency	479	479.5	480	MHz	0° to 60°C

3.3. Tuning function

PLL (I²C Bus)

Reference Oscillator	4.00	MHz
Minimum Frequency Step	depending on PLL setting	kHz

(see 5.: Instruction codes for PLL device SP 5659)

3.4 I / Q output

	Min.	Typ.	Max.	[...]	1 kΩ‖15pF load
Output Level		700		mVp-p	
Output DC Level		0		V	AC coupled
I / Q Phase Accuracy		± 1.5	± 3	degs	Type 3x7245
I / Q Amplitude Match		± 0.5	± 1	dB	0 - 30 MHz
Baseband Flatness		± 1	± 2	dB	

Note:

A/D conversion and Nyquist filtering are to be realized externally.

The output baseband amplifiers drive low reactance loads with maximum capacities of 20 pF. To drive higher capacitive loads, the use of emitter-follower buffers on the I/Q outputs is recommended to prevent excessive loading.

3.5 Phase Noise

Total Phase Noise:	Min.	Typ.	Max.	[...]	@ 500 kHz step size
100 Hz Offset		-60	-55	dBc/Hz	
1 kHz Offset		-62	-57	dBc/Hz	
10 kHz Offset		-80	-75	dBc/Hz	
100 kHz Offset		-105	-95	dBc/Hz	
1 MHz Offset		-125	-115	dBc/Hz	

3.6 Control Functions

3.6.1 Internal AGC Monitor Output

	Min.	Typ.	Max.	[...]
Output Impedance @ Pin 9			100	Ω
Maximum Load @ Pin 9			1000	Ω
Voltage at Maximum Gain		3.5		V
Voltage at Minimum Gain		0.5		V

3.6.2 External AGC (I/Q Level)

AGC Control Range		18		dB
U_{AGC} for Maximum Gain @ Pin 8		1.0		V
U_{AGC} for Minimum Gain @ Pin 8		4.0		V
I_{AGC} @ Pin 8			100	µA

4. I²C Bus

Instruction codes for PLL SP5659

4.1 I²C Bus Interface

I²C Bus Port	Tuner Pin No.	
SDA	12	via internal 33pF shunt capacitor
SCL	11	and 100 Ω series resistor
I²C Bus Address		fixed internally to $C0

4.2 Data Format

Table1 - Write Data Format

		MSB							LSB	
Address	Byte 1	1	1	0	0	0	MA1	MA0	0	A
Progr. Divider	Byte 2	0	N14	N13	N12	N11	N10	N9	N8	A
Progr. Divider	Byte 3	N7	N6	N5	N4	N3	N2	N1	N0	A
Control Data	Byte 4	1	N16	N15	PE	R3	R2	R1	R0	A
Control Data	Byte 5	C1	C0	RE	RTS	P3	P2/TS2	P1/TS1	P0/TS0	A

A : Acknowledge Bit
MA1, MA0 : Address Bits, both fixed to zero
Write Address = $C0
N16,...,N0 : Programmable Divider Bits

$$N = N16 \times 2^{16} + N15 \times 2^{15} + ... + N1 \times 2^{1} + N0$$

PE: Prescaler Enable (PE=1 for LO-frequencies above 2 GHz and while tuning)
R3, R2, R1, R0: Reference Division Ratio select (see Table 3)
C0, C1 : Charge Pump current (see Table 4)
RE: not used in 1795 DS5, for normal operation RE=0
RTS: not used in 1795 DS5, for normal operation RTS=0
TS2, TS1, TS0: not used in 1795 DS5, TS2=TS1=TS0=don´t care
P3,P2,P1,P0: Port output state, P3,P0=don´t care,
Only for types with switchable IF Bandwidth:
P1 and P2 for switching IF Bandwidth

Table 2 - Read Data Format

		MSB							LSB	
Address Byte	Byte 1	1	1	0	0	0	MA1	MA0	1	A
Status Byte	Byte 2	POR	FL	x	x	x	A2	A1	A0	A

A : Acknowledge Bit
MA1, MA0 : Programmable Address Bits (both fixed to zero)
Read Address = $C1
POR : Power-On Reset flag.
FL : In-Lock flag (FL=1 when the loop is phase-locked).
A2, A1, A0 : digital outputs of the 5-level A/D converter, not used in 1795 DS5.

Table 3 - Reference division ratios

R3	R2	R1	R0	Ratio	Comparsion frequency with a 4 MHz ext. reference
0	0	0	0	2	2 MHz
0	0	0	1	4	1 MHz
0	0	1	0	8	500 kHz
0	0	1	1	16	250 kHz
0	1	0	0	32	125 kHz
0	1	0	1	64	62.5 kHz
0	1	1	0	128	31.25 kHz
0	1	1	1	256	15.625 kHz
1	0	0	0	not allowed	-
1	0	0	1	5	800 kHz
1	0	1	0	10	400 kHz
1	0	1	1	20	200 kHz
1	1	0	0	40	100 kHz
1	1	0	1	80	50 kHz
1	1	1	0	160	25 kHz
1	1	1	1	320	12.5 kHz

Table 4 - Charge Pump current

C1	C0	typ. current in µA
0	0	+/- 130
0	1	+/- 280
1	0	+/- 600
1	1	+/- 1300

4.3 Example for determination of divider bytes

Desired Channel Frequency: f_{CH} = 1641.25 MHz

LO frequency: $f_{LO} = f_{CH} + f_{IF}$ = 2120.75 MHz with f_{IF} = 479.5 MHz

f_{LO} > 2 GHz => PE= 1 Prescaler enabled

Choose reference frequency: f_{REF} = 125 kHz

Look up divider ratio in table 4: ratio = 32, R3=0, R2=1, R1=0, R0=0

Programmable Divider N:

$$N = \frac{f_{LO}}{2^{PE}} \cdot \frac{1}{f_{REF}}$$

$$= \frac{2120.75 \cdot 10^6}{2^1} \cdot \frac{1}{125 \cdot 10^3}$$

$$= 8483$$

$$= 2123_{hex}$$

Minimum frequency step: $f_{St} = f_{REF} \cdot 2^{PE} = 125\,kHz \cdot 2 = 250\,kHz$

Choose Charge Pump current: CPC = 130µA
Look up bits in table 4: C1=0, C0=0

Address select voltage fixed at 0 V: MA1 = 0, MA0 = 0

For the example above the following bytes have to be written to the SP5659:

Byte 1	1	1	0	0	0	0	0	0
$	**C**				**0**			
Byte 2	0	0	1	0	0	0	0	1
$	**2**				**1**			
Byte 3	0	0	1	0	0	0	1	1
$	**2**				**3**			
Byte 4	1	0	0	1	0	1	0	0
$	**9**				**4**			
Byte 5	0	0	0	0	0	0	0	0
$	**0**				**0**			

Attention !!

Due to the high free-running frequency of the LO after power up the PLL is not able to lock with the prescaler disabled. Use the prescaler enabled option to program the tuner after a power on reset. Once the PLL is locked, with oscillator frequencies up to 2 GHz the prescaler can be successfully disabled. Enabling of the prescaler is recommended during ALL tuning transitions.

4.4 IF-Bandwidth:

The IF-Bandwidth is switched via IIC Bus with port 1 (P1) and port 2 (P2).

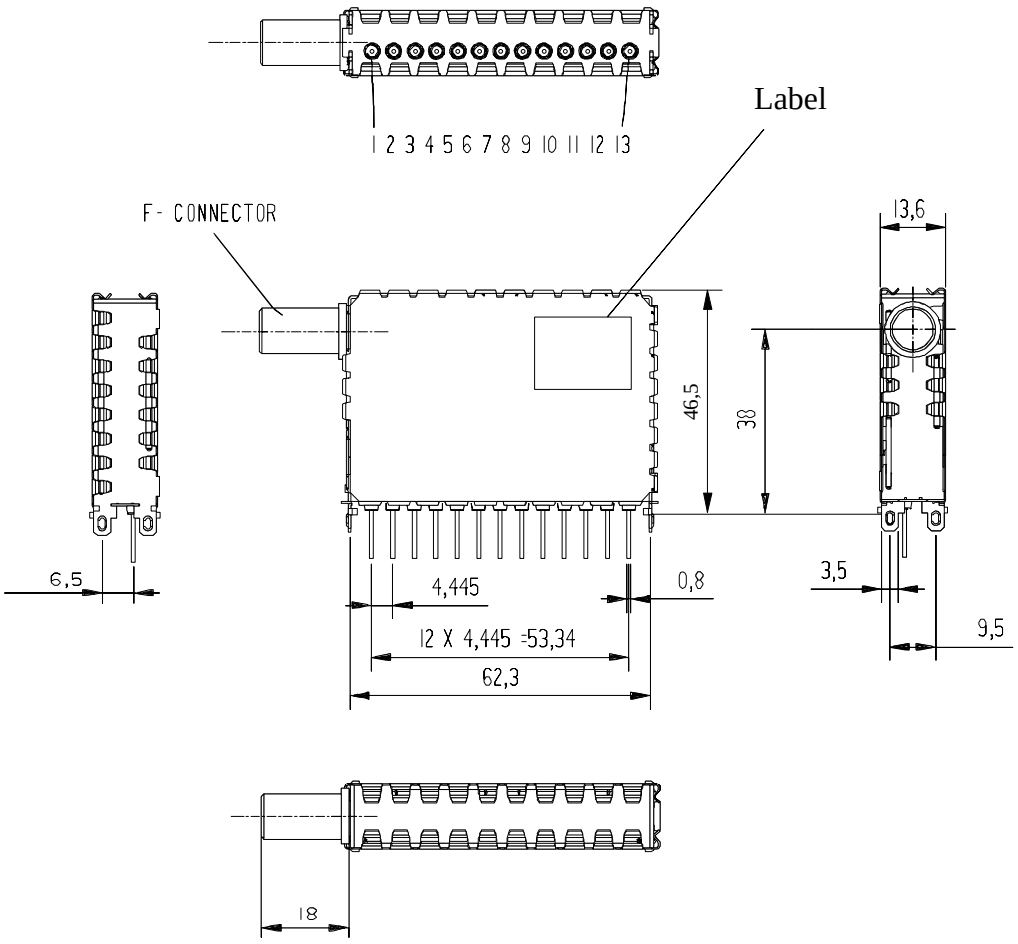
Single Bandwidth:

For single IF bandwidth tuners the port P1 and port P2 are not used.

Dual Bandwidth:		7 / 14 MHz	27 / 36 MHz	27 / 55 MHz
P1 = 0	P2 = 1	IF BW = 14 MHz	IF BW = 36 MHz	IF BW = 55 MHz
P1 = 1	P2 = 0	IF BW = 7 MHz	IF BW = 27 MHz	IF BW = 27 MHz

5. Mechanical characteristics

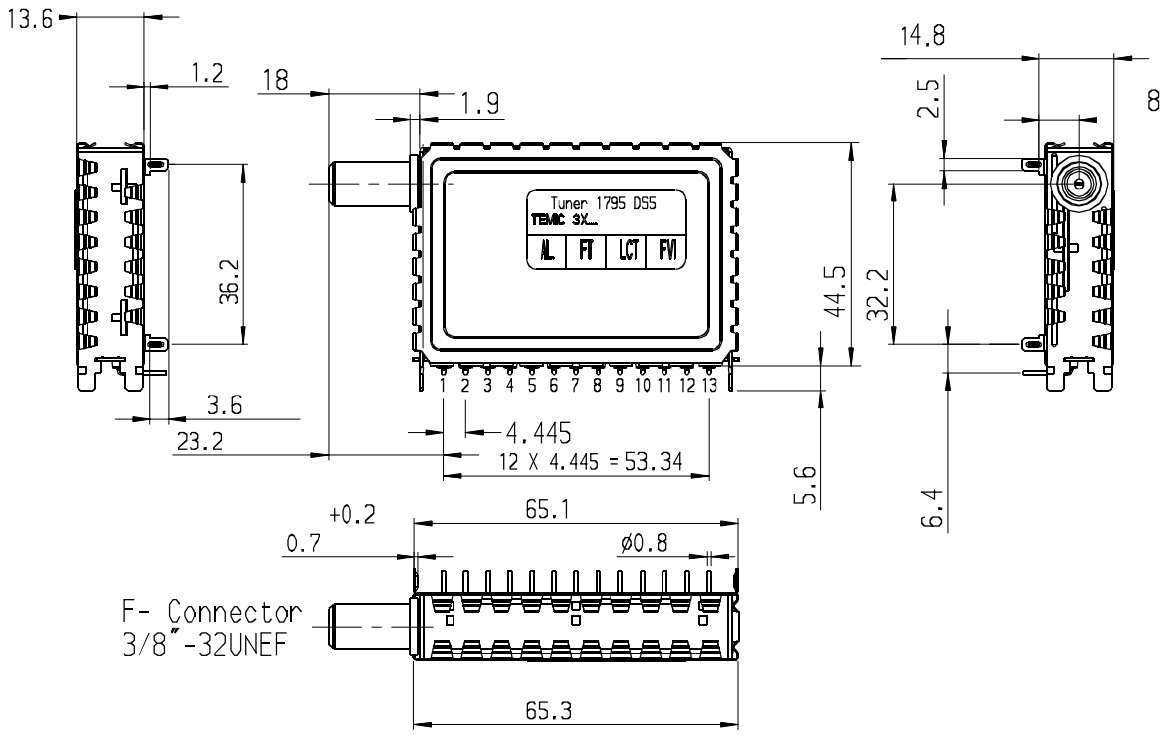
5.1 Vertical version



Pin	Connection		Pin	Connection
1	LNB Supply		8	AGC In
2	n.c.		9	AGC Monitor Out
3	n.c.		10	Power Supply: + 5 V
4	Output I		11	IIC Bus SCL
5	Output Q		12	IIC Bus SDA
6	n.c		13	Tuning Voltage + 28 V
7	n.c.			

Weight: approx. 54 g

5.2 Horizontal version



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5	Output Q		12	IIC Bus SDA
6	n.c.		13	Tuning Voltage + 28 V
7	n.c.			

Weight: approx. 54 g

6. Safety and Reliability

6.1. ESD protection

The tuner contains components that can be damaged by static discharge.

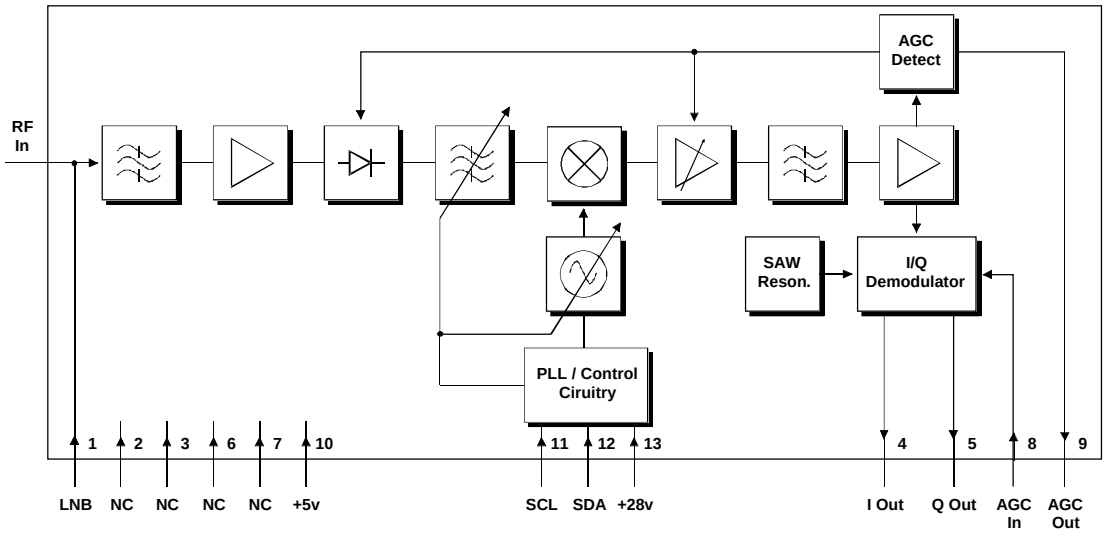
Observe these precautions:
Ground yourself before handling the tuner.
Do not touch the tuner connector pins without ESD protection.

6.2. High Voltage: The tuner meets specifications IEC 1000-4-2.

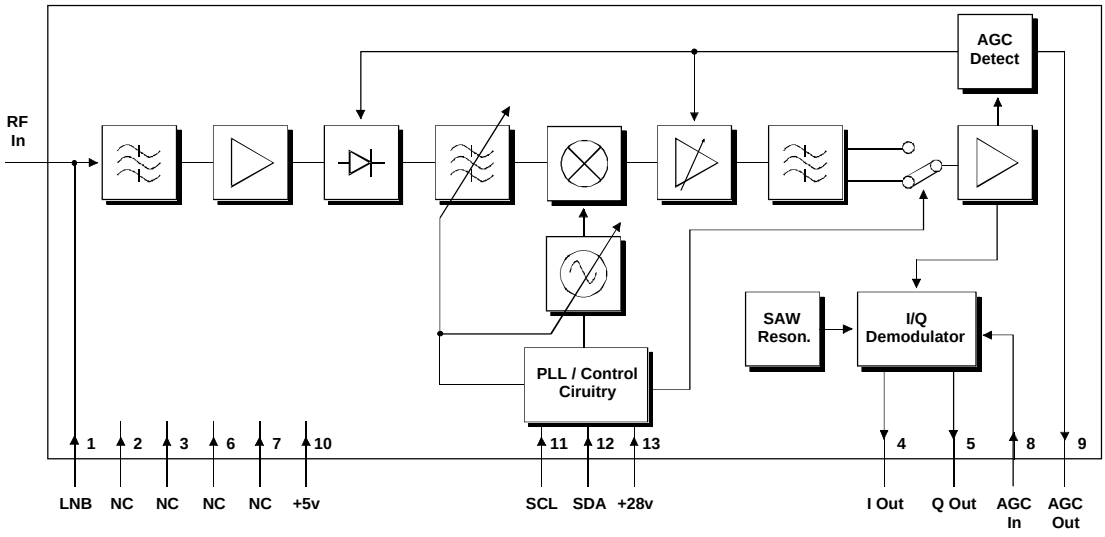
We reserve the right to make changes to improved technical design without further notice.

REV.:	01					
FÄM.- NO.	071					
DATE	10.12.98					
NAME	Stump					

7. Block Diagrams



1795DS5 Electrical Block Diagram -- Fixed Bandwidth Versions



1795DS5 Electrical Block Diagram -- Switched Bandwidth Versions