
Hyperband television tuners

KS-H-94 S1

FEATURES

- * Members of the KS-H-90 family
VHF/Hyperband/UHF tuners
- * Systems CCIR: B/G, H, L/L'
OIRT: D/K
- * Off-air channels, S-cable channels and Hyperband
- * Digitally controlled (PLL) tuning via I²C-bus
- * Compact size
- * Comply to "CENELEC EN55020" and "EN55013"

DESCRIPTION

The KS-H-94 S1 tuners belong to the KS-H-90 family of tuners, which are designed to meet a wide range of applications. It is a combined VHF / Hyperband / UHF tuner suitable for CCIR systems B/G, H, L/L', or OIRT systems D/K. The low IF output impedance has been designed for direct drive of a wide variety of saw filters with sufficient suppression of triple transient.

The tuners comply with the requirements of radiation, signal handling capability and immunity conforming with:

- * CISPR 13 (1990) including amendment 1 (1992) and amendment 2 (1993)
- * European standards CENELEC EN55013, EN 55020

MARKING

The following items of information are printed on a sticker that is on the top cover of the tuner or printed directly on the top cover:

- * Company logo
- * Type number
- * Year and month code
- * Quality inspection print

ORDERING INFORMATION

TYPE	SYSTEM	DESCRIPTION
KS-H-94 ES1	CCIR	symmetrical IF output; IEC connector (14.5 mm)
KS-H-94 OS1	OIRT	symmetrical IF output; IEC connector (14.5 mm)

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INTERMEDIATE FREQUENCIES

SIGNAL	FREQUENCY (MHz)			
	SYSTEM B/G, H	SYSTEM L	SYSTEM L'	SYSTEM D/K
Picture carrier	38.90	38.90	33.40	38.00
Colour	34.47	34.47	37.83	33.594, 33.75
Sound	33.40	32.40	39.90	31.50

Note

1. The oscillator frequency is above the input signal frequency.

CHANNEL COVERAGE

TYPE	BAND	OFF-AIR CHANNELS		CABLE CHANNELS	
		CHANNELS	FREQUENCY RANGE (MHz)	CHANNELS	FREQUENCY RANGE (MHz)
KS-H-94 ES1 OS1	Low band	E2 to C	48.25 to 83.25 ⁽¹⁾	S01 to S6	105.25 to 140.25
	Mid band	E5 to E12	175.25 to 224.25	S7 to S41	143.25 to 463.25
	High band	E21 to E69	471.25 to 855.25 ⁽²⁾		

Notes

1. Enough margin is available to tune down to 45.25 MHz.
2. Enough margin is available to tune up to 863.25 MHz.

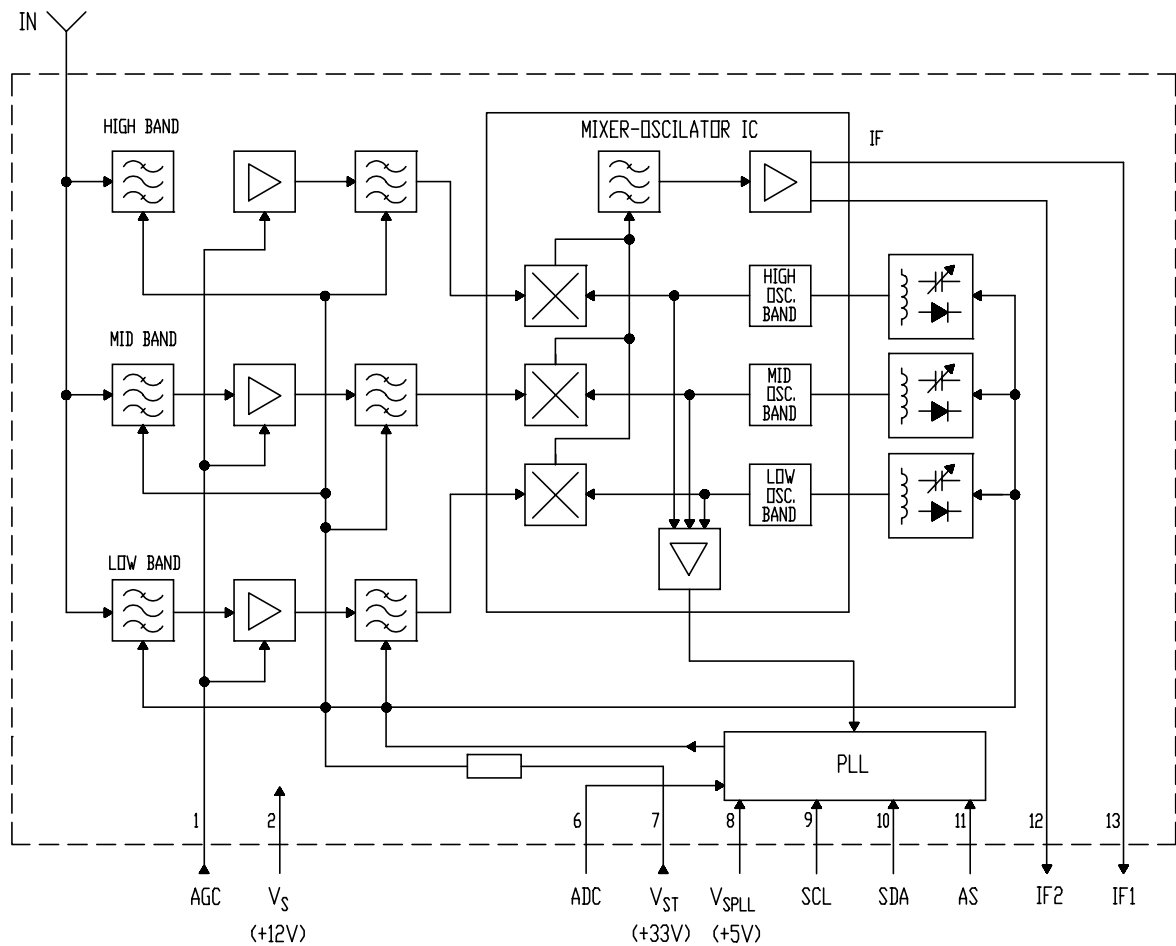


Fig.1 Electrical block diagram

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PINNING

SYMBOL	PIN	DESCRIPTION
AGC	1	gain control voltage
V _S	2	supply voltage +12 V
ADC	6	ADC output/input
V _{ST}	7	Tuning voltage +33 V
V _{SPLL}	8	PLL supply voltage +5 V
SCL	9	I ² C bus-serial clock
SDA	10	I ² C-bus serial data
AS	11	I ² C-bus address select
IF2	12	Symmetrical IF output
IF1	13	Symmetrical IF output
GND	MT1, MT2	mounting tags (ground)
	IN	aerial input connector IEC (14.5 mm)

LIMITING VALUES

Environmental conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Non-operational conditions					
T _{amb}	ambient temperature		-40	+60	°C
RH	relative humidity		85	%	
Operational conditions					
T _{amb}	ambient temperature		-10	+60	°C
RH	relative humidity		93	%	

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Limiting values under operational conditions

The tuner can be guaranteed to function properly under the following conditions.

SYMBOL	PARAMETER	PIN	MIN.	TYP.	MAX.	UNIT
V_S I_S	supply voltage supply current	2	10.8	12	13.2 85	V mA
V_{ST} I_{ST}	tuning supply voltage tuning supply current	7	30	33	35 1.7	V mA
V_{SPLL} I_{SPLL}	PLL supply voltage PLL supply current	8	4.75	5	5.5 75	V mA
V_{AGC} ΔV_{AGC} I_{AGC}	AGC input voltage AGC input voltage range AGC input current	1	0.85	9.2	13.2 9.7 30	V V μ A
V_{AS} V_{SCL} V_{SDA} I_{SDA}	address select input voltage serial clock input voltage serial data input voltage serial data input current	11 9 10	 -0.3 -0.3 1	 	5.5 5.5 5.5 5	V V V mA

ELECTRICAL DATA

Conditional data

Unless otherwise specified, all electrical values for Chapter "Electrical data" apply at the following conditions and the electrical performance is related both to systems B/G, H, L/L' and D/K.

A proper function is guaranteed within the specified operational conditions but a certain deterioration of performance parameters may occur at the limits of operational conditions.

SYMBOL	PARAMETER	VALUE	UNIT
T_{amb}	ambient temperature	25 +/- 5	$^{\circ}$ C
RH	relative humidity	60 +/- 15	%
V_S	supply voltage	12 +/- 0.25	V
V_{SPLL}	PLL supply voltage	5 +/- 0.125	V
V_{AGC}	AGC input voltage	9.2 +/- 0.25	V
V_{ST}	tuning supply voltage	33 +/- 0.5	V
t_{pr}	pre-heating time (+12 V at pin 2)	10	minute
$Z_{S(AE)}$	aerial source impedance (unbalanced)	75	Ω

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Aerial input characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
WSWR	reflection coefficient	referred to 75 Ω impedance		4	
V_{ant}	antenna connection disturbance voltage	< 1.75 GHz; comply to "EN55013 section 3.3"		46	dB μ V

General characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_b	frequency range, low band mid band high band		48.25 143.25 471.25	140.25 463.25 855.25	MHz MHz MHz
G_v	voltage gain: all channels gain taper		40	7	dB dB
F	noise: low band mid band high band			9 10 10	dB dB dB
ΔV_{AGC}	AGC input voltage range: low and mid band high band		45 40		dB dB
α_i	image rejection: low band mid band high band		70 65 53		dB dB dB
α_{IF}	IF rejection (picture) low and mid band high band		60 70		
Δf	oscillator characteristics Oscillator tuning resolution lock-in time			note 1 150	kHz msec

Note 1. Resolution 31.25 kHz, 50.00 kHz or 62.5 kHz (see Table "Ratio select bits").

Visibility test

The tuners meet the requirements of the European norm "EN55020", when measured in an adequate television receiver.

Radiation

The tuners meet the requirements of the European norm "EN55013" and "CISPR13" (1990), when measured in an adequate television receiver.

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APPLICATION INFORMATION

WRITE mode

	MSB							LSB	A ⁽¹⁾
Address byte	1	1	0	0	0	MA1	MA0	R/W ⁽²⁾	A
Program divider byte 1	0	n14	n13	n12	n11	n10	n9	n8	A
Program divider byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A
Control information byte 1	1	CP	0	0	1	RSA	RSB	0	A
Control information byte 2	P7	P6	P5	P4	X	P2	P1	P0	A

Notes

1. A = Acknowledge
2. R/W bit = 0 for WRITE mode, R/W bit = 1 for READ mode

Address selection

MA1	MA0	Voltage at pin 11
0	0	GND to $0.1XV_{PLL}$
0	1	OPEN or $0.2XV_{PLL}$ to $0.3XV_{PLL}$
1	0	$0.4XV_{PLL}$ to $0.7XV_{PLL}$
1	1	$0.8XV_{PLL}$ to $1.1XV_{PLL}$

Programmable divider settings (bytes 1 and 2)

Divider ratio:

$$N = R \times \{ f_{RF,pc} + f_{IF,pc} \},$$

$$R = 16 \text{ with reference divider} = 512$$

$$R = 20 \text{ with reference divider} = 640$$

$$R = 32 \text{ with reference divider} = 1024$$

$$N = (16384 \times n14) + (8192 \times n13) + (4096 \times n12) + (2048 \times n11) + (1024 \times n10) + (512 \times n9) + (256 \times n8) + (128 \times n7) + (64 \times n6) + (32 \times n5) + (16 \times n4) + (8 \times n3) + (4 \times n2) + (2 \times n1) + n0$$

Control byte 1

CP can be set to either 0 (low current) or 1 (high current).

Charge pump settings:

CP = 1, for fast tuning

CP = 0, for moderate speed tuning with slightly better residual oscillator FM.

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Ratio select bits

RSA	RSB	REFERENCE DIVIDER	STEP SIZE (kHz)
X	0	640	50.00
0	1	1024	31.25
1	1	512	62.50

Band switching
(Control byte 2)

Band	Active port	P7	P6	P5	P4	X	P2	P1	P0
Low band	P1	X	X	X	X	X	0	1	0
Mid band	P2	X	X	X	X	X	1	0	0
High band	P0	X	X	X	X	X	0	0	1

READ mode

	MSB							LSB	
Address byte	1	1	0	0	0	MA1	MA0	1	A
Status byte	POR	FL	X	X	X	A2	A1	A0	A

- Notes
1. A = Acknowledge.
 2. POR = Power On Reset flag (POR=1 at power on).
 3. FL = In-lock flag (FL=1 at loop is phase-locked).

ADC byte

A2	A1	A0	Voltage at pin 6
1	0	0	$0.60XV_{PLL}$ to V_{PLL}
0	1	1	$0.45XV_{PLL}$ to $0.60XV_{PLL}$
0	1	0	$0.30XV_{PLL}$ to $0.45XV_{PLL}$
0	0	1	$0.15XV_{PLL}$ to $0.30XV_{PLL}$
0	0	0	0 to $0.15XV_{PLL}$

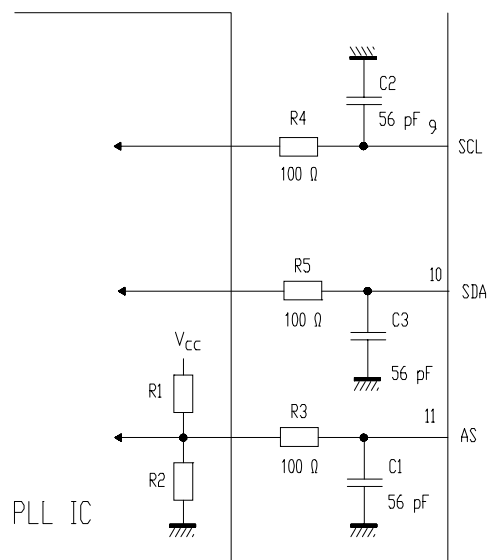
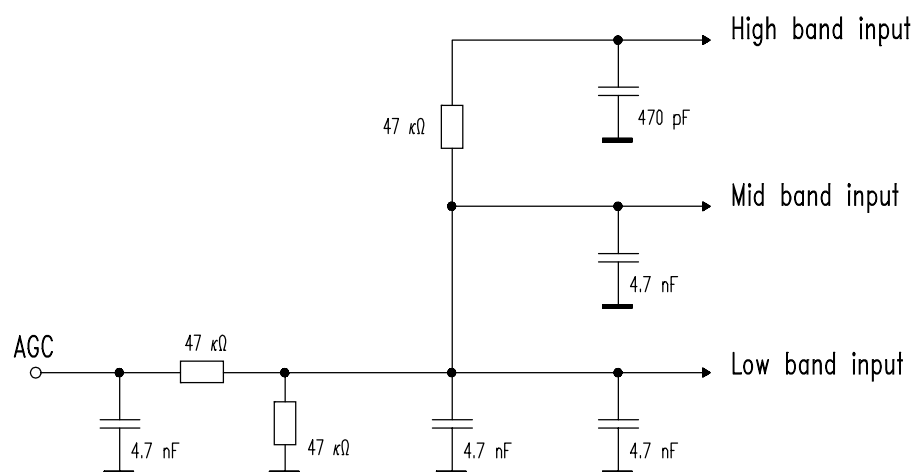
Fig.2 I²C-bus load.

Fig.3 Internal AGC circuit.

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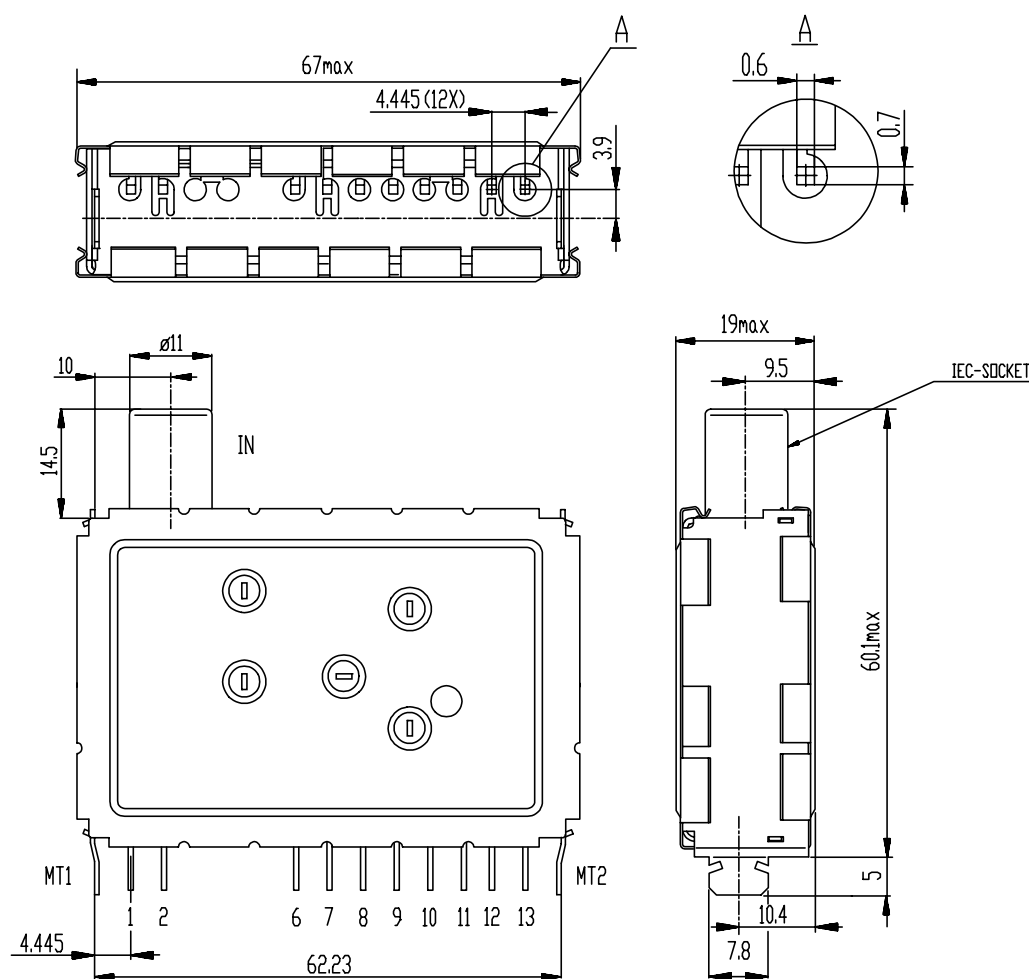


Fig.4 Mechanical outline

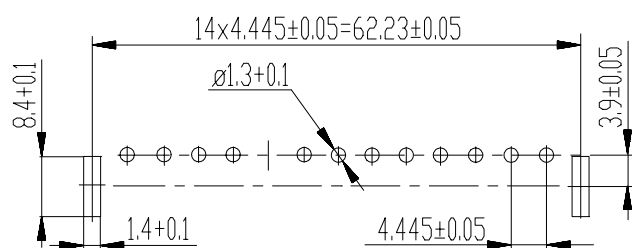


Fig.5 Punching pattern seen from solder side

Aerial connections

Standard IEC socket female 75 Ω .

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Selteka customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Selteka for any damages resulting from such improper use or sale.