

**Hyperband television tuner****KS-H-132 S****FEATURES**

- Member of the KS-H-130 family small sized VHF/Hyperband/UHF tuner
- Systems CCIR: B/G, H; OIRT: D/K
- Digitally controlled (PLL) tuning via I<sup>2</sup>C-bus
- Off-air channels, S-cable channels and Hyperband
- World standardized mechanical dimensions and world standard pinning
- Transformer (balun) on antenna input provides an additional output.
- Compact size
- Comply to "CENELEC EN55020" and "EN55013"

**MARKING**

The following items of information are printed on a sticker that is on the top cover of the tuner or printed directly on the top cover:

- Company logo
- Type number
- Year and month code
- Quality inspection print

**DESCRIPTION**

The KS-H-132S tuner belongs to the KS-H-130 family of tuners, which are designed to meet a wide range of applications. It is a combined VHF/Hyperband/UHF tuner suitable for CCIR systems B/G, H, or OIRT systems D/K. The low IF output impedance has been designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple transient.

An integrated splitter allows to use the tuner in PIP applications via a IEC-plug (male) output (75Ω).

The tuners comply with the requirements of radiation, signal handling capability and immunity conforming with:

- CISPR 13 (1990) include. amendment 1 (1992) and amendment 2 (1993)
- European standards CENELEC EN55013, EN55020

**ORDERING INFORMATION**

| TYPE        | SYSTEM | DESCRIPTION   |
|-------------|--------|---|
| KS-H-132 ES | CCIR   | symmetrical IF output; IEC connectors (14.5 mm), I <sup>2</sup> C status byte |
| KS-H-132 OS | OIRT   | symmetrical IF output; IEC connectors (14.5 mm), I <sup>2</sup> C status byte |

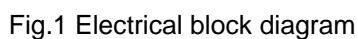
**KS-H-132 S**

| SIGNAL          | FREQUENCY (MHz) |               |
|-----------------|-----------------|---------------|
|                 | SYSTEM B/G, H   | SYSTEM D/K    |
| Picture carrier | 38.90           | 38.00         |
| Colour          | 34.47           | 33.594, 33.75 |
| Sound           | 33.40           | 31.5          |

1. The oscillator frequency is above the input signal frequency.

| BAND      | OFF-AIR CHANNELS |                                 | CABLE CHANNELS |                       |
|-----------|------------------|---------------------------------|----------------|-----------------------|
|           | CHANNELS         | FREQUENCY RANGE (MHz)           | CHANNELS       | FREQUENCY RANGE (MHz) |
| Low band  | E2 to C          | 48.25 to 82.25 <sup>(1)</sup>   | S01 to S10     | 69.25 to 168.25       |
| Mid band  | E5 to E12        | 175.25 to 224.25                | S11 to S41     | 231.25 to 463.25      |
| High band | E21 to E69       | 471.25 to 855.25 <sup>(2)</sup> |                |                       |

1. Enough margin is available to tune down to 45.25 MHz.
2. Enough margin is available to tune up to 863.25 MHz.



## Hyperband television tuner

KS-H-132 S

## PINNING

| SYMBOL          | PIN      | DESCRIPTION   |
|-----------------|----------|---|
| AGC             | 1        | gain control voltage                                |
| V <sub>T</sub>  | 2        | tuning voltage                                      |
| AS              | 3        | I <sup>2</sup> C-bus address select                 |
| SCL             | 4        | I <sup>2</sup> C-bus serial clock                   |
| SDA             | 5        | I <sup>2</sup> C-bus serial data                    |
| n.c.            | 6        | not connected                                       |
| V <sub>S</sub>  | 7        | PLL supply voltage +5 V                             |
| ADC             | 8        | ADC input   |
| V <sub>ST</sub> | 9        | tuning supply voltage +33 V                         |
| IF2             | 10       | symmetrical IF output                               |
| IF1             | 11       | symmetrical IF output                               |
| GND             | MT1, MT2 | mounting tags (ground)                              |
| IN              |          | aerial input connector IEC-socket (14.5 mm, female) |
| OUT             |          | aerial output connector IEC-plug (14.5 mm, male)    |

## LIMITING VALUES

## Environmental conditions

| SYMBOL                            | PARAMETER           | MIN. | MAX. | UNIT |
|-----------------------------------|---------------------|------|------|------|
| <b>Non-operational conditions</b> |                     |      |      |      |
| T <sub>amb</sub>                  | ambient temperature | -40  | +60  | °C   |
| RH                                | relative humidity   | -    | 100  | %    |
| <b>Operational conditions</b>     |                     |      |      |      |
| T <sub>amb</sub>                  | ambient temperature | -15  | +60  | °C   |
| RH                                | relative humidity   | -    | 93   | %    |

## Hyperband television tuner

## KS-H-132 S

## Limiting values under operational conditions

The tuner can be guaranteed to function properly under the following conditions

| SYMBOL           | PARAMETER                    | PIN | MIN. | TYP. | MAX. | UNIT    |
|------------------|------------------------------|-----|------|------|------|---------|
| $V_S$            | supply voltage               | 7   | 4.75 | 5.00 | 5.5  | V       |
| $I_S$            | supply current               |     | -    | -    | 130  | mA      |
| $V_{ST}$         | supply voltage               | 9   | 30   | 33   | 35   | V       |
| $I_{ST}$         | supply current               |     | -    | -    | 1.7  | mA      |
| $V_{AGC}$        | AGC input voltage            | 1   | -    | 4.0  | 4.5  | V       |
| $\Delta V_{AGC}$ | AGC input voltage range      |     | 0.3  | -    | 4.0  | V       |
| $I_{AGC}$        | AGC input current            |     | -    | -    | 20   | $\mu$ A |
| $V_{AS}$         | address select input voltage | 3   | -    | -    | 5.5  | V       |
| $V_{SCL}$        | serial clock input voltage   | 4   | -    | -    | 5.5  | V       |
| $V_{SDA}$        | serial data input voltage    | 5   | -    | -    | 5.5  | V       |
| $I_{SDA}$        | serial data input current    |     | -1   | -    | 5    | mA      |

## ELECTRICAL DATA

## Conditional data

Unless otherwise specified, all electrical values for Chapter "Electrical data" apply at the following conditions and the electrical performance is related both to systems B, G, H and D, K.

A proper function is guaranteed within the specified operational conditions but a certain deterioration of performance parameters may occur at the limits of operational conditions.

| SYMBOL      | PARAMETER                            | VALUE       | UNIT         |
|-------------|--------------------------------------|-------------|--------------|
| $T_{amb}$   | ambient temperature                  | 25 +/- 5    | $^{\circ}$ C |
| RH          | relative humidity                    | 60 +/- 15   | %            |
| $V_S$       | supply voltage                       | 5.0 +/- 0.1 | V            |
| $V_{AGC}$   | AGC input voltage                    | 4.0 +/- 0.1 | V            |
| $V_{ST}$    | tuning supply voltage                | 33 +/- 0.5  | V            |
| $t_{pr}$    | pre-heating time (+5 V at pin 7)     | 10          | minute       |
| $Z_{S(AE)}$ | aerial source impedance (unbalanced) | 75          | $\Omega$     |

## Hyperband television tuner

## KS-H-132 S

## Aerial input characteristics

| SYMBOL           | PARAMETER                              | CONDITIONS                                  | MIN. | TYP. | MAX. | UNIT       |
|------------------|--|---|------|------|------|------------|
| VSWR             | reflection coefficient                 | referred to 75 $\Omega$ impedance           | -    | 2    | 4    |            |
| V <sub>ant</sub> | antenna connection disturbance voltage | < 1.75 GHz; comply to "EN55013 section 3.3" | -    | -    | 46   | dB $\mu$ V |

## General characteristics

| SYMBOL           | PARAMETER                             | CONDITIONS  | MIN.   | TYP. | MAX.   | UNIT |
|------------------|---------------------------------------|---|--------|------|--------|------|
| f <sub>p</sub>   | frequency range:                      |   |        |      |        |      |
|                  | low band                              |   | 48.25  | -    | 168.25 | MHz  |
|                  | mid band                              |   | 175.25 | -    | 463.25 | MHz  |
|                  | high band                             |   | 471.25 | -    | 855.25 | MHz  |
| G <sub>v</sub>   | voltage gain:                         | The IF output is loaded with a test circuit according diagram fig.2 |        |      |        |      |
|                  | all channels                          |   | 36     | 42   | 48     | dB   |
|                  | gain taper                            |   | -      | -    | 7      | dB   |
| F                | noise:                                | The IF output is loaded with a test circuit according diagram fig.3 |        |      |        |      |
|                  | low band                              |   | -      | 10.0 | 14     | dB   |
|                  | mid band                              |   | -      | 10.0 | 14     | dB   |
|                  | high band                             |   | -      | 9.0  | 13     | dB   |
| $\Delta V_{AGC}$ | AGC input voltage range:              |   |        |      |        |      |
|                  | low and mid band                      |   | 45     | 60   | -      | dB   |
|                  | high band                             |   | 40     | 50   | -      | dB   |
| $\alpha_i$       | image rejection:                      |   |        |      |        |      |
|                  | low band                              |   | 66     | 70   | -      | dB   |
|                  | mid band                              |   | 60     | 69   | -      | dB   |
|                  | high band                             |   | 50     | 60   | -      | dB   |
| $\alpha_{IF}$    | IF rejection (picture):               |   |        |      |        |      |
|                  | channel E2                            |   | 55     | 68   | -      | dB   |
|                  | low, mid and high bands               |   | 65     | 71   | -      | dB   |
| V <sub>ESD</sub> | electrostatic discharge (ESD):        | note 1  |        |      |        |      |
|                  | protection on pins 1 to 5 and 6 to 11 |   | 2      | -    | -      | kV   |
|                  | protection on antenna socket and plug |   | 8      | -    | -      | kV   |
|                  | oscillator characteristics:           |   |        |      |        |      |
|                  | oscillator tuning resolution          |   | -      | -    | note 2 | kHz  |
|                  | lock-in time                          |   | -      | -    | 150    | msec |

## Notes

1. The tuner meets specifications IEC 1000-4-2 level 1 for pins and level 4 for antenna socket.
2. Resolution 31.25 kHz, 50.00 kHz or 62.5 kHz (see Table "Ratio select bits").
3. For all measurements the splitter output should be loaded with 75  $\Omega$ .

## Hyperband television tuner

KS-H-132 S

## Visibility test

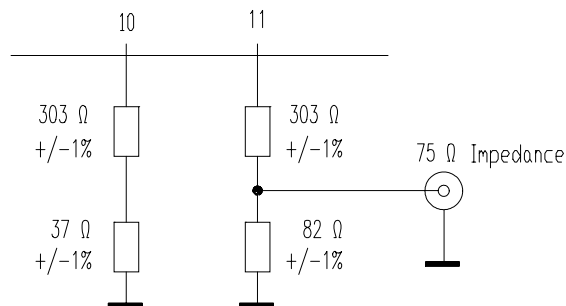
The tuners meet the requirements of the European norm "EN55020", when measured in an adequate television receiver.

## Recommended adjustment of Tuner AGC in TV chassis:

Channel: E21 (471.25 MHz PC-frequency)  
 Input level: 70 dB $\mu$ V/75  $\Omega$   
 IF output level: 105 dB $\mu$ V  
 Gain reduction: 10 dB  
 AGC-Voltage: 2.9 V  $\pm$ 0.2V

## Radiation

The tuners meet the requirements of the European norm "EN55013" and "CISPR13" (1990), when measured in an adequate television receiver.



test circuit attenuation : 26 dB

Fig. 2 Test circuit for voltage gain.

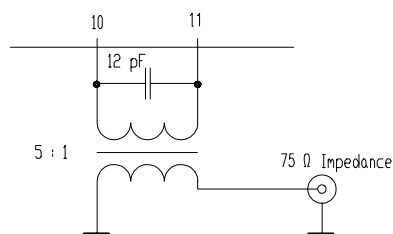


Fig. 3 Test circuit for noise figure.

## Hyperband television tuner

## KS-H-132 S

## APPLICATION INFORMATION

## WRITE mode

| BYTE                       | BITS                    |     |     |     |     |     |     |                   |                  |
|----------------------------|-------------------------|-----|-----|-----|-----|-----|-----|-------------------|------------------|
|                            | 7 <sup>(1)</sup><br>MSB | 6   | 5   | 4   | 3   | 2   | 1   | 0<br>LSB          | A <sup>(2)</sup> |
| Address byte               | 1                       | 1   | 0   | 0   | 0   | MA1 | MA2 | RW <sup>(3)</sup> | A                |
| Program divider byte 1     | 0                       | n14 | n13 | n12 | n11 | n10 | n9  | n8                | A                |
| Program divider byte 2     | n7                      | n6  | n5  | n4  | n3  | n2  | n1  | n0                | A                |
| Control information byte1  | 1                       | CP  | 0   | 0   | 1   | RSA | RSB | 0                 | A                |
| Control information byte 2 | P7                      | P6  | P5  | P4  | X   | P2  | P1  | P0                | A                |

## Notes

1. X = don't care.
2. A = Acknowledge.
3. R/W bit = 0 for WRITE mode, R/W bit = 1 for READ mode.

## Address selection

$V_s = \pm 5$  V (PLL supply voltage).

| MA1 | MA0 | ADDRESS | VOLTAGE AT PIN 3               |
|-----|-----|---------|--------------------------------|
| 0   | 0   | C0      | GND to $0.1XV_s$               |
| 0   | 1   | C2      | OPEN or $0.2XV_s$ to $0.3XV_s$ |
| 1   | 0   | C4      | $0.4XV_s$ to $0.7XV_s$         |
| 1   | 1   | C6      | $0.8XV_s$ to $1.1XV_s$         |

## Programmable divider settings (bytes 1 and 2)

Divider ratio:

$$N = R \times \{ f_{RF,pc} + f_{IF,pc} \},$$

R = 16 with reference divider = 512

R = 20 with reference divider = 640

R = 32 with reference divider = 1024

$$N = (16384 \times n_{14}) + (8192 \times n_{13}) + (4096 \times n_{12}) + (2048 \times n_{11}) + (1024 \times n_{10}) + (512 \times n_9) + (256 \times n_8) + (128 \times n_7) + (64 \times n_6) + (32 \times n_5) + (16 \times n_4) + (8 \times n_3) + (4 \times n_2) + (2 \times n_1) + n_0$$

## Control byte 1

CP can be set to either 0 (low current) or 1 (high current).

Charge pump settings:

CP = 1, for fast tuning

CP = 0, for moderate speed tuning with slightly better residual oscillator FM.

Unnecessary charge pump action will result in very low tuning voltage ( $V_T=0V$ ) which may drive the oscillator to extreme conditions.

## Hyperband television tuner

KS-H-132 S

## Ratio select bits

| RSA | RSB | REFERENCE DIVIDER | STEP SIZE (kHz) |
|-----|-----|-------------------|-----------------|
| X   | 0   | 640               | 50.00           |
| 0   | 1   | 1024              | 31.25           |
| 1   | 1   | 512               | 62.50           |

## Band switching (Control byte 2)

| BIT       |    |    |    |    |    |    |           | ACTIVE PORT | BAND      |
|-----------|----|----|----|----|----|----|-----------|-------------|-----------|
| P7<br>MSB | P6 | P5 | P4 | P3 | P2 | P1 | P0<br>LSB |             |           |
| X         | X  | X  | X  | X  | 0  | 1  | 0         | P1          | Low band  |
| X         | X  | X  | X  | X  | 1  | 0  | 0         | P2          | Mid band  |
| X         | X  | X  | X  | X  | 0  | 0  | 1         | P0          | High band |

## READ mode

| BYTE         | BITS               |                   |   |   |   |                   |                   |                   |                  |
|--------------|--------------------|-------------------|---|---|---|-------------------|-------------------|-------------------|------------------|
|              | 7<br>MSB           | 6                 | 5 | 4 | 3 | 2                 | 1                 | 0<br>LSB          | A <sup>(1)</sup> |
| Address byte | 1                  | 1                 | 0 | 0 | 0 | MA1               | MA0               | 1                 | A                |
| Status byte  | POR <sup>(2)</sup> | FL <sup>(3)</sup> | X | X | X | A2 <sup>(4)</sup> | A1 <sup>(4)</sup> | A0 <sup>(4)</sup> | A                |

## Notes

1. A = Acknowledge.
2. POR = Power On Reset flag (POR=1 at power on).
3. FL = In-lock flag (FL=1 at loop is phase-locked).
4. A2, A1, and A0 are the digital outputs of the 5 level ADC.

## ADC byte

| VOLTAGE AT PIN 8         | A2 | A1 | A0 |
|--------------------------|----|----|----|
| $0.60XV_S$ to $V_S$      | 1  | 0  | 0  |
| $0.45XV_S$ to $0.60XV_S$ | 0  | 1  | 1  |
| $0.30XV_S$ to $0.45XV_S$ | 0  | 1  | 0  |
| $0.15XV_S$ to $0.30XV_S$ | 0  | 0  | 1  |
| 0 to $0.15XV_S$          | 0  | 0  | 0  |



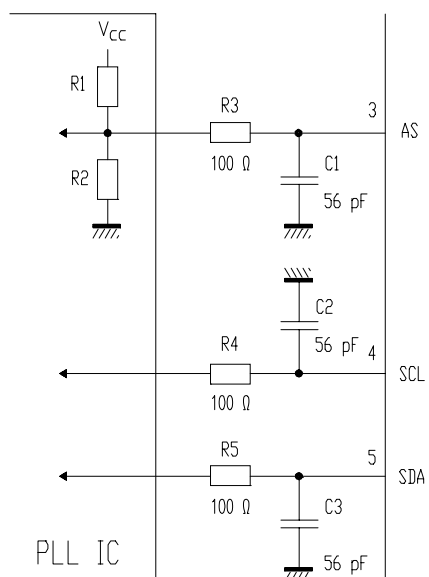
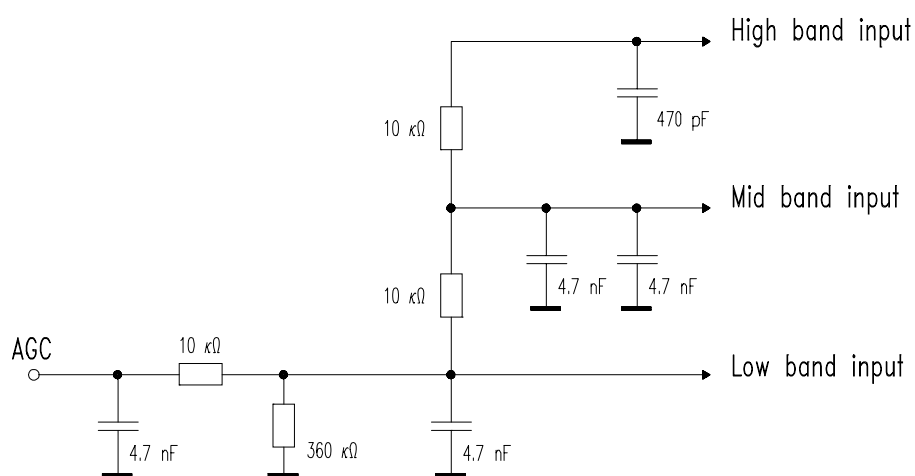
Fig.4 I<sup>2</sup>C-bus load.

Fig.5 Internal AGC circuit.

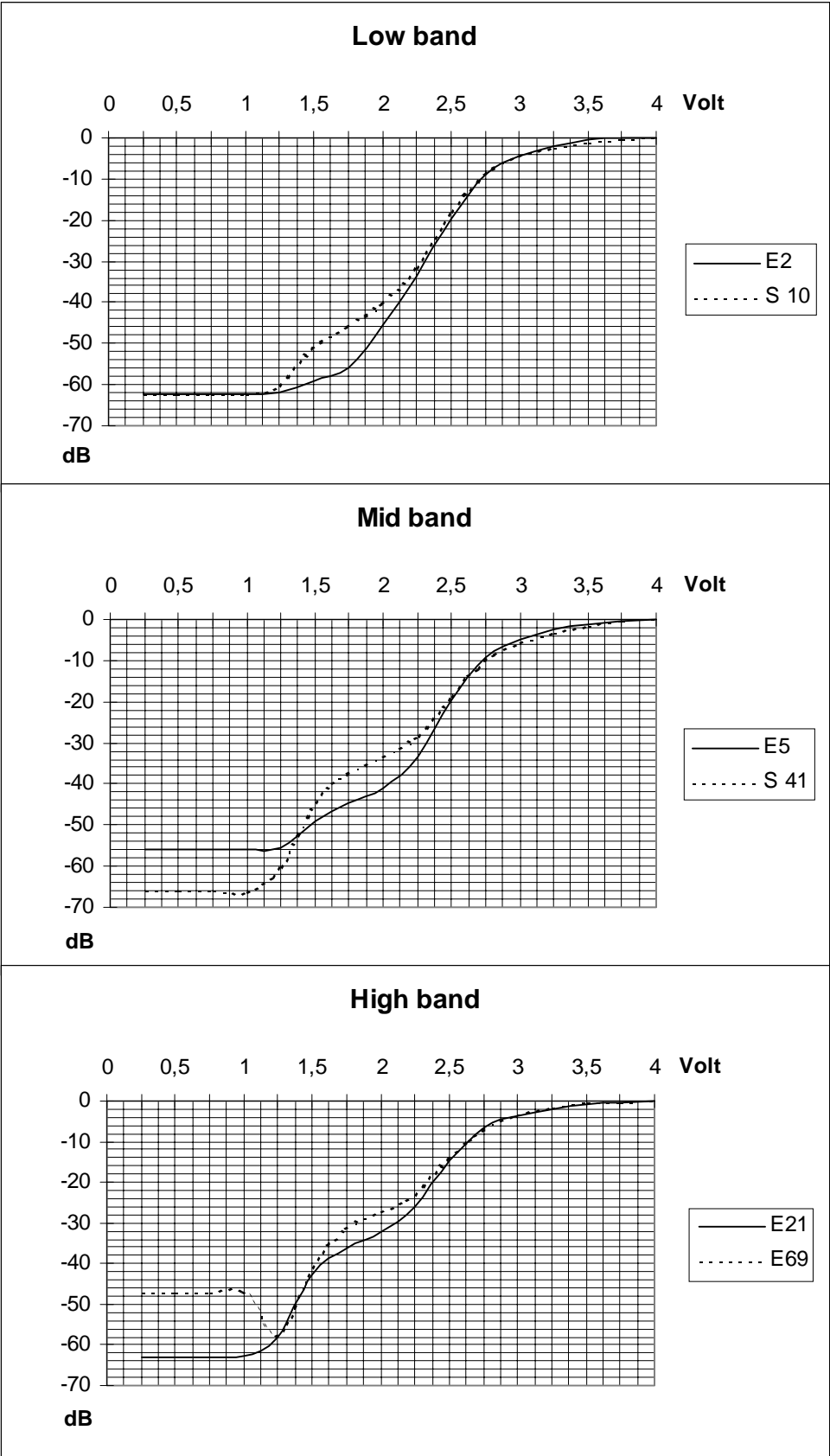


Fig.6 AGC characteristics.

## Hyperband television tuner

KS-H-132 S

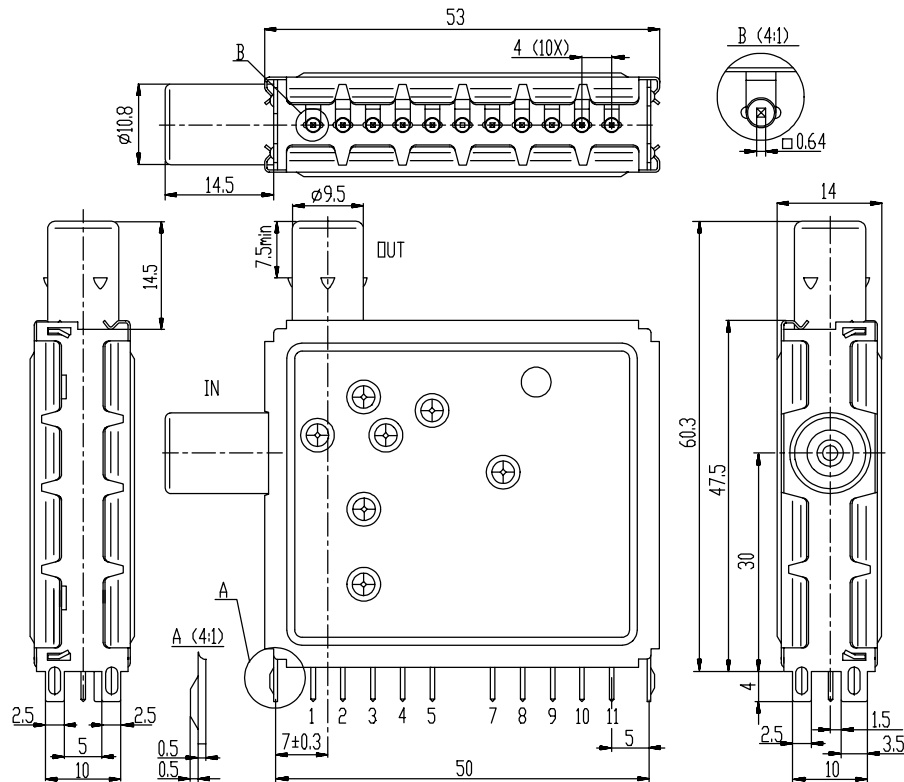


Fig.7 Mechanical outline

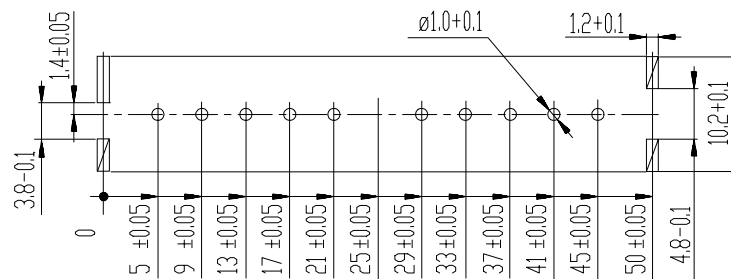


Fig.8 Punching pattern seen from solder side

**Aerial connections**

Standard IEC socket female 75  $\Omega$ .

**LIFE SUPPORT APPLICATIONS**

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