SECTION 2

REFERENCES AND LOW DROPOUT LINEAR REGULATORS

Walt Jung

Reference circuits and linear regulators actually have much in common. In fact, the latter could be functionally described as a reference circuit, but with greater current (or power) output. Accordingly, almost all of the specifications of the two circuit types have great commonality (even though the performance of references is usually tighter with regard to drift, accuracy, etc.). This chapter is broadly divided into an initial discussion on voltage references, followed by a concluding discussion on linear regulators, with emphasis on their low dropout operation for highest power efficiency.

PRECISION VOLTAGE REFERENCES

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Voltage references have a major impact on the performance and accuracy of analog systems. A ±5mV tolerance on a 5V reference corresponds to ±0.1% absolute accuracy–only 10-bits. For a 12-bit system, choosing a reference that has a ±1mV tolerance may be far more cost effective than performing manual calibration, while both high initial accuracy and calibration will be necessary in a system making absolute 16-bit measurements. Note that many systems make *relative* measurements rather than absolute ones, and in such cases the absolute accuracy of the reference is not important, although noise and short-term stability may be. Figure 2.1 summarizes some key points of the reference selection process.

Temperature drift or drift due to aging may be an even greater problem than absolute accuracy. The initial error can always be trimmed, but compensating for drift is difficult. Where possible, references should be chosen for temperature coefficient and aging characteristics which preserve adequate accuracy over the operating temperature range and expected lifetime of the system.

Noise in voltage references is often overlooked, but it can be very important in system design. It is generally specified on data sheets, but system designers frequently ignore the specification and assume that voltage references do not contribute to system noise.

There are two dynamic issues that must be considered with voltage references: their behavior at start-up, and their behavior with transient loads. With regard to the first, always bear in mind that voltage references *do not power up instantly* (this is true of references inside ADCs and DACs as well as discrete designs). Thus it is rarely possible to turn on an ADC and reference, whether internal or external, make

a reading, and turn off again within a few microseconds, however attractive such a procedure might be in terms of energy saving.

Regarding the second point, a given reference IC may or may not be well suited for pulse-loading conditions, dependent upon the specific architecture. Many references use low power, and therefore low bandwidth, output buffer amplifiers. This makes for poor behavior under fast transient loads, which may degrade the performance of fast ADCs (especially successive approximation and flash ADCs). Suitable decoupling can ease the problem (but some references oscillate with capacitive loads), or an additional external broadband buffer amplifier may be used to drive the node where the transients occur.

References, like almost all other ICs today, are fast migrating to such smaller packages such as SO-8, and the even more tiny SOT-23, enabling much higher circuit densities within a given area of real estate. In addition to the system size reductions these steps bring, there are also tangible reductions in standby power and cost with the smaller and less expense ICs.

CHOOSING VOLTAGE REFERENCES FOR HIGH PERFORMANCE SYSTEMS

- **Tight Tolerance Improves Accuracy, Reduces System Costs**
- **Temperature Drift Affects Accuracy**
- **Long-Term Stability, Low Hysteresis Assures Repeatability**
- **Noise Limits System Resolution**
- **Dynamic Loading Can Cause Errors**
- **Power Consumption is Critical to Battery Systems**
- **Tiny Low Cost Packages Increase Circuit Density**

Figure 2.1

TYPES OF VOLTAGE REFERENCES

In terms of the functionality of their circuit connection, standard reference ICs are often only available in *series*, or *three-terminal* form (V_{IN}, Common, V_{OUT}), and also in positive polarity only. The series types have the potential advantages of lower and more stable quiescent current, standard pre-trimmed output voltages, and relatively high output current without accuracy loss. *Shunt*, or *two-terminal* (i.e., diode-like) references are more flexible regarding operating polarity, but they are also more restrictive as to loading. They can in fact eat up excessive power with widely varying resistor-fed voltage inputs. Also, they sometimes come in non-standard voltages. All of these various factors tend to govern when one functional type is preferred over the other.

Some simple diode-based references are shown in Figure 2.2. In the first of these, a current driven forward biased diode (or diode-connected transistor) produces a voltage, $V_f = V_{REF}$. While the junction drop is somewhat decoupled from the raw supply, it has numerous deficiencies as a reference. Among them are a strong TC of about –0.3%/°C, some sensitivity to loading, and a rather inflexible output voltage: it is only available in 600mV jumps.

By contrast, these most simple references (as well as all other shunt-type regulators) have a basic advantage, which is the fact that the polarity is readily reversible by flipping connections and reversing the drive current. However, a basic limitation of all shunt regulators is that load current must always be less (usually appreciably less) than the driving current, I_D.

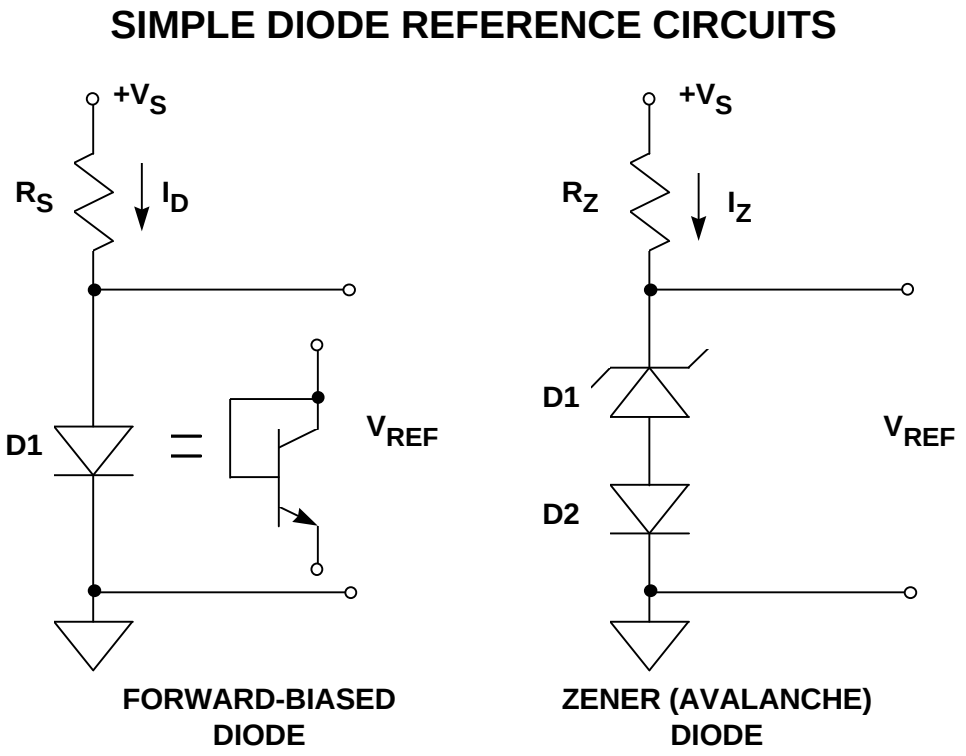

Figure 2.2

In the second circuit of Figure 2.2, a zener or avalanche diode is used, and an appreciably higher output voltage realized. While true *zener* breakdown occurs below 5V, *avalanche* breakdown occurs at higher voltages and has a positive temperature coefficient. Note that diode reverse breakdown is referred to almost universally today as *zener*, even though it is usually avalanche breakdown. With a D1 breakdown voltage in the 5 to 8V range, the net positive TC is such that it equals the negative TC of forward-biased diode D2, yielding a net TC of 100ppm/°C or less with proper bias current. Combinations of such carefully chosen diodes formed the basis of the early single package "temperature-compensated zener" references, such as the 1N821-1N829 series.

The temperature-compensated zener reference is limited in terms of initial accuracy, since the best TC combinations fall at odd voltages, such as the 1N829's 6.2V. And,

the scheme is also limited for loading, since for best TC the diode current must be carefully controlled. Unlike a fundamentally lower voltage (<2V) reference, zener diode based references must of necessity be driven from voltage sources appreciably higher than 6V levels, so this precludes operation of zener references from 5V system supplies. References based on low TC zener (avalanche) diodes also tend to be noisy, due to the basic noise of the breakdown mechanism. This has been improved greatly with *monolithic* zener types, as is described further below.

At this point, we know that a reference circuit can be functionally arranged into either a series or shunt operated form, and the technology within may use either bandgap based or zener diode based circuitry. In practice there are all permutations of these available, as well as a third major technology category. The three major reference technologies are now described in more detail.

BANDGAP REFERENCES

The development of low voltage (<5V) references based on the bandgap voltage of silicon led to the introductions of various ICs which could be operated on low voltage supplies with good TC performance. The first of these was the LM109 (Reference 1), and a basic bandgap reference cell is shown in Figure 2.3.

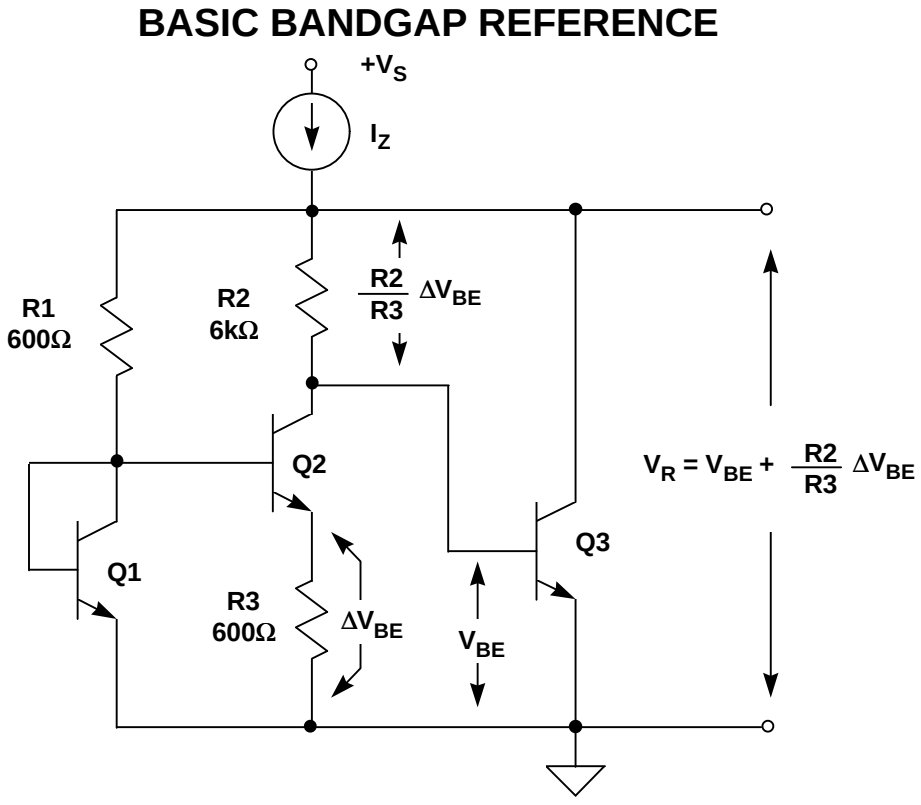

Figure 2.3

This circuit is also called a "ΔV_{BE}" reference because the differing current densities between matched transistors Q1-Q2 produces a ΔV_{BE} across R3. It works by summing the V_{BE} of Q3 with the amplified ΔV_{BE} of Q1-Q2, developed across R2. The ΔV_{BE} and V_{BE} components have opposite polarity TCs; ΔV_{BE} is proportional-to-absolute-temperature (PTAT), while V_{BE} is complementary-to-absolute-temperature (CTAT). The summed output is V_R, and when it is equal to 1.205V (silicon bandgap voltage), the TC is a minimum.

The bandgap reference technique is attractive in IC designs because of several reasons; among these are the relative simplicity, and the avoidance of zeners and their noise. However, very important in these days of ever decreasing system supplies is the fundamental fact that bandgap devices operate at low voltages, i.e., <5V. Not only are they used for stand-alone IC references, but they are also used within the designs of many other linear ICs such as ADCs, DACs, and op-amps.

Buffered forms of 1.2V two terminal bandgap references, such as the AD589 IC, remain stable under varying load currents. The H-02A metal can AD589, a 1.235V reference, handles 50µA to 5mA with an output impedance of 0.6Ω, and TCs ranging between 10 and 100ppm/°C. The more recent and functionally similar AD1580, a 1.225V reference, is in the tiny SOT-23 package and handles the same nominal currents as the AD589, with TCs of 50 and 100ppm/°C.

However, the basic designs of Figure 2.3 suffer from load and current drive sensitivity, plus the fact that the output needs accurate scaling to more useful levels, i.e., 2.5V, 5V, etc. The load drive issue is best addressed with the use of a buffer amplifier, which also provides convenient voltage scaling to standard levels.

An improved three-terminal bandgap reference, the AD580, is shown in Figure 2.4. Popularly called the "Brokaw Cell" (see References 2 and 3), this circuit provides on-chip output buffering, which allows good drive capability and standard output voltage scaling. The AD580 was the first precision bandgap based IC reference, and variants of the topology have influenced further generations of both industry standard references such as the REF01 and REF02 series, as well as more recent ADI parts such as the REF195 series, the AD680, AD780, and the AD1582-85 series.

The AD580 has two 8:1 emitter-scaled transistors Q1-Q2 operating at identical collector currents (and thus 1/8 current densities), by virtue of equal load resistors and a closed loop around the buffer op-amp. Due to the resultant smaller V_{BE} of the 8× area Q2, R2 in series with Q2 drops the ΔV_{BE} voltage, while R1 (due to the current relationships) drops a PTAT voltage V1:

$$V_1 = 2 \times \frac{R1}{R2} \times \Delta V_{BE} \quad .$$

AD580 PRECISION BANDGAP REFERENCE USES BROKAW CELL

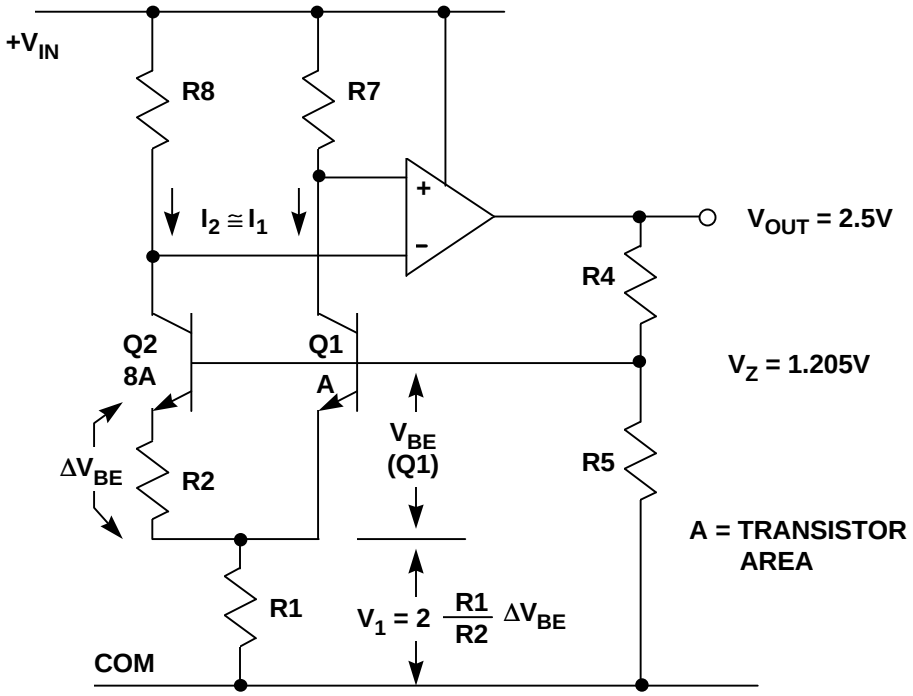

Figure 2.4

The bandgap cell reference voltage V_Z appears at the base of Q1, and is the sum of V_{BE}(Q1) and V1, or 1.205V, the bandgap voltage:

$$
\begin{aligned}
V_Z &= V_{BE(Q1)} + V_1 \\
&= V_{BE(Q1)} + 2 \times \frac{R1}{R2} \times \Delta V_{BE} \\
&= V_{BE(Q1)} + 2 \times \frac{R1}{R2} \times \frac{kT}{q} \times \ln \frac{J1}{J2} \\
&= V_{BE(Q1)} + 2 \times \frac{R1}{R2} \times \frac{kT}{q} \times \ln 8 \\
&= 1.205V\ .
\end{aligned}
$$

Note that J1 = current density in Q1, J2 = current density in Q2, and J1/J2 = 8.

However, because of the presence of the R4/R5 (laser trimmed) thin film divider and the op-amp, the actual voltage appearing at V_{OUT} can be scaled higher, in the AD580 case 2.5V. Following this general principle, V_{OUT} can be raised to other practical levels, such as for example in the AD584, with taps for precise 2.5, 5, 7.5, and 10V operation. The AD580 provides up to 10mA output current while operating from supplies between 4.5 and 30V. It is available in tolerances as low as 10mV, with TCs as low as 10ppm/°C.

Many of the recent developments in bandgap references have focused on smaller package size and cost reduction, to address system needs for smaller, more power efficient and less costly reference ICs. Among these are several recent bandgap based IC references.

The AD1580 is a shunt mode IC reference which is functionally quite similar to the classic shunt IC reference, the AD589 mentioned above. A key difference is the fact that the AD1580 uses a newer, small geometry process, enabling its availability within the tiny SOT-23 package. The very small size of this package allows use in a wide variety of space limited applications, and the low operating current lends itself to portable battery powered uses. The AD1580 circuit is shown in simplified form in Figure 2.5.

AD1580 1.2V SHUNT TYPE BANDGAP REFERENCE HAS TINY SIZE IN SOT-23 FOOTPRINT

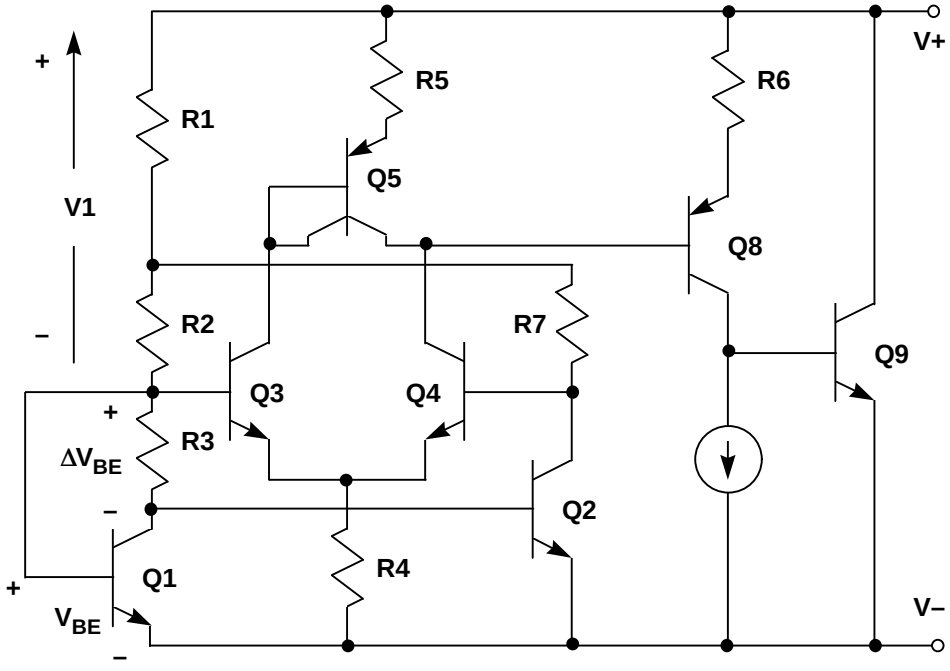

Figure 2.5

In this circuit, like transistors Q1 and Q2 form the bandgap core, and are operated at a current ratio of 5 times, determined by the ratio of R7 to R2. An op amp is formed by the differential pair Q3-Q4, current mirror Q5, and driver/output stage Q8-Q9. In closed loop equilibrium, this amplifier maintains the bottom ends of R2-R7 at the same potential.

As a result of the closed loop control described, a basic ΔV_{BE} voltage is dropped across R3, and a scaled PTAT voltage also appears as V1, which is effectively in series with V_{BE}. The nominal bandgap reference voltage of 1.225V is then the sum of Q1's V_{BE} and V1. The AD1580 is designed to operate at currents as low as 50 µA, also handling maximum currents as high as 10 mA. It is available in grades with voltage tolerances of ±1 or ±10 mV, and with corresponding TC's of 50 or 100 ppm/°C.

The AD1582-AD1585 series comprises a family of series mode IC references, which produce voltage outputs of 2.5, 3.0, 4.096 and 5.0V. Like the AD1580, the series uses a small geometry process to allow packaging within an SOT-23. The AD1582 series specifications are summarized in Figure 2.6.

AD1582-AD1585 2.5-5V SERIES TYPE BANDGAP SERIES SPECIFICATIONS

- **V_{OUT} : 2.500, 3.000, 4.096, & 5.000V**
- **2.7V to 12V Supply Range**
- **Supply Current : 65µA max**
- **Initial Accuracy: ±0.1% max**
- **Temperature Coefficient: 50 ppm/°C max**
- **Noise: 50µV rms (10Hz - 10kHz)**
- **Long-Term Drift: 100ppm/1khrs**
- **High Output Current: ±5mA min**
- **Temperature Range –40°C to +85°C**
- **Low Cost SOT-23 Package**

Figure 2.6

The circuit diagram for the series, shown in Figure 2.7, may be recognized as a variant of the basic Brokaw bandgap cell, as described under Figure 2.4. In this case Q1-Q2 form the core, and the overall loop operates to produce the stable reference voltage V_{BG} at the base of Q1. A notable difference here is that the op amp's output stage is designed with push-pull common-emitter stages. This has the effect of requiring an output capacitor for stability, but it also provides the IC with relatively low dropout operation. The low dropout feature means essentially that V_{IN} can be lowered to as close as several hundred mV above the V_{OUT} level without disturbing operation. The push-pull operation also means that this device series can actually both sink and source currents at the output, as opposed to the classic reference operation of sourcing current (only). For the various output voltage ratings, the divider R5-R6 is adjusted for the respective levels.

The AD1582 series is designed to operate with quiescent currents of only 65µA (maximum), which allows good power efficiency when used in low power systems with varying voltage inputs. The rated output current for the series is 5 mA, and they are available in grades with voltage tolerances of ±0.1 or ±1% of V_{OUT}, with corresponding TC's of 50 or 100ppm/°C.

Because of stability requirements, devices of the AD1582 series must be used with both an output and input bypass capacitor. Recommended worst case values for these are shown in the hookup diagram of Figure 2.8. For the electrical values noted, it is likely that tantalum chip capacitors will be the smallest in size.

AD1582-AD1585 2.5-5V SERIES TYPE BANDGAP REFERENCES HAVE TINY SIZE IN SOT-23 FOOTPRINT

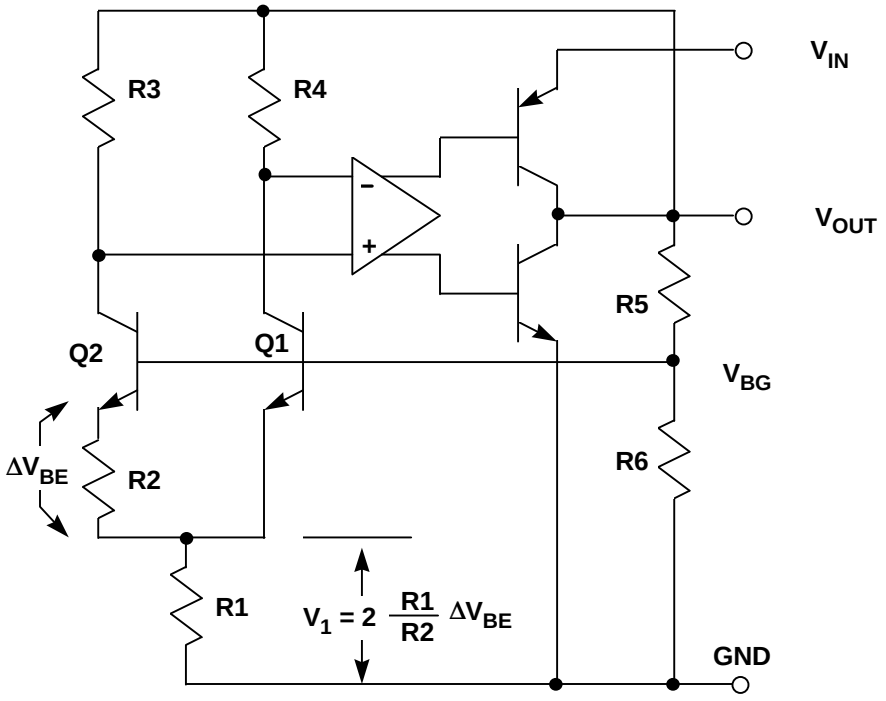

Figure 2.7

AD1582-AD1585 SERIES CONNECTION DIAGRAM

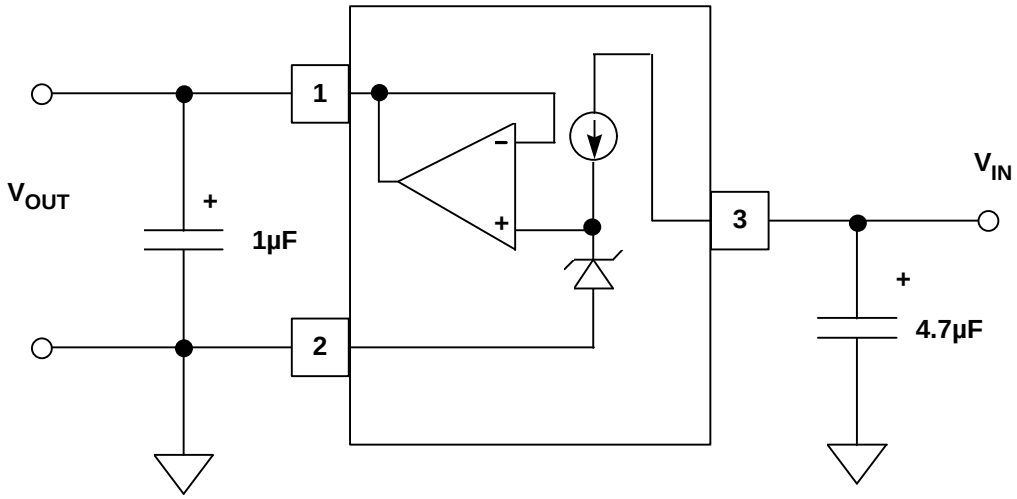

Figure 2.8

BURIED ZENER REFERENCES

In terms of the design approaches used within the reference core, the two most popular basic types of IC references consist of the bandgap and buried zener units. Bandgaps have been discussed, but zener based references warrant some further discussion.

In an IC chip, surface operated diode junction breakdown is prone to crystal imperfections and other contamination, thus zener diodes formed at the surface are more noisy and less stable than are *buried* (or sub-surface) ones. ADI zener based IC references employ the much preferred buried zener. This improves substantially upon the noise and drift of surface-mode operated zeners (see Reference 4). Buried zener references offer very low temperature drift, down to the 1-2ppm/°C (AD588 and AD586), and the lowest noise as a percent of full-scale, i.e., 100nV/√Hz or less. On the downside, the operating current of zener type references is usually relatively high, typically on the order of several mA.

An important general point arises when comparing noise performance of different references. The best way to do this is to compare the ratio of the noise (within a given bandwidth) to the DC output voltage. For example, a 10V reference with a 100nV/√Hz noise density is 6dB more quiet in relative terms than is a 5V reference with the same noise level.

XFET™ REFERENCES

A third and brand new category of IC reference core design is based on the properties of junction field effect (JFET) transistors. Somewhat analogous to the bandgap reference for bipolar transistors, the JFET based reference operates a pair of junction field effect transistors with different pinchoff voltages, and amplifies the differential output to produce a stable reference voltage. One of the two JFETs uses an extra ion implantation, giving rise to the name XFET™ (eXtra implantation junction Field Effect Transistor) for the reference core design.

The basic topology for the XFET™ reference circuit is shown in Figure 2.9. J1 and J2 are the two JFET transistors, which form the core of the reference. J1 and J2 are driven at the same current level from matched current sources, I1 and I2. To the right, J1 is the JFET with the extra implantation, which causes the difference in the J1-J2 pinchoff voltages to differ by 500mV. With the pinchoff voltage of two such FETs purposely skewed, a differential voltage will appear between the gates for identical current drive conditions and equal source voltages. This voltage, ΔV_P, is:

$$\Delta V_P = V_{P1} - V_{P2},$$

where V_{P1} and V_{P2} are the pinchoff voltages of FETs J1 and J2, respectively.

ADR290-ADR293 2.048-5V XFET™ REFERENCE TOPOLOGY FEATURES HIGH STABILITY AND LOW POWER

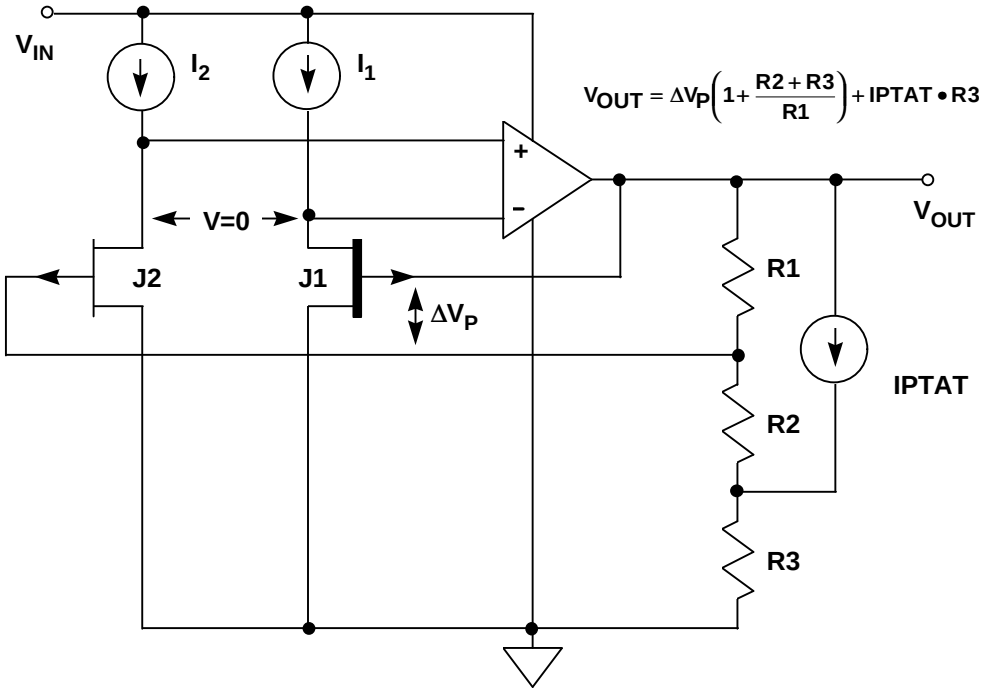

Figure 2.9

Note that, within this circuit, the voltage ΔV_P exists between the *gates* of the two FETs. We also know that, with the overall feedback loop closed, the op amp axiom of zero input differential voltage will hold the sources of the two JFET at same potential. These source voltages are applied as inputs to the op amp, the output of which drives feedback divider R1-R3. As this loop is configured, it stabilizes at an output voltage from the R1-R2 tap which does in fact produce the required ΔV_P between the J1-J2 gates. In essence, the op amp amplifies ΔV_P to produce V_{OUT},where

$$V_{OUT} = \Delta V_P\left(1+\frac{R2+R3}{R1}\right) + (I_{PTAT})(R3).$$

As can be noted, this expression includes the basic output scaling (leftmost portion of the right terms), plus a rightmost temperature dependent term including I_{PTAT}. The I_{PTAT} portion of the expression compensates for a basic negative temperature coefficient of the XFET™ core, such that the overall net temperature drift of the reference is typically in a range of 3 to 8ppm/°C.

During manufacture, the R1-R3 scaling resistance values are adjusted to produce the different voltage output options of 2.048, 2.5, 4.096 and 5.0V for the ADR290, ADR291, ADR292 and ADR293 family (ADR29X). This ADR29X family of series mode references is available in 8 pin packages with a standard footprint, as well as a TO-92 3 lead format. They operate from supplies of V_{OUT} plus 200mV to 15V, with a typical quiescent current of 12 µA, and output currents of up to 5 mA. A summary of specifications for the family appears in Figure 2.10.

ADR290-ADR293 XFET™ SERIES SPECIFICATIONS

- **V_{OUT} : 2.048, 2.500, 4.096, & 5.000V**
- **2.7V to 15V Supply Range**
- **Supply Current : 12µA max**
- **Initial Accuracy: ±2 mV max**
- **Temperature Coefficient: 8 ppm/°C max**
- **Low-Noise: 6µVp-p (0.1 - 10Hz)**
- **Wideband Noise: 420nV/√Hz @ 1kHz**
- **Long-Term Drift: 0.2ppm/1khrs**
- **High Output Current: 5mA min**
- **Temperature Range –40°C to +125°C**
- **Standard REF02 Pinout**
- **8-Lead Narrow Body SOIC, 8-Lead TSSOP, and 3-Lead TO-92**

Figure 2.10

The XFET™ architecture offers performance improvements over bandgap and buried zener references, particularly for systems where operating current is critical, yet drift and noise performance must still be excellent. XFET™ noise levels are lower than bandgap based bipolar references operating at an equivalent current, the temperature drift is low and linear at 3-8 ppm/°C (allowing easier compensation when required), and the series has lower hysteresis than bandgaps. Thermal hysteresis is a low 50ppm over a –40 to +125°C range, less that half that of a typical bandgap device. Finally, the long-term stability is excellent, typically only 0.2ppm/1000 hours.

Figure 2.11 summarizes the pro and con characteristics of the three reference architectures; bandgap, buried zener, and XFET™.

Modern IC references come in a variety of styles, but series operating, fixed output positive types do tend to dominate. These devices can use bandgap based bipolars, JFETs, or buried zeners at the device core, all of which has an impact on the part's ultimate performance and application suitability. They may or may not also be low power, low noise, and/or low dropout, and be available within a certain package. Of course, in a given application, any single one of these differentiating factors can drive a choice, thus it behooves the designer to be aware of all the different devices available.

CHARACTERISTICS OF REFERENCE ARCHITECTURES

BANDGAP	BURIED ZENER	XFET™
< 5V Supplies	> 5V Supplies	< 5V Supplies
High Noise @ High Power	Low Noise @ High Power	Low Noise @ Low Power
Fair Drift and Long Term Stability	Good Drift and Long Term Stability	Excellent Drift and Long Term Stability
Fair Hysteresis	Fair Hysteresis	Low Hysteresis

Figure 2.11

STANDARD POSITIVE OUTPUT THREE TERMINAL REFERENCE HOOKUP (8-PIN DIP PINOUT)

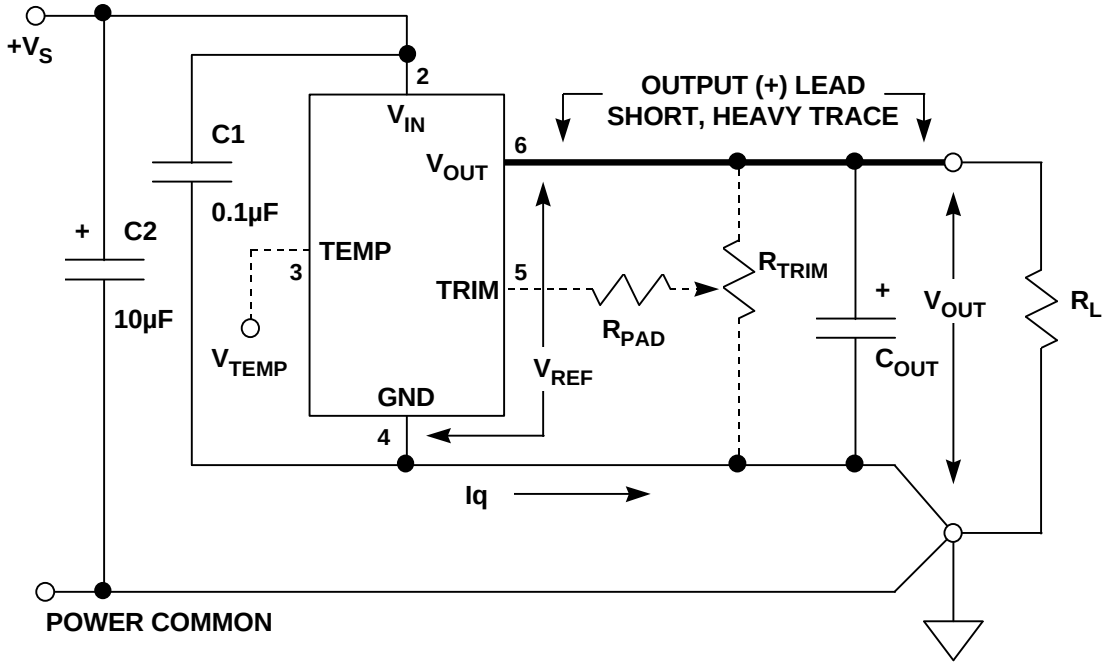

Figure 2.12

Figure 2.12 shows the standard footprint for such a series type IC positive reference in an 8 pin package (Note that "(x)" numbers refer to the standard pin for that function). There are several details which are important. Many references allow optional trimming by connecting an external trim circuit to drive the references' *trim* input pin (5). Some bandgap references also have a high impedance PTAT output (V_{TEMP}) for temperature sensing (3). The intent here is that no appreciable current be drawn from this pin, but it can be useful for such non-loading types of connections as comparator inputs, to sense temperature thresholds, etc.

All references should use decoupling capacitors on the input pin (2), but the amount of decoupling (if any) placed on the output (6) depends upon the stability of the reference's output op-amp with capacitive load. Simply put, there is no hard and fast rule for capacitive loads here. For example, some three terminal types *require* the output capacitor (i.e., REF19X and AD1582-85 series), while with others it is optional for performance improvement (AD780, REF43). The safest rule then is that you should verify what are the specific capacitive loading ground rules for the reference you intend to use, for the load conditions your circuit presents.

VOLTAGE REFERENCE SPECIFICATIONS

TOLERANCE

It is usually better to select a reference with the required value and accuracy and to avoid external trimming and scaling if possible. This allows the best TCs to be realized, as tight tolerances and low TCs usually go hand-in-hand. Tolerances as low as 0.04% can be achieved with the AD586, AD780, REF195, while the AD588 is 0.01%. If and when trimming must be used, be sure to use the recommended trim network with no more range than is absolutely necessary. When/if additional external scaling is required, a precision op-amp should be used, along with ratio-accurate, low TC tracking thin film resistors.

DRIFT

The XFET™ and buried zener reference families have the best long term drift and TC performance. TCs as low as 1-2ppm/°C are available with the AD586 and AD588, and the AD780 bandgap reference is almost as good at 3ppm/°C. The XFET™ series achieve long terms drifts of 0.2 ppm/1000 hours, while the buried zener types come in at 25ppm/1000 hours. Note that where a figure is given for long term drift, it is usually drift expressed in ppm/1000 hours. There are 8766 hours in a year, and many engineers multiply the 1000 hour figure by 8.77 to find the annual drift - this is not correct, and can in fact be quite pessimistic. Long term drift in precision analog circuits is a "random walk" phenomenon and increases with the *square root* of the elapsed time (this supposes that drift is due to random micro-effects in the chip and not some over-riding cause such as contamination). The 1 year figure will therefore be about $\sqrt{8.766} \approx 3$ times the 1000 hour figure, and the ten year value will be roughly 9 times the 1000 hour value. In practice, things are a little better even than this, as devices tend to stabilize with age.

The accuracy of an ADC or DAC can be no better than that of its reference. Reference temperature drift affects fullscale accuracy as shown in Figure 2.13. This table shows system resolution and the TC required to maintain 1/2 LSB error over an operating temperature range of 100°C. For example, a TC of about 1ppm/°C is required to maintain 1/2LSB error at 12-bits. For smaller operating temperature ranges, the drift requirement will be less. The last three columns of the table show the voltage value of 1/2 LSB for popular full scale ranges.

REFERENCE TEMPERATURE DRIFT REQUIREMENTS FOR VARIOUS SYSTEM ACCURACIES (1/2 LSB CRITERIA, 100°C SPAN)

		½ LSB WEIGHT (mV) 10, 5, AND 2.5V FULLSCALE RANGES		
BITS	REQUIRED DRIFT (ppm/°C)	10V	5V	2.5V
8	19.53	19.53	9.77	4.88
9	9.77	9.77	4.88	2.44
10	4.88	4.88	2.44	1.22
11	2.44	2.44	1.22	0.61
12	1.22	1.22	0.61	0.31
13	0.61	0.61	0.31	0.15
14	0.31	0.31	0.15	0.08
15	0.15	0.15	0.08	0.04
16	0.08	0.08	0.04	0.02

Figure 2.13

SUPPLY RANGE

IC reference supply voltages range from about 3V (or less) above rated output, to as high as 30V (or more) above rated output. Exceptions are devices designed for low dropout, such as the REF195 and the AD1582-AD1585 series. At low currents, the REF195 can deliver 5V with an input as low as 5.1V (100mV dropout). Note that due to process limits, some references may have more restrictive maximum voltage input ranges, such as the AD1582-AD1585 series (12V), or the ADR29X series (18V).

LOAD SENSITIVITY

Load sensitivity (or output impedance) is usually specified in µV/mA of load current, or mΩ. While figures of 100µV/mA (100mΩ) or less are quite good (AD780, REF43, REF195), it should be noted that external wiring drops can produce comparable errors at high currents, without care in layout. Load current dependent errors are minimized with short, heavy conductors on the (+) output and on the ground return. For the highest precision, buffer amplifiers and Kelvin sensing circuits (AD588 and AD688) are used to ensure accurate voltages at the load.

The output of a buffered reference is the output of an op amp, and therefore the source impedance is a function of frequency. Typical reference output impedance rises at 6dB/octave from the DC value, and is nominally about 10Ω at a few hundred kHz. This impedance can be lowered with an external capacitor, provided the op-amp within the reference remains stable for such loading.

LINE SENSITIVITY

Line sensitivity (or regulation) is usually specified in µV/V of input change, and is lower than 50µV/V (–86dB) in the REF43, REF195, AD680, and AD780. For DC and very low frequencies, such errors are easily masked by noise.

As with op-amps, the line sensitivity (or power supply rejection) of references degrades with increasing frequency, typically 30 to 50dB at a few hundred kHz. For this reason, the reference input should be highly decoupled (LF and HF). Line rejection can also be increased with a low dropout pre-regulator, such as one of the ADP3300 series parts.

Figure 2.14 summarizes the major reference specifications.

VOLTAGE REFERENCE DC SPECIFICATIONS (TYPICAL VALUES AVAILABLE)

- **Tolerance:**
  - **AD588: 0.01%**
  - **AD586, AD780, REF195: 0.04%**
- **Drift (TC):**
  - **AD586, AD588: 1-2ppm/°C**
  - **AD780, ADR29X 3 ppm/°C**
- **Drift (long term):**
  - **ADR29X: 0.2 ppm/1000 hours**
  - **AD588: 25 ppm/1000 hours**
- **Supply Range:**
  - **REF19X, AD1582-AD1585: V_{OUT} plus ~0.5 V**
- **Load Sensitivity: 100µV/mA (100mohm)**
- **Line Sensitivity: 50µV/V (-86 dB)**

Figure 2.14

NOISE

Reference noise is not always specified, and when it is, there is not total uniformity on how. For example, some devices are characterized for peak-to-peak noise in a 0.1 to 10Hz bandwidth, while others are specified in terms of wideband rms or peak-to-peak noise over a specified bandwidth. The most useful way to specify noise (as with op-amps) is a plot of noise voltage spectral density (nV/√Hz) versus frequency.

Low noise references are important in high resolution systems to prevent loss of accuracy. Since white noise is statistical, a given noise density must be related to an equivalent peak-to-peak noise in the relevant bandwidth. Strictly speaking, the peak-to-peak noise in a gaussian system is infinite (but its probability is infinitesimal). Conventionally, the figure of 6.6 × rms is used to define a practical peak value - statistically, this occurs less than 0.1% of the time. This peak-to-peak value should be less than 1/2LSB in order to maintain required accuracy. If peak-to-peak noise is assumed to be 6 times the rms value, then for an N-bit system, reference voltage fullscale V_{REF}, reference noise bandwidth (BW), the required noise voltage spectral density E_n (V/√Hz) is given by:

$$E_n \leq \frac{V_{REF}}{12 \cdot 2^N \cdot \sqrt{BW}}.$$

For a 10V, 12-bit, 100kHz system, the noise requirement is a modest 643nV/√Hz. Figure 2.15 shows that increasing resolution and/or lower fullscale references make noise requirements more stringent. The 100kHz bandwidth assumption is somewhat arbitrary, but the user may reduce it with external filtering, thereby reducing the noise. Most good IC references have noise spectral densities around 100nV/√Hz, so additional filtering is obviously required in most high resolution systems, especially those with low values of V_{REF}.

REFERENCE NOISE REQUIREMENTS FOR VARIOUS SYSTEM ACCURACIES (1/2 LSB / 100kHZ CRITERIA)

	NOISE DENSITY (nV/√Hz) FOR 10, 5, AND 2.5V FULLSCALE RANGES		
BITS	**10V**	**5V**	**2.5V**
12	**643**	**322**	**161**
13	**322**	**161**	**80**
14	**161**	**80**	**40**
15	**80**	**40**	**20**
16	**40**	**20**	**10**

Figure 2.15

Some references, for example the AD587 buried zener type have a pin designated as the *noise reduction pin* (see data sheet). This pin is connected to a high impedance node preceding the on-chip buffer amplifier. Thus an externally connected capacitor C_N will form a low pass filter with an internal resistor, to limits the effective noise bandwidth seen at the output. A 1µF capacitor gives a 3 dB bandwidth of 40 Hz. Note that this method of noise reduction is by no means universal, and other devices may implement noise reduction differently, if at all.

There are also general purpose methods of noise reduction, which can be used to reduce the noise of any reference IC, at any standard voltage level. The reference circuit of Figure 2.16 (References 5 and 6) is one such example. This circuit uses external filtering and a precision low-noise op-amp to provide both very low noise and high DC accuracy. Reference U1 is a 2.5, 3.0, 5, or 10V reference with a low noise buffered output. The output of U1 is applied to the R1-C1/C2 noise filter to produce a corner frequency of about 1.7 Hz. Electrolytic capacitors usually imply DC leakage errors, but the bootstrap connection of C1 causes its applied bias voltage to be only the relatively small drop across R2. This lowers the leakage current through R1 to acceptable levels. Since the filter attenuation is modest below a few Hertz, the reference noise still affects overall performance at low frequencies (i.e., <10 Hz).

COMBINING LOW-NOISE AMPLIFIER WITH EXTENSIVE FILTERING YIELDS EXCEPTIONAL REFERENCE NOISE PERFORMANCE (1.5 TO 5nV/√Hz @ 1kHZ)

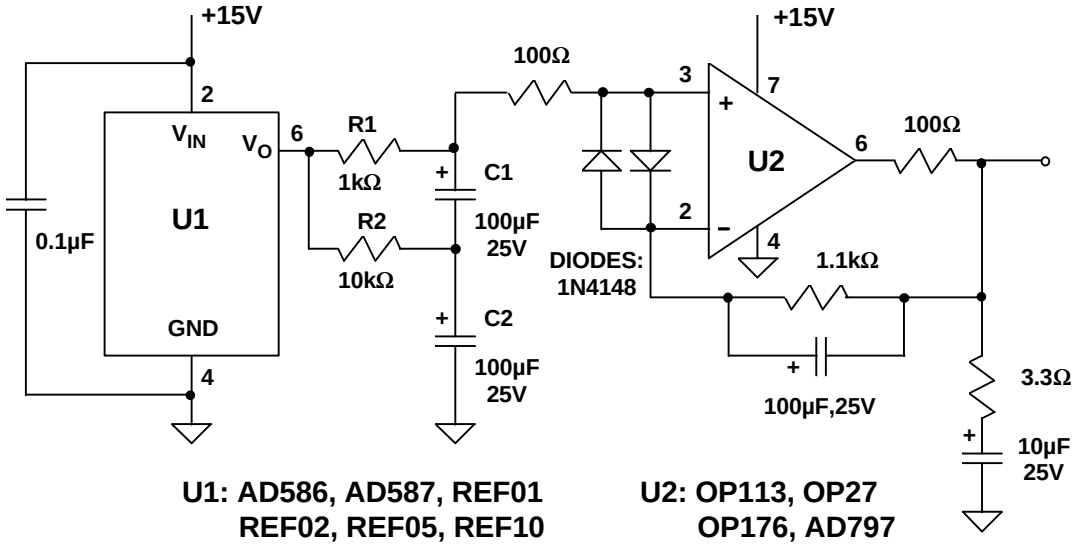

Figure 2.16

The output of the filter is then buffered by a precision low noise unity-gain follower, such as the OP113EP. With less than ±150µV of offset error and under 1µV/°C drift, the buffer amplifier's DC performance will not seriously affect the accuracy/drift of most references. For example, an ADR292E for U1 will have a typical drift of 3ppm/°C, equivalent to 7.5µV/°C, higher than the buffer amplifier. Almost any op amp will have a current limit higher than a typical IC reference. Further, even lower noise op-amps are available for 5-10V use. The AD797 offers 1kHz noise performance less than 2nV/√Hz in this circuit, compared to about 5nV/√Hz for the

OP113. With any amplifier, Kelvin sensing can be used at the load point, a technique which can eliminate I×R related output voltage errors.

SCALED REFERENCES

A useful approach when a non-standard reference voltage is required is to simply buffer and scale a basic low voltage reference diode. With this approach, a potential difficulty is getting an amplifier to work well at such low voltages as 3V. A workhorse solution is the low power reference and scaling buffer shown in Figure 2.17. Here a low current 1.2V two terminal reference diode is used for D1, which can be either a 1.235V AD589, or the 1.225V AD1580. Resistor R1 sets the diode current in either case, and is chosen for 50µA at a minimum supply of 2.7V (a current suitable for either diode). Obviously, loading on the unbuffered diode must be minimized at the V_{REF} node.

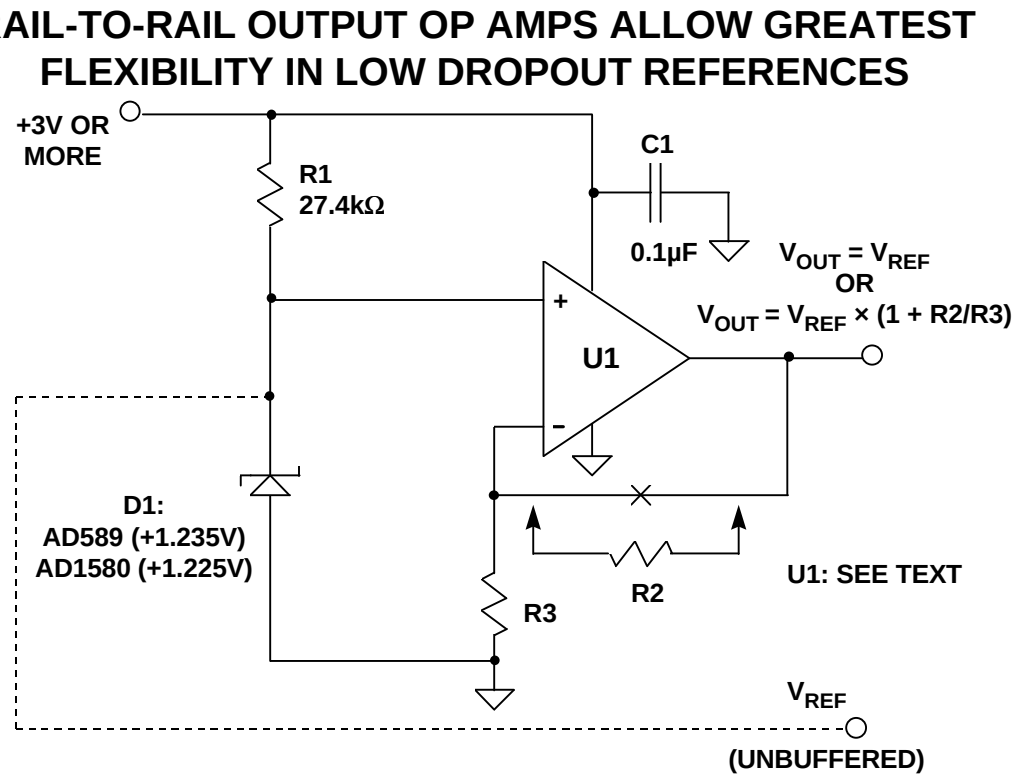

Figure 2.17

The amplifier U1 both buffers and optionally scales up the nominal 1.2V reference, allowing much higher source/sink output currents. Of course, a higher op amp quiescent current is expended in doing this, but this is a basic tradeoff of the approach. Quiescent current is amplifier dependent, ranging from 45µA/channel with the OP196/296/496 series to 1000-2000µA/channel with the OP284 and OP279. The former series is most useful for very light loads (<2mA), while the latter series provide device dependent outputs up to 50mA. Various devices can be used in the circuit as shown, and their key specs are summarized in Figure 2.18.

OP AMPS USEFUL IN LOW VOLTAGE RAIL-RAIL REFERENCES AND REGULATORS

DEVICE*	Iq, mA per channel	Vsat (+) V (min @ mA)	Vsat (–) V (max @ mA)	Isc, mA min
OP181/281/481	0.003	4.93 @ 0.05	0.075 @ 0.05	± 3.5
OP193/293/493	0.017	4.20 @ 1	0.280 @ 1 (typ)	± 8
OP196/296/496	0.045	4.30 @ 1	0.400 @ 1	± 4 (typ)
OP295/495	0.150**	4.50 @ 1	0.110 @ 1	± 11
OP191/291/491	0.300	4.80 @ 2.5	0.075 @ 2.5	± 8.75
AD820/822	0.620	4.89 @ 2	0.055 @ 2	± 15
OP184/284/484	1.250**	4.85 @ 2.5	0.125 @ 2.5	± 7.5
AD8531/32/34	1.400	4.90 @ 10	0.100 @ 10	± 250
OP279	2.000	4.80 @ 10	0.075 @ 10	± 45

*** Typical device specifications @ Vs = +5V, TA = 25°C, unless otherwise noted**
**** Maximum**

Figure 2.18

In Figure 2.17, without gain scaling resistors R2-R3, V_{OUT} is simply equal to V_{REF}. With the use of the scaling resistors, V_{OUT} can be set anywhere between a lower limit of V_{REF}, and an upper limit of the positive rail, due to the op amp's rail-rail output swing. Also, note that this buffered reference is inherently low dropout, allowing a +4.5V (or more) reference output on a +5V supply, for example. The general expression for V_{OUT} is shown in the figure, where V_{REF} is the reference voltage.

Amplifier standby current can be further reduced below 20µA, if an amplifier from the OP181/281/481 or the OP193/293/493 series is used. This choice will be at some expense of current drive, but can provide very low quiescent current if necessary. All devices shown operate from voltages down to 3V (except the OP279, which operates at 5V).

REFERENCE PULSE CURRENT RESPONSE

The response of references to dynamic loads is often a concern, especially in applications such as driving ADCs and DACs. Fast changes in load current invariably perturb the output, often outside the rated error band. For example, the reference input to a sigma-delta ADC may be the switched capacitor circuit shown in Figure 2.19. The dynamic load causes current spikes in the reference as the capacitor C_{IN} is charged and discharged. As a result, noise may be induced on the ADC reference circuitry.

SWITCHED CAPACITOR INPUT OF SIGMA-DELTA ADC PRESENTS A DYNAMIC LOAD TO THE VOLTAGE REFERENCE

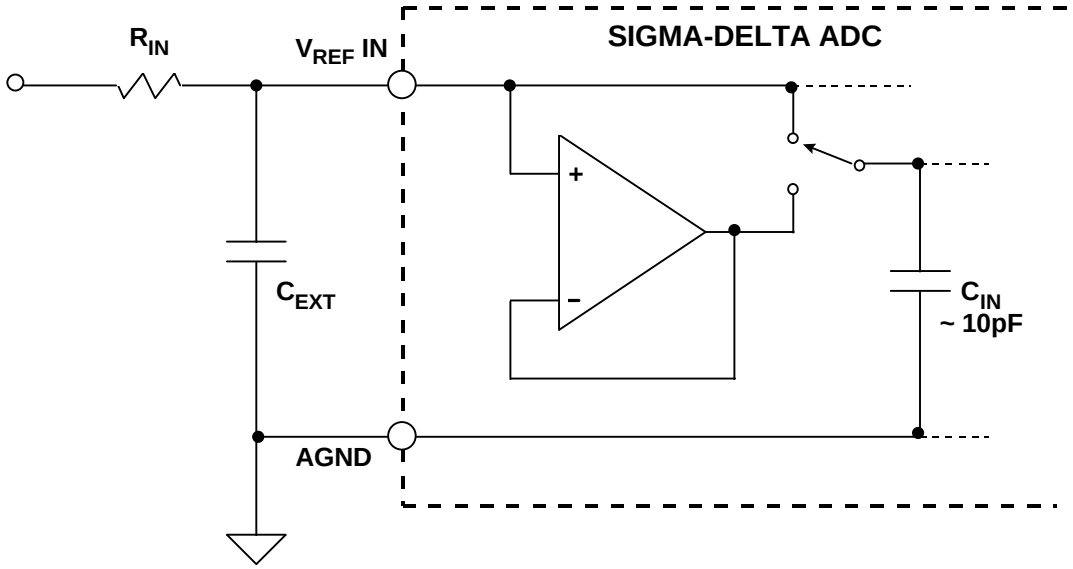

Figure 2.19

Although sigma-delta ADCs have an internal digital filter, transients on the reference input can still cause appreciable conversion errors. Thus it is important to maintain a low noise, transient free potential at the ADC's reference input. Be aware that if the reference source impedance is too high, dynamic loading can cause the reference input to shift by more than 5mV.

A bypass capacitor on the output of a reference may help it to cope with load transients, but many references are unstable with large capacitive loads. Therefore it is quite important to verify that the device chosen will satisfactorily drive the output capacitance required. In any case, the input to references should always be decoupled - with at least 0.1µF, and with an additional 5-50µF if there is any LF ripple on its supply. See Figure 2.12 (again).

Since some references misbehave with transient loads, either by oscillating or by losing accuracy for comparatively long periods, it is advisable to test the pulse response of voltage references which may encounter transient loads. A suitable circuit is shown in Figure 2.20. In a typical voltage reference, a step change of 1mA produces the transients shown. Both the duration of the transient, and the amplitude of the ringing *increase* when a 0.01µF capacitor is connected to the reference output.

MAKE SURE REFERENCE IS STABLE WITH LARGE CAPACITIVE LOADS

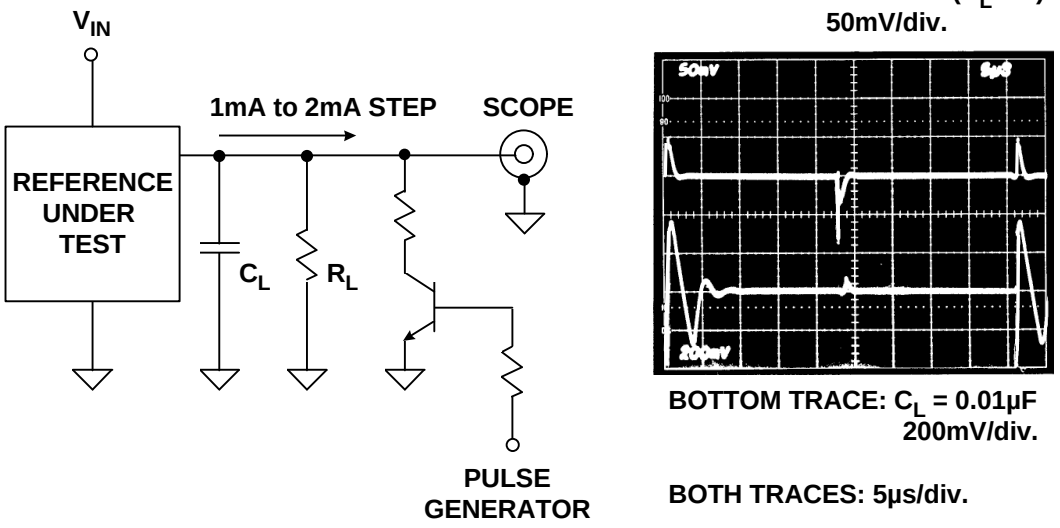

Figure 2.20

Where possible, a reference should be designed to drive large capacitive loads. The AD780 is designed to drive unlimited capacitance without oscillation, it has excellent drift and an accurate output, in addition to relatively low power consumption. Other references which are useful with output capacitors are the REF19X and AD1582-AD1585 series.

As noted above, reference bypass capacitors are useful when driving the reference inputs of successive-approximation ADCs. Figure 2.21 illustrates reference voltage settling behavior immediately following the "Start Convert" command. A small capacitor (0.01µF) does not provide sufficient charge storage to keep the reference voltage stable during conversion, and errors may result. As shown by the bottom trace, decoupling with a ≥1µF capacitor maintains the reference stability during conversion.

Where voltage references are required to drive large capacitances, it is also critically important to realize that their turn-on time will be prolonged. Experiment may be needed to determine the delay before the reference output reaches full accuracy, but it will certainly be much longer than the time specified on the data sheet for the same reference in a low capacitance loaded state.

SUCCESSIVE APPROXIMATION ADCs CAN PRESENT A DYNAMIC TRANSIENT LOAD TO THE REFERENCE

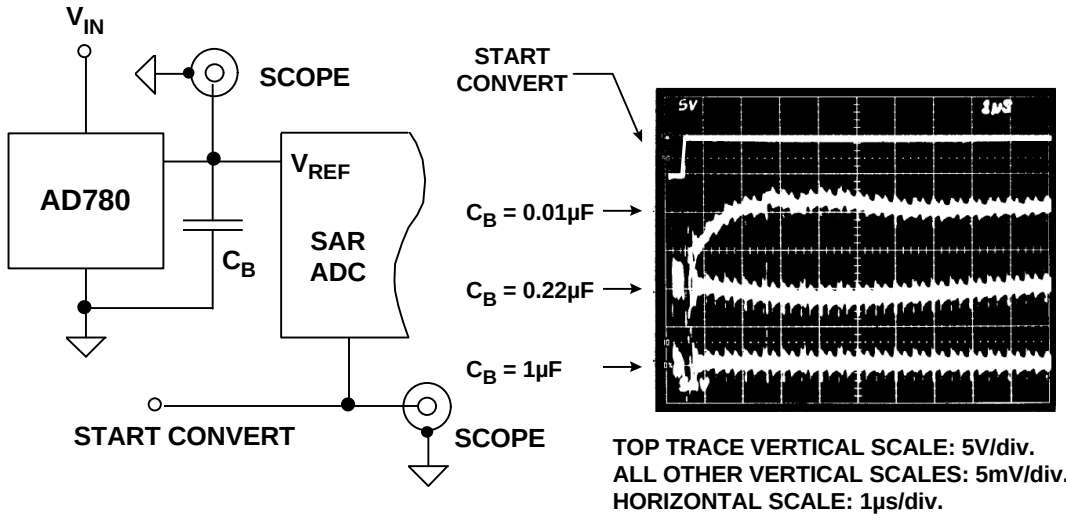

Figure 2.21

LOW NOISE REFERENCES FOR HIGH RESOLUTION CONVERTERS

High resolution converters (both sigma-delta and high speed ones) can benefit from recent improvements in IC references, such as lower noise and the ability to drive capacitive loads. Even though many data converters have internal references, the performance of these references is often compromised because of the limitations of the converter process. In such cases, using an external reference rather than the internal one often yields better overall performance. For example, the AD7710-series of 22-bit ADCs has a 2.5V internal reference with a 0.1 to 10Hz noise of 8.3µV rms (2600nV/√Hz), while the AD780 reference noise is only 0.67µV rms (200nV/√Hz). The internal noise of the AD7710-series in this bandwidth is about 1.7µV rms. The use of the AD780 increases the effective resolution of the AD7710 from about 20.5-bits to 21.5 bits.

Figure 2.22 shows the AD780 used as the reference for the AD7710-series ADCs. The use of the AD780's optional 3V scaling enhances the dynamic range of the ADC, while lowering overall system noise as described above. In addition, the AD780 allows a large decoupling capacitor on its output thereby minimizing conversion errors due to transients.

There is one possible but yet quite real problem when replacing the internal reference of a converter with a higher precision external one. The converter in question may have been trimmed during manufacture to deliver its specified performance with a relatively inaccurate internal reference. In such a case, using a more accurate external reference with the converter may actually introduce additional gain error! For example, the early AD574 had a guaranteed uncalibrated gain accuracy of 0.125% when using an internal 10V reference (which itself had a specified accuracy of only ±1%). It is obvious that if such a device, having an internal

reference which is at one end of the specified range, is used with an external reference of exactly 10V, then its gain will be about 1% in error.

THE AD780 IS IDEAL FOR DRIVING PRECISION SIGMA-DELTA ADCs

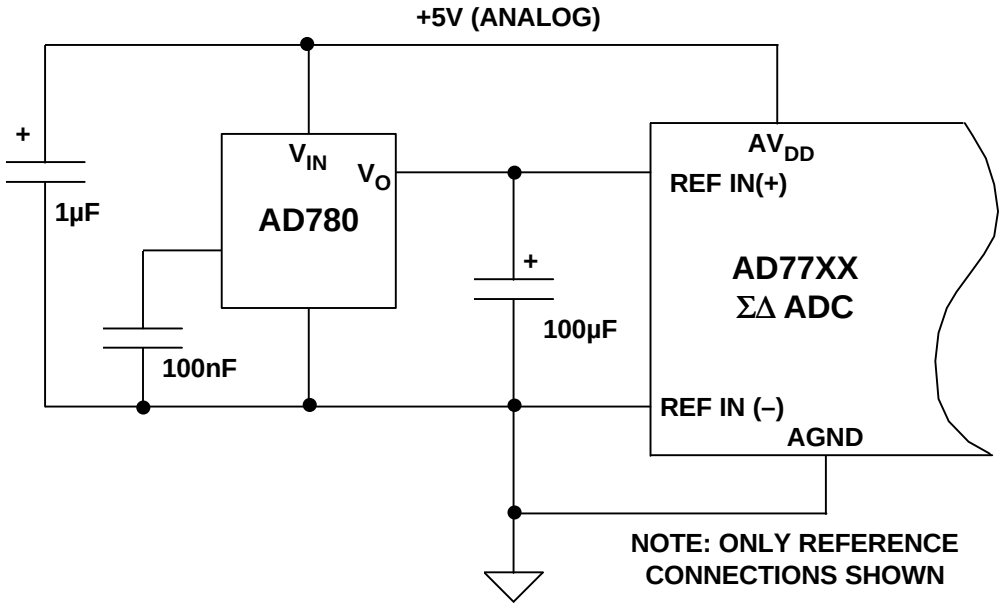

Figure 2.22

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2. Paul Brokaw, *A Simple Three-Terminal IC Bandgap Voltage Reference*, **IEEE Journal of Solid State Circuits**, Vol. SC-9, December, 1974.

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5. Walt Jung, *Build an Ultra-Low-Noise Voltage Reference*, **Electronic Design Analog Applications Issue**, June 24, 1993.

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LOW DROPOUT REGULATORS

Walt Jung

INTRODUCTION

Linear IC voltage regulators have long been standard power system building blocks. After an initial introduction in 5 V logic voltage regulator form, they have since expanded into other standard voltage levels spanning from 3 to 24 V, handling output currents from as low as 100 mA (or less) to as high as 5 A (or more). For several good reasons, linear style IC voltage regulators have been valuable system components since the early days. One reason is the relatively low noise characteristic vis-à-vis the switching type of regulator. Others are a low parts count and overall simplicity compared to discrete solutions. But, because of their power losses, these linear regulators have also been known for being relatively inefficient. Early generation devices (of which many are still available) required 2V or more of unregulated input above the regulated output voltage, making them lossy in power terms.

More recently however, linear IC regulators have been developed with more liberal (i.e., lower) limits on minimum input-output voltage. This voltage, known more commonly as *dropout* voltage, has led to what is termed the Low DropOut regulator, or more popularly, the LDO. Dropout voltage (V_{MIN}) is defined simply as that minimum input-output differential where the regulator undergoes a 2% reduction in output voltage. For example, if a nominal 5.0V LDO output drops to 4.9V (-2%) under conditions of an input-output differential of 0.5V, by this definition the LDO's V_{MIN} is 0.5V.

As will be shown in this section, dropout voltage is extremely critical to a linear regulator stage's power efficiency. The lower the voltage allowable across a regulator while still maintaining a regulated output, the less power the regulator dissipates as a result. A low regulator dropout voltage is the key to this, as it takes this lower dropout to maintain regulation as the input voltage lowers. In performance terms, the bottom line for LDOs is simply that more useful power is delivered to the load and less heat is generated in the regulator. LDOs are key elements of power systems that must provide stable voltages from batteries, such as portable computers, cellular phones, etc. This is simply because they maintain their regulated output down to lower points on the battery's discharge curve. Or, within classic mains-powered raw DC supplies, LDOs allow lower transformer secondary voltages, reducing system susceptibility to shutdown under brownout conditions as well as allowing cooler operation.

LINEAR VOLTAGE REGULATOR BASICS

A brief review of three terminal linear IC regulator fundamentals is necessary to understanding the LDO variety. As it turns out, almost all LDOs available today, as well as many of the more general three terminal regulator types, are *positive leg, series style* regulators. This simply means that they control the regulated voltage

output by means of a pass element which is in series with the positive side of unregulated input.

This is shown more clearly in Figure 2.23, which is a hookup diagram for a hypothetical three terminal style regulator. To re-iterate what was said earlier in the chapter about reference ICs, in terms of their basic functionality, many standard voltage regulator ICs are available in the series three-terminal form as is shown here (V_{IN}, GND or Common, V_{OUT}).

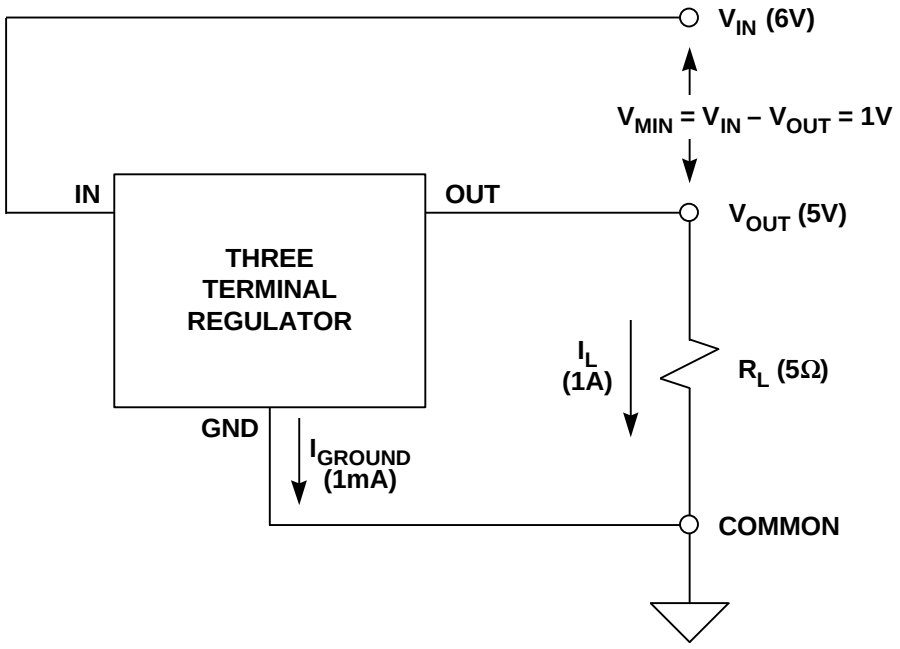


Figure 2.23

This diagram also allows some statements to be made about power losses in the regulator. There are two components to power which are dissipated in the regulator, one a function of $V_{IN} - V_{OUT}$ and I_L, plus a second which is a function of V_{IN} and Iground. If we call the total power P_D, this then becomes:

$$P_D = (V_{IN} - V_{OUT})(I_L) + (V_{IN})(\text{Iground}).$$

Obviously, the magnitude of the load current and the regulator dropout voltage both greatly influence the power dissipated. However, it is also easy to see that for a given I_L, as the dropout voltage is lowered, the first term of P_D is reduced. With an intermediate dropout voltage rating of 1V, a 1A load current will produce 1W of heat in this regulator, which may require a heat sink for continuous operation. It is this first term of the regulator power which usually predominates, at least for loaded regulator conditions.

The second term, being proportional to Iground (typically only 1-2 mA, sometimes even less) usually only becomes significant when the regulator is unloaded, and the regulator's quiescent or standby power then produces a constant drain on the source V_{IN}.

However, it should be noted that in some types of regulators (notably those which have very low β pass devices such as lateral PNP transistors) the Iground current under load can actually run quite high. This effect is worst at the onset of regulation, or when the pass device is in saturation, and can be noted by a sudden Iground current "spike", where the current jumps upward abruptly from a lower low level. All LDO regulators using bipolar transistor pass devices which can be saturated (such as PNPs) can show this effect. It is much less severe in PNP regulators using vertical PNPs (since these have a higher intrinsic β) and doesn't exist to any major extent in PMOS LDOs (since PMOS transistors are controlled by voltage level, not current).

In the example shown, the regulator delivers 5V × 1A, or 5W to the load. With a dropout voltage of 1V, the input power is 6V times the same 1A, or 6W. In terms of power efficiency, this can be calculated as:

$$P_{EFF(\%)} = 100 \times \frac{P_{OUT}}{P_{IN}},$$

where P_{OUT} and P_{IN} are the total output and input powers, respectively.

In these sample calculations, the relatively small portion of power related to Iground will be ignored for simplicity, since this power is relatively small. In an actual design, this simplifying step may not be justified.

In the case shown, the efficiency would be 100 × 5/6, or about 83%. But by contrast, if an LDO were to be used with a dropout voltage of 0.1V instead of 1V, the input voltage can then be allowed to go as low as 5.1V. The new efficiency for this condition then becomes 100 × 5/5.1, or 98%. It is obvious that an LDO can potentially greatly enhance the power efficiency of linear voltage regulator systems.

A more detailed look within a typical regulator block diagram reveals a variety of elements, as is shown in Figure 2.24.

In this diagram virtually all of the elements shown can be considered to be fundamentally necessary, the exceptions being the shutdown control and saturation sensor functions (shown dotted). While these are present on many current regulators, the shutdown feature is relatively new as a standard function, and certainly isn't part of standard three-terminal regulators. When present, shutdown control is a logic level controllable input, whereby a digital HIGH (or LO) is defined as regulation active (or vice-versa). The error output, $\overline{ERR}$, is useful within a system to detect regulator overload, such as saturation of the pass device, thermal overload, etc. The remaining functions shown are always part of an IC power regulator.

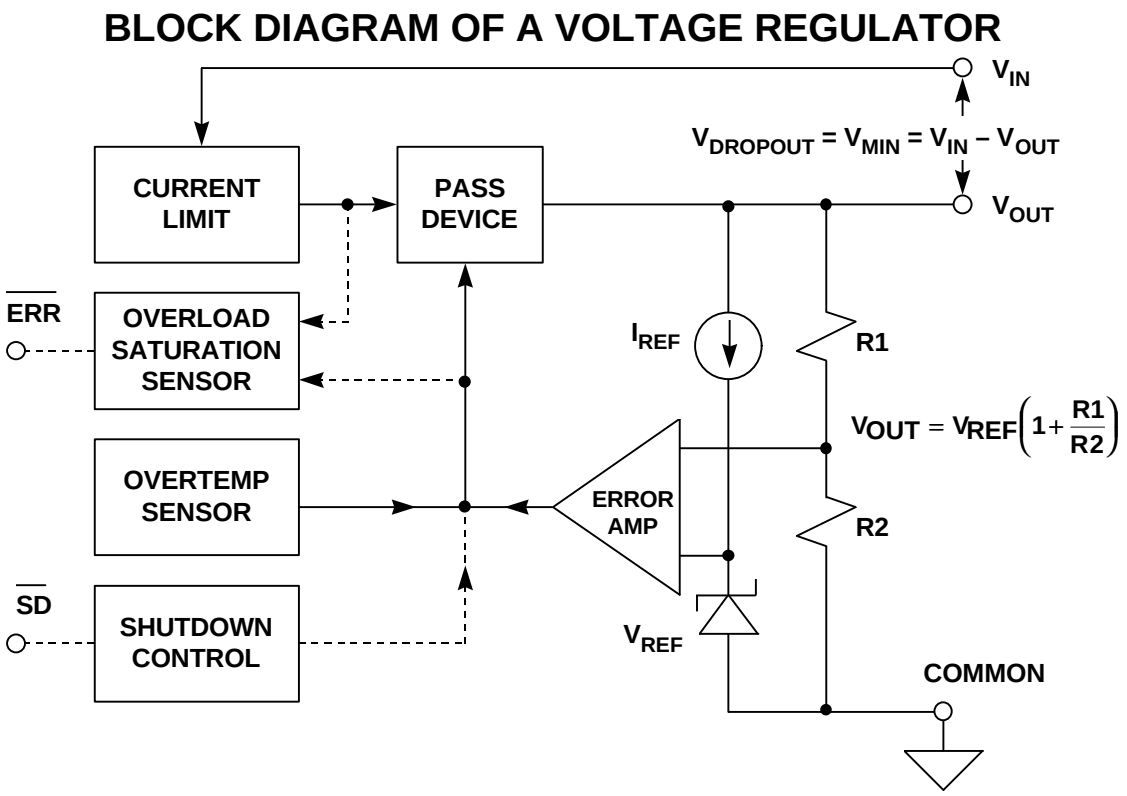


Figure 2.24

In operation, a voltage reference block produces a stable voltage V_{REF}, which is almost always a bandgap based voltage, typically ~1.2V, which allows output voltages of 3V or more from supplies as low as 5V. This voltage is presented to one input of an error amplifier, with the other input connected to the V_{OUT} sensing divider, R1-R2. The error amplifier drives the pass device, which in turn controls the output. The resulting regulated voltage is then simply:

$$V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right).$$

With a typical bandgap reference voltage of 1.2V, the R1/R2 ratio will be approximately 3/1 for a 5V output. When standby power is critical, several design steps will be taken. The resistor values of the divider will be high, the error amplifier and pass device driver will be low power, and the reference current I_{REF} will also be low. By these means the regulator's unloaded standby current can be reduced to a mA or less using bipolar technology, and to only a few μA in CMOS parts. In regulators which offer a shutdown mode, the shutdown state standby current will be reduced to a μA or less.

Nearly all regulators will have some means of current limiting and over temperature sensing, to protect the pass device against failure. Current limiting is usually by a series sensing resistor for high current parts, or alternately by a more simple drive current limit to a controlled β pass device (which achieves the same end). For higher voltage circuits, this current limiting may also be combined with voltage limiting, to

provide complete load line control for the pass device. All power regulator devices will also have some means of sensing over-temperature, usually by means of a fixed reference voltage and a V_{BE}-based sensor monitoring chip temperature. When the die temperature exceeds a dangerous level (above ~150°C), this can be used to shutdown the chip, by removing the drive to the pass device. In some cases an error flag output may be provided to warn of this shutdown (and also loss of regulation from other sources).

PASS DEVICES AND THEIR ASSOCIATED TRADEOFFS

The discussion thus far has not treated the pass device in any detail. In practice, this major part of the regulator can actually take on quite a number of alternate forms. Precisely which type of pass device is chosen has a major influence on almost all major regulator performance issues. Most notable among these is the dropout voltage, V_{MIN}.

Figure 2.25a through 2.25e illustrates a number of pass devices which are useful within voltage regulator circuits, shown in simple schematic form. On the figure is also listed the salient V_{MIN} for the device as it would typically be used, which directly indicates its utility for use in an LDO. Not shown in these various mini-figures are the remaining circuits of a regulator.

It is difficult to fully compare all of the devices from their schematic representations, since they differ in so many ways beyond their applicable dropout voltages. For this reason, the chart of Figure 2.26 is useful.

This chart compares the various pass elements in greater detail, allowing easy comparison between the device types, dependent upon which criteria is most important. Note that columns A-E correspond to the schematics of Figure 2.25a-2.25e. Note also that the pro/con comparison items are in *relative* terms, as opposed to a hard specification limit for any particular pass device type.

For example, it can be seen that the all NPN pass devices of columns A and B have the attributes of a follower circuit, which allows high bandwidth and provides relative immunity to cap loading because of the characteristic low Z_{OUT}. However, neither the single NPN nor the Darlington NPN can achieve low dropout, for any load current. This is because the V_{BE}(s) of the pass device appears in series with the input, preventing its saturation, and thus setting a V_{MIN} of about 1 or 2V.

By contrast, the inverting mode device connections of both columns C and E do allow the pass device to be effectively saturated, which lowers the associated voltage losses to a minimum. This single factor makes these two pass device types optimum for LDO use, at least in terms of power efficiency.

PASS DEVICES USEFUL IN VOLTAGE REGULATORS

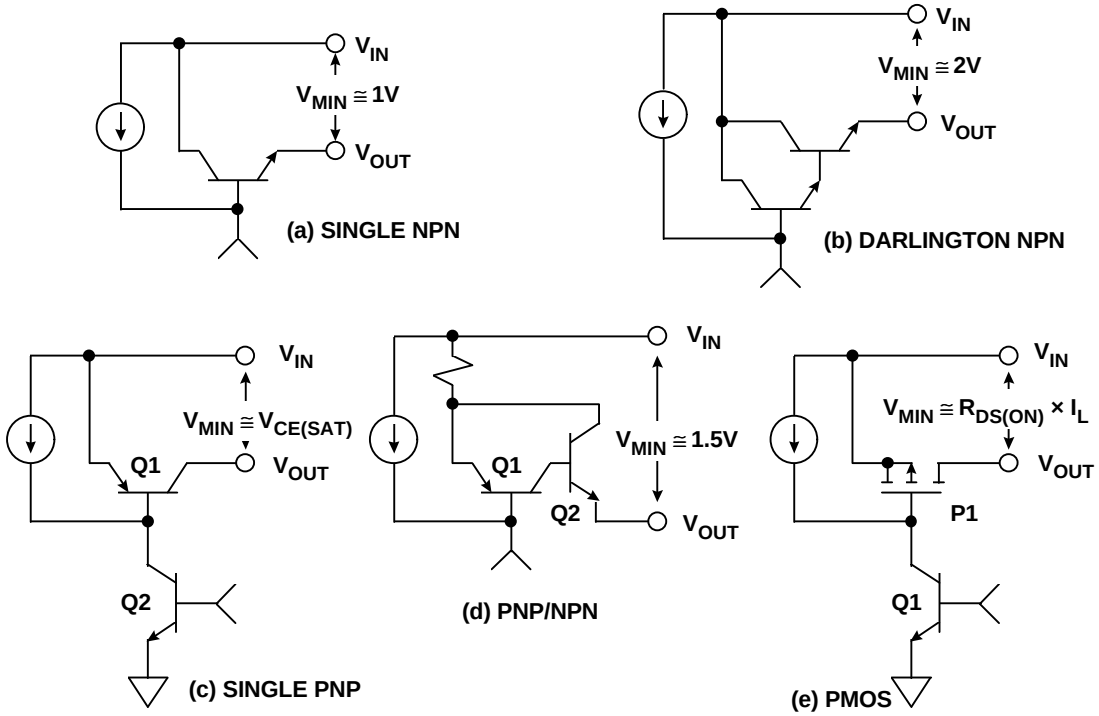


Figure 2.25

PROS AND CONS OF VOLTAGE REGULATOR PASS DEVICES

A SINGLE NPN	B DARLINGTON NPN	C SINGLE PNP	D PNP/NPN	E PMOS
V_{MIN} ~ 1V	V_{MIN} ~ 2V	V_{MIN} ~ 0.1V	V_{MIN} ~ 1.5V	$V_{MIN} \sim R_{DS(ON)} \times I_L$
I_L < 1A	I_L > 1A	I_L < 1A	I_L > 1A	I_L > 1A
Follower	Follower	Inverter	Inverter	Inverter
Low Z_{OUT}	Low Z_{OUT}	High Z_{OUT}	High Z_{OUT}	High Z_{OUT}
Wide BW	Wide BW	Narrow BW	Narrow BW	Narrow BW
C_L Immune	C_L Immune	C_L Sensitive	C_L Sensitive	C_L Sensitive

Figure 2.26

For currents below 1A, either a single PNP or a PMOS pass device is most useful for low dropout, and they both can achieve a V_{MIN} of 0.1V or less at currents of 100mA. The dropout voltage of a PNP will be highly dependent upon the actual device used and the operating current, with vertical PNP devices being superior for saturation losses, as well as minimizing the Iground spike when in saturation. PMOS pass devices offer the potential for the lowest possible V_{MIN}, since the actual dropout voltage will be the product of the device $R_{DS(ON)}$ and I_L. Thus a low $R_{DS(ON)}$ PMOS device can always be chosen to minimize V_{MIN} for a given I_L. PMOS pass devices are typically *external* to the LDO IC, making the IC actually a controller (as opposed to a complete and integral LDO). PMOS pass devices can allow currents up to several amps or more with very low dropout voltages. The PNP/NPN connection of column D is actually a hybrid hookup, intended to boost the current of a single PNP pass device. This it does, but it also adds the V_{BE} of the NPN in series (which cannot be saturated), making the net V_{MIN} of the connection about 1.5V.

All of the three connections C/D/E have the characteristic of high output impedance, and require an output capacitor for stability. The fact that the output cap is part of the regulator frequency compensation is a most basic application point, and one which needs to be clearly understood by the regulator user. This factor, denoted by "C_L sensitive", makes regulators using them generally critical as to the exact C_L value, as well as its ESR (equivalent series resistance). Typically this type of regulator must be used only with a specific size as well as type of output capacitor, where the ESR is controlled with respect to both time and temperature to fully guarantee regulator stability. Fortunately, some recent Analog Devices LDO IC circuit developments have eased this burden on the part of the regulator user a great deal, and will be discussed below in further detail.

Some examples of standard IC regulator architectures illustrate the points above regarding pass devices, and allow an appreciation of regulator developments leading up to more recent LDO technologies.

The classic LM309 5V/1A three-terminal regulator (see Reference 1) was the originator in a long procession of regulators. This circuit is shown in much simplified form in Figure 2.27, with current limiting and over temperature details omitted. This IC type is still in standard production today, not just in original form, but in family derivatives such as the 7805, 7815 etc., and their various low and medium current alternates. Using a Darlington pass connection for Q18-Q19, the design has never been known for low dropout characteristics (~1.5V typical), or for low quiescent current (~5mA). It is however relatively immune to instability issues, due to the internal compensation of C1, and the buffering of the emitter follower output. This helps make it easy to apply.

The LM109/309 bandgap voltage reference actually used in this circuit consists of a more involved scheme, as opposed to the basic form which was described with Figure 2.3. Resistor R8 drops a PTAT voltage, which drives the Darlington connected error amplifier, Q9-Q10. The negative TC V_{BE}s of Q9-Q10 and Q12-Q13 are summed with this PTAT voltage, and this sum produces a temperature-stable 5V output voltage. Current buffering of the error amplifier Q10 is provided by PNP Q11, which drives the NPN pass devices.

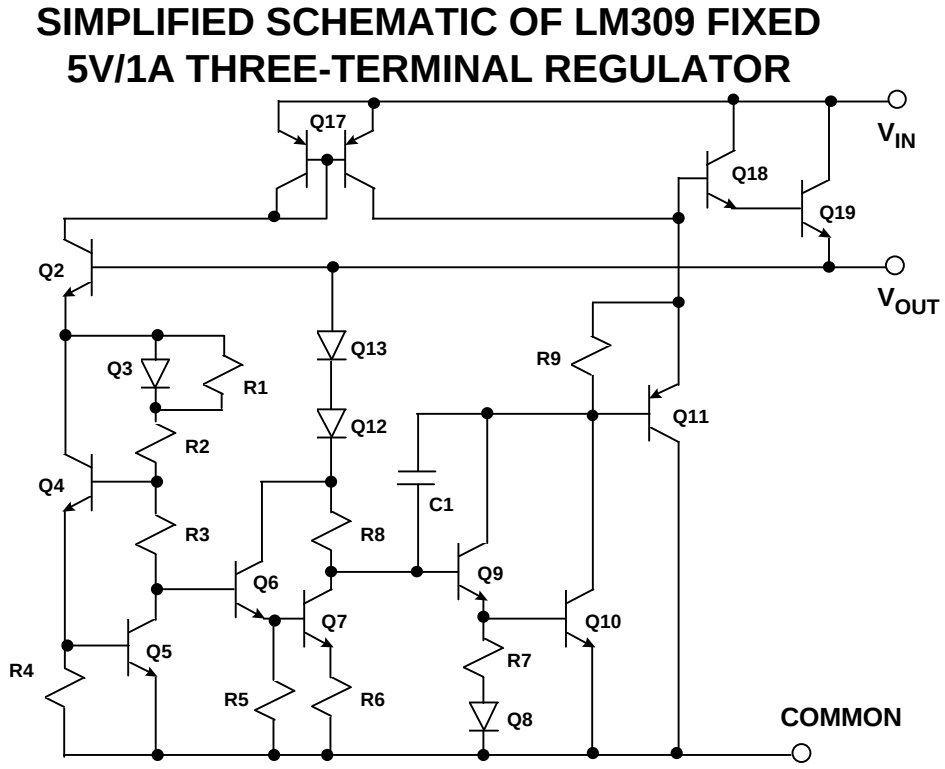


Figure 2.27

Later developments in references and three-terminal regulation techniques led to the development of the voltage adjustable regulator. The original IC to employ this concept was the LM317 (see Reference 2), which is shown in simplified schematic form in Figure 2.28. Note that this design does not use the same ΔV_{BE} form of reference as in the LM309. Instead, Q17-Q19, etc. are employed as a form of a Brokaw bandgap reference cell (see Figure 2.4 again, and Reference 3).

This adjustable regulator bootstraps the reference cell transistors Q17-Q19 and the error amplifier transistors Q16-Q18. The output of the error amplifier drives Darlington pass transistors Q25-Q26, through buffer Q12. The basic reference cell produces a fixed voltage of 1.25V, which appears between the V_{OUT} and ADJ pins of the IC as shown. External scaling resistors R1 and R2 set up the desired output voltage, which is:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + 50\mu A \times R2 .$$

SIMPLIFIED SCHEMATIC OF LM317 ADJUSTABLE THREE-TERMINAL REGULATOR

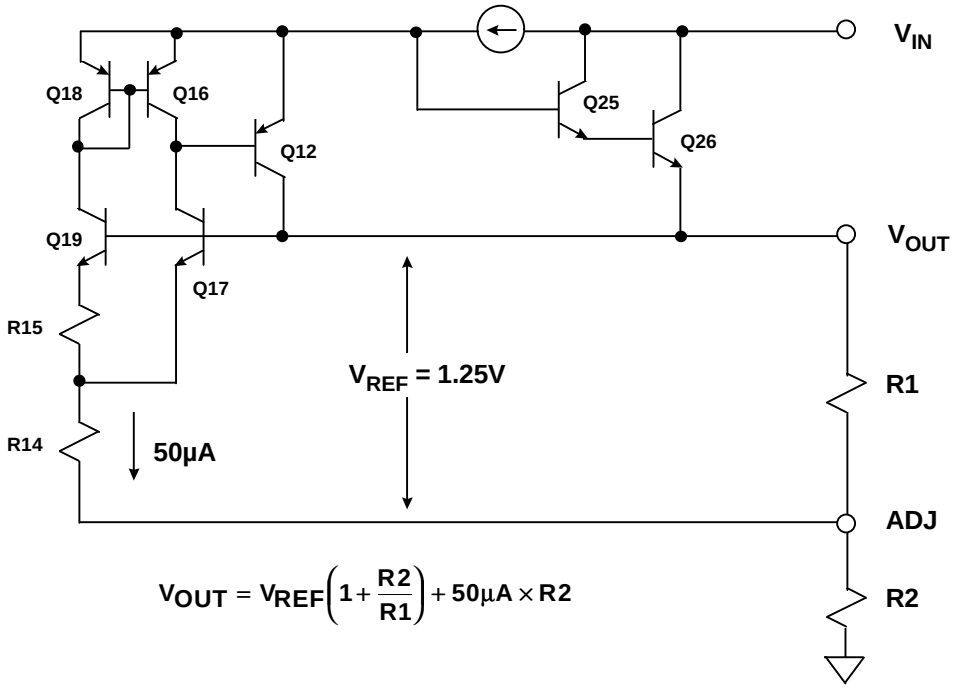


Figure 2.28

As can be noted, the voltage output is a scaling of V_{REF} by R2-R1, plus a small voltage component which is a function of the 50µA reference cell current. Typically, the R1-R2 values are chosen to draw >5mA, making the rightmost term relatively small by comparison. The design is internally compensated, and in many applications will not necessarily need an output bypass capacitor.

Like the LM309 fixed voltage regulator, the LM317 series has relatively high dropout voltage, due to the use of Darlington pass transistors. It is also not a low power IC (quiescent current typically 3.5mA). The strength of this regulator lies in the wide range of user voltage adaptability it allows.

Subsequent variations on the LM317 pass device topology modified the method of output drive, substituting a PNP/NPN cascade for the LM317's Darlington NPN pass devices. This development achieves a lower V_{MIN}, 1.5V or less (see Reference 4). The modification also allows all of the general voltage programmability of the basic LM317, but at some potential increase in application sensitivity to output capacitance. This sensitivity is brought about by the fundamental requirement for an output capacitor for the IC's frequency compensation, which is a differentiation from the original LM317.

LOW DROPOUT REGULATOR ARCHITECTURES

As has been shown thus far, all LDO pass devices have the fundamental characteristics of operating in an inverting mode. This allows the regulator circuit to

achieve pass device saturation, and thus low dropout. A by-product of this mode of operation is that this type of topology will necessarily be more susceptible to stability issues. These basic points give rise to some of the more difficult issues with regard to LDO performance. In fact, these points influence both the design and the application of LDOs to a very large degree, and in the end, determine how they are differentiated in the performance arena.

A traditional LDO architecture is shown in Figure 2.29, and is generally representative of actual parts employing either a PNP pass device as shown, or alternately, a PMOS device. There are both DC and AC design and application issues to be resolved with this architecture, which are now discussed.

TRADITIONAL LDO ARCHITECTURE

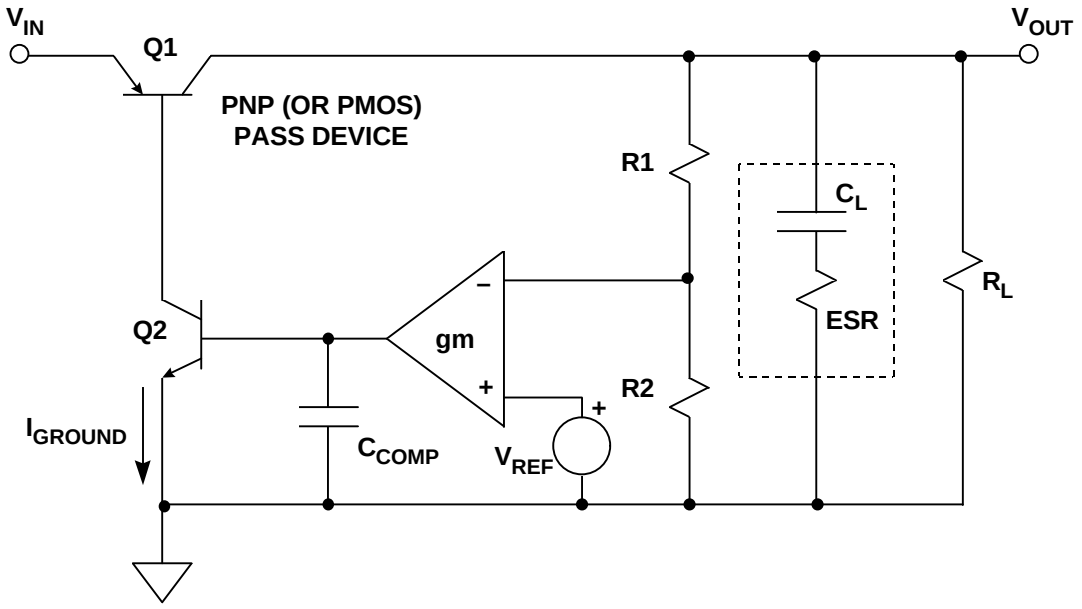


Figure 2.29

In DC terms, perhaps the major issue is the type of pass device used, which influences dropout voltage and ground current. If a lateral PNP device is used for Q1, the β will be low, sometimes only on the order or 10 or so. Since Q1 is driven from the collector of Q2, the relatively high base current demanded by a lateral PNP results in relatively high emitter current in Q2, or a high Iground. For a typical lateral PNP based regulator operating with a 5V/150mA output, Iground will be typically ~18mA, and can be as high as 40mA. To compound the problem of high Iground in PNP LDOs, there is also the "spike" in Iground, as the regulator is operating within its dropout region. Under such conditions, the output voltage is out of tolerance, and the regulation loop forces higher drive to the pass device, in an attempt to maintain loop regulation. This results in a substantial spike upward in Iground, which is typically internally limited by the regulator's saturation control circuits.

PMOS pass devices do not demonstrate a similar current spike in Iground, since they are voltage controlled. But, while devoid of the Iground spike, PMOS pass

devices do have some problems of their own. Problem number one is that high quality, low R_{ON}, low threshold PMOS devices generally aren't compatible with many IC processes. This makes the best technical choice for a PMOS pass device an external part, driven from the collector of Q2 in the figure. This introduces the term "LDO controller", where the LDO architecture is completed by an external pass device. While in theory NMOS pass devices would offer lower R_{ON} choice options, they also demand a boosted voltage supply to turn on, making them impractical for a simple LDO. PMOS pass devices are widely available in low both R_{ON} and low threshold forms, with current levels up to several amperes. They offer the potential of the lowest dropout of any device, since dropout can always be lowered by picking a lower R_{ON} part.

The dropout voltage of lateral PNP pass devices is reasonably good, typically around 300mV at 150mA, with a maximum of 600mV. These levels are however considerably bettered in regulators using vertical PNPs, which have a typical β of ~150 at currents of 200mA. This leads directly to an Iground of 1.5mA at the 200mA output current. The dropout voltage of vertical PNPs is also an improvement vis-à-vis that of the lateral PNP regulator, and is typically 180mV at 200mA, with a maximum of 400mV.

There are also major AC performance issues to be dealt with in the LDO architecture of Fig. 2.29. This topology has an inherently high output impedance, due to the operation of the PNP pass device in a common-emitter (or common-source with a PMOS device) mode. In either case, this factor causes the regulator to appear as a high source impedance to the load.

The internal compensation capacitor of the regulator, C_{COMP}, forms a fixed frequency pole, in conjunction with the g_m of the error amplifier. In addition, load capacitance C_L forms an output pole, in conjunction with R_L. This particular pole, because it is a second (and sometimes variable) pole of a two-pole system, is the source of a major LDO application problem. The C_L pole can strongly influence the overall frequency response of the regulator, in ways that are both useful as well as detrimental. Depending upon the relative positioning of the two poles in the frequency domain, along with the relative value of the ESR of capacitor C_L, it is quite possible that the stability of the system can be compromised for certain combinations of C_L and ESR. Note that C_L is shown here as a real capacitor, which is actually composed of a pure capacitance plus the series parasitic resistance ESR.

Without a heavy duty exercise into closed-loop stability analysis, it can safely be said that LDOs, like other feedback systems, need to satisfy certain basic stability criteria. One of these is the gain-versus-frequency rate-of-change characteristic in the region approaching the system's unity loop gain crossover point. For the system to be closed loop stable, the phase shift must be less than 180° at the point of unity gain. In practice, a good feedback design needs to have some phase margin, generally 45° or more to allow for various parasitic effects. While a single pole system is intrinsically stable, two pole systems are *not* necessarily so—they may in fact be stable, or they may also be unstable. Whether or not they are stable for a given instance is highly dependent upon the specifics of their gain-phase characteristics.

If the two poles of such a system are widely separated in terms of frequency, stability may not be a serious problem. The emitter-follower output of a classic regulator like the LM309 is an example with widely separated pole frequencies, as the very low Z_{OUT} of the NPN follower pushes the output pole due to load capacitance far out in frequency, where it does little harm. The internal compensation capacitance (C1 of Fig. 2.27, again) then forms part of a *dominant pole*, which reduces loop gain to below unity at the much higher frequencies where the output pole does occur. Thus stability is not necessarily compromised by load capacitance in this type of regulator.

Figure 2.30 summarizes the various DC and AC design issues of LDOs.

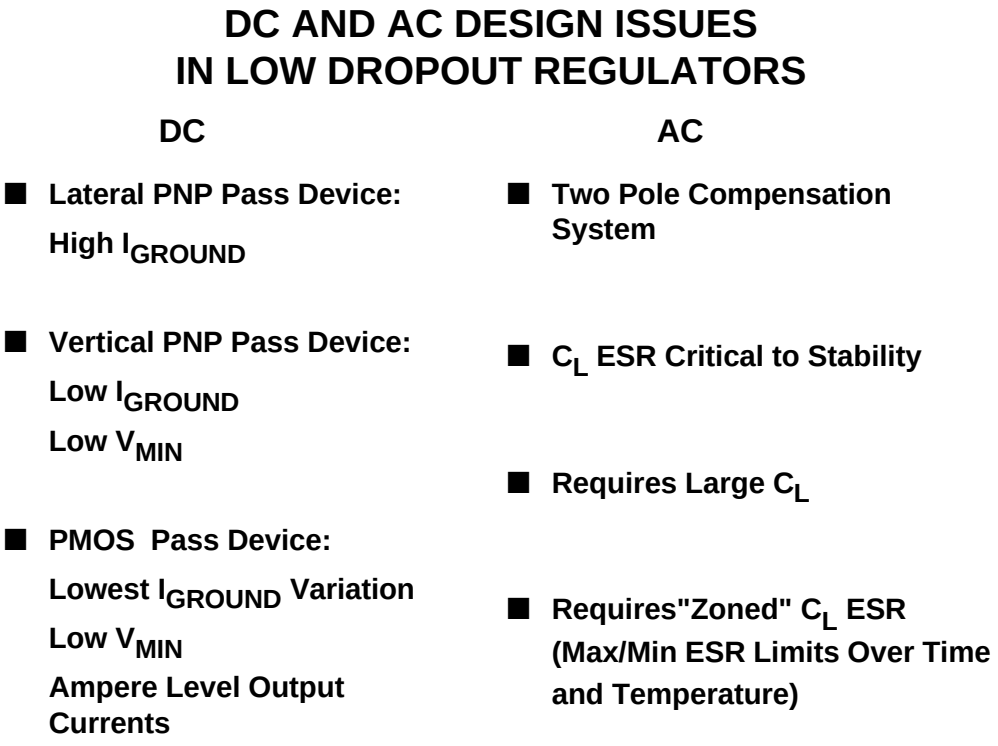


Figure 2.30

By their nature however, LDOs simply can't afford the luxury of emitter follower outputs, they must instead operate with pass devices capable of saturation. Thus, given the existence of two or more poles (one or more internal and a second formed by external loading) there is the potential for the cumulative gain-phase to add in a less than satisfactory manner. The potential for instability under certain output loading conditions is, for better or worse, a fact-of-life for most LDO topologies.

However, the output capacitor which gives rise to the instability can, for certain circumstances, also be the solution to the same instability. This seemingly paradoxical situation can be appreciated by realizing that almost all practical capacitors are actually as shown in Fig. 2.29, a series combination of the capacitance C_L and a parasitic resistance, ESR. While load resistance R_L and C_L do form a pole, C_L and its ESR also form a zero. The effect of the zero is to mitigate the de-stabilizing effect of C_L for certain conditions. For example, if the pole and zero in

question are appropriately placed in frequency relative to the internal regulator poles, some of the deleterious effects can be made to essentially cancel, leaving little or no problematic instability (see Reference 5). The basic problem with this setup is simply that the capacitor's ESR, being a parasitic term, is not at all well controlled. As a result, LDOs which depend upon output pole-zero compensation schemes must very carefully limit the capacitor ESR to certain *zones*, such as shown by Figure 2.31.

ZONED LOAD CAPACITOR ESR CAN MAKE AN LDO APPLICATIONS NIGHTMARE

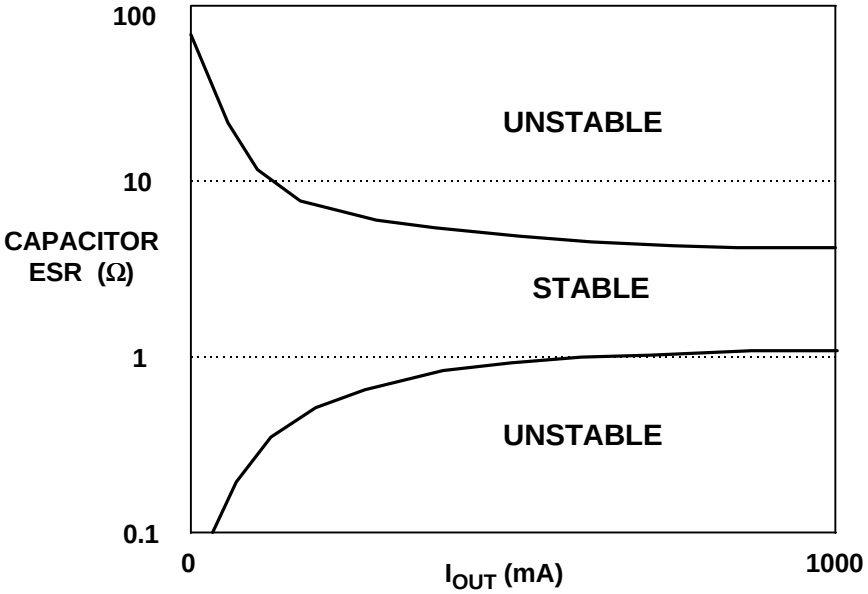


Figure 2.31

A zoned ESR chart such as this is meant to guide the user of an LDO in picking an output capacitor which confines ESR to the stable region, i.e., the central zone, for all operating conditions. Note that this generic chart is not intended to portray any specific device, just the general pattern. Unfortunately, capacitor facts of life make such data somewhat limited in terms of the real help it provides. Bearing in mind the requirements of such a zoned chart, it effectively means that general purpose aluminum electrolytic are prohibited from use, since they deteriorate in terms of ESR at cold temperatures. Very low ESR types such as OS-CON or multi-layer ceramic units have ESRs which are too low for use. While they could in theory be padded up into the stable zone with external resistance, this would hardly be a practical solution. This leaves tantalum types as the best all around choice for LDO output use. Finally, since a large capacitor value is likely to be used to maximize stability, this effectively means that the solution for an LDO such as Fig. 2.29 must use a more expensive and physically large tantalum capacitor. This is not desirable if small size is a major design criteria.

THE anyCAP™ LOW DROPOUT REGULATOR FAMILY

Some novel modifications to the basic LDO architecture of Fig. 2.29 allow major improvements in terms of both DC and AC performance. These developments are shown schematically in Figure 2.32, which is a simplified diagram of the Analog Devices ADP330X series LDO regulator family. These regulators are also known as the anyCAP™ family, so named for their relative insensitivity to the output capacitor in terms of both size and ESR. They are available in power efficient packages such as the Thermal Coastline (discussed below), in both stand-alone LDO and LDO controller forms, and also in a wide span of output voltage options.

ADP330X anyCAP™ TOPOLOGY FEATURES IMPROVED DC & AC PERFORMANCE OVER TRADITIONAL LDOs

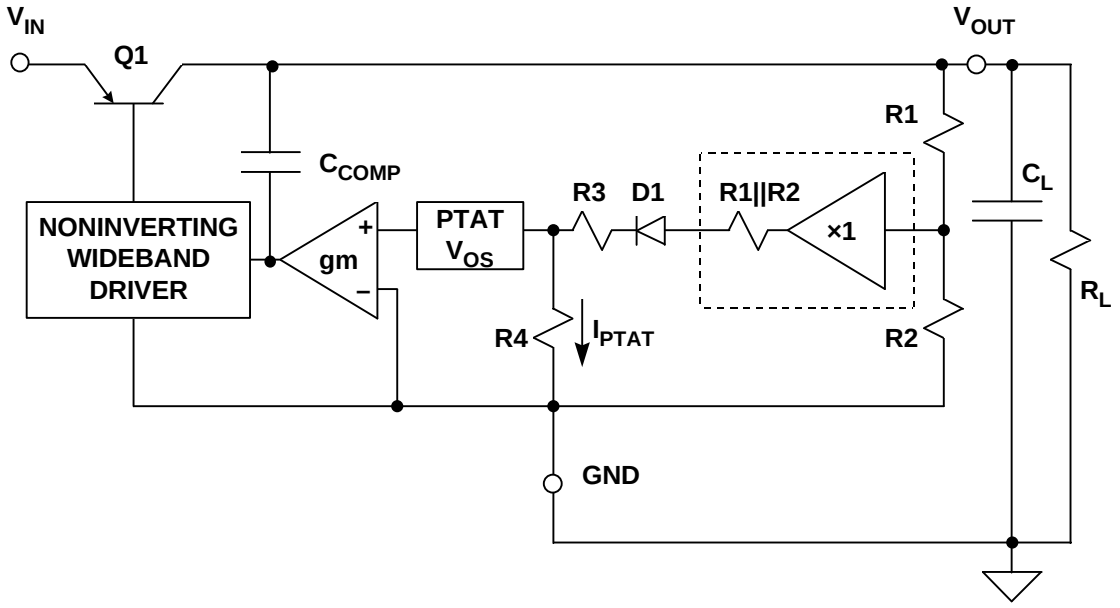


Figure 2.32

Design Features Related to DC Performance

One of the key differences in the ADP330X series is the use of a high gain vertical PNP pass device, with all of the advantages described above with Figs. 2.29 and 2.30 (also, see Reference 6). This allows the typical dropout voltages for the series to be on the order of 1mV/mA for currents of 200mA or less.

It is important to note that the topology of this LDO is distinctly different from that of the generic form in Fig. 2.29, as there is no obvious V_{REF} block. The reason for this is the fact that the ADP330X series uses what is termed a “merged” amplifier-reference design. The operation of the integral amplifier and reference scheme illustrated in Fig. 2.32 can be described as follows.

In this circuit, V_{REF} is defined as a reference voltage existing at the output of a zero impedance divider of ratio R1/R2. In the figure, this is depicted symbolically by the (dotted) unity gain buffer amplifier fed by R1/R2, which has an output of V_{REF}. This reference voltage feeds into a series connection of (dotted) R1||R2, then actual components D1, R3, R4, etc.

The error amplifier, shown here as a gm stage, is actually a PNP input differential stage with the two transistors of the pair operated at different current densities, so as to produce a predictable PTAT offset voltage. Although shown here as a separate block V_{OS}, this offset voltage is inherent to a bipolar pair for such operating conditions. The PTAT V_{OS} causes a current I_{PTAT} to flow in R4, which is simply:

$$I_{PTAT} = \frac{V_{OS}}{R4}.$$

Note that this current also flows in series connected R4, R3, and the Thevenin resistance of the divider, R1||R2, so:

$$V_{PTAT} = I_{PTAT}\left(R3 + R4 + R1||R2\right).$$

The *total* voltage defined as V_{REF} is the sum of two component voltages:

$$V_{REF} = V_{PTAT} + V_{D1},$$

where the I_{PTAT} scaled voltages across R3, R4, and R1||R2 produce a net PTAT voltage V_{PTAT}, and the diode voltage V_{D1} is a CTAT voltage. As in a standard bandgap reference, the PTAT and CTAT components add up to a temperature stable reference voltage of 1.25V. In this case however, the reference voltage is not directly accessible, but instead it exists in the virtual form described above. It acts as it would be seen at the output of a zero impedance divider of a numeric ratio of R1/R2, which is then fed into the R3-D1 series string through a Thevenin resistance of R1||R2 in series with D1.

With the closed loop regulator at equilibrium, the voltage at the virtual reference node will be:

$$V_{REF} = V_{OUT}\left(\frac{R2}{R1 + R2}\right).$$

With minor re-arrangement, this can be put into the standard form to describe the regulator output voltage, as:

$$V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right).$$

In the various devices of the ADP330X series, the R1-R2 divider is adjusted to produce standard output voltages of 2.7, 3.0, 3.2, 3.3, and 5.0V.

As can be noted from this discussion, unlike a conventional reference setup, there is no power wasting reference current such as used in a conventional regulator topology (I_{REF} of Fig. 2.24). In fact, the Fig. 2.32 regulator behaves as if the entire error amplifier has simply an offset voltage of V_{REF} volts, as seen at the output of a conventional R1-R2 divider.

Design Features Related to AC Performance

While the above described DC performance enhancements of the ADP330X series are worthwhile, the most dramatic improvements come in areas of AC related performance. These improvements are in fact the genesis of the anyCAP™ series name.

Capacitive loading and the potential instability it brings is a major deterrent to easily applying LDOs. While low dropout goals prevent the use of emitter follower type outputs, and so preclude their desirable buffering effect against cap loading, there is an alternative technique of providing load immunity. One method of providing a measure of insusceptibility against variation in a particular amplifier response pole is called *pole splitting* (see Reference 8). It refers to an amplifier compensation method whereby two response poles are shifted in such a way so as to make one a dominant, lower frequency pole. In this manner the secondary pole (which in this case is the C_L related output pole) becomes much less of a major contributor to the net AC response. This has the desirable effect of greatly de-sensitizing the amplifier to variations in the output pole.

A Basic Pole-Splitting Topology

A basic LDO topology with frequency compensation as modified for pole splitting is shown in Figure 2.33. Here the internal compensation capacitor C_{COMP} is connected as an integrating capacitor, around pass device Q1 (C1 is the pass device input capacitance). While it is true that this step will help immunize the regulator to the C_L related pole, it also has a built in fatal flaw. With C_{COMP} connected directly to the Q1 base as shown, the line rejection characteristics of this setup will be quite poor. In effect, when doing it this way one problem (C_L sensitivity) will be exchanged for another (poor line rejection).

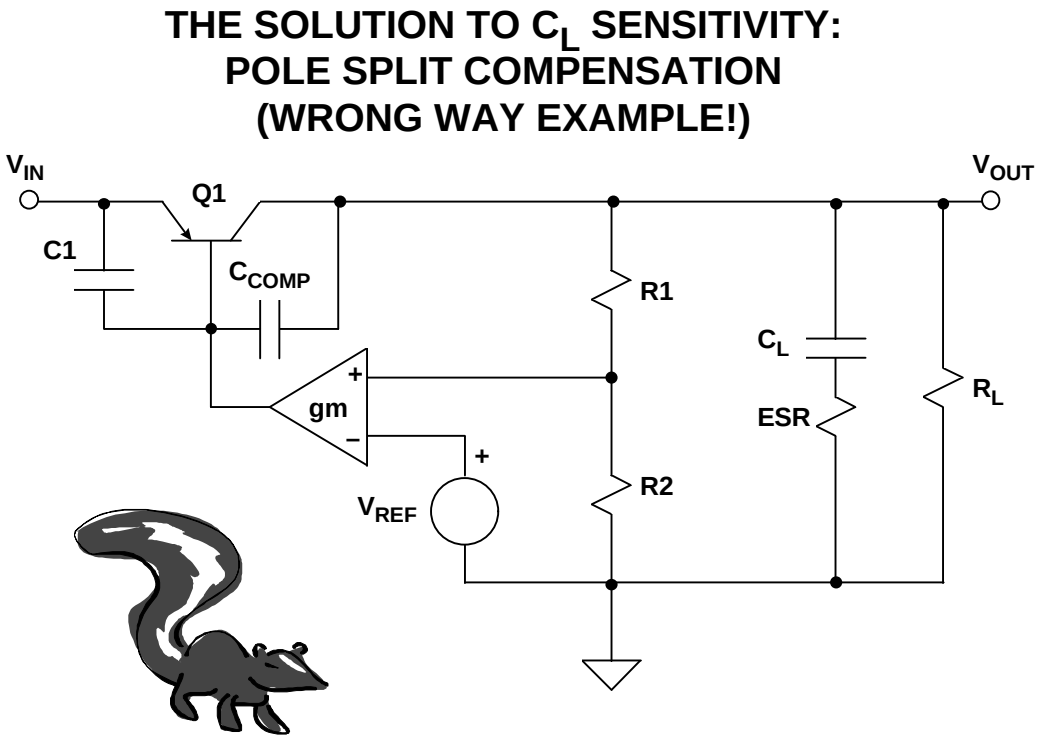


Figure 2.33

The anyCAP™ Pole-Splitting Topology

Returning to the anyCAP™ series topology, (Fig. 2.32, again) it can be noted that in this case C_{COMP} is isolated from the pass device's base (and thus input ripple variations), by the wideband non-inverting driver. But insofar as frequency compensation is concerned, because of this buffer's isolation, C_{COMP} still functions as a modified pole splitting capacitor (see Reference 9), and it does provide the benefits of a buffered, C_L independent single-pole response. The regulator's frequency response is dominated by the internal compensation, and becomes relatively immune to the value and ESR of load capacitor C_L. Thus the name anyCAP™ for the series is apt, as the design is tolerant of virtually any output capacitor type.

The benefits of the anyCAP™ topology are summarized by Figure 2.34. As can be noted, C_L can be as low as 0.47µF, and it can also be a multi-layer ceramic capacitor (MLCC) type. This allows a very small physical size for the entire regulation function, such as when a SOT-23 packaged anyCAP™ LDO is used, for example the ADP3300 device. Because of the in-sensitivity to C_L, the designer needn't worry about such things as ESR zones, and can better concentrate on the system aspects of the regulator application.

BENEFITS OF anyCAP™ LDO TOPOLOGY

- Internal C_{COMP} Dominates Response Rolloff
- C_L Can Range from 0.47µF(min) to Infinity
- Low and Ultra-Low C_L ESR is OK
- MLCC Types for C_L Work, is Physically Smallest Solution
- No ESR Exclusion Zones
- Fast Load Transient Response and Good Line Rejection

Figure 2.34

The anyCAP™ LDO series devices

The major specifications of the anyCAP™ series of LDO regulators are summarized in Figure. 2.35. The devices include both single and dual output parts, with current capabilities ranging from 50 to 200mA. Rather than separate individual specifications for output tolerance, line and load regulation, plus temperature, the anyCAP™ series devices are rated simply for a combined total accuracy figure. This accuracy is either 0.8% at 25°C, or 1.4% over the temperature range with the device operating over an input range of V_{OUT} +0.3 (or 0.5V), up to 12V. With total accuracy being covered by one clear specification, the designer can then achieve a higher degree of confidence. It is important to note that this method of specification also includes operation within the regulator dropout range (unlike some LDO parts specified for higher input-output voltage difference conditions).

anyCAP™ SERIES LDO REGULATOR DEVICES

Part Number	V_{MIN} @ I_L (V, typ/max)	I_L (mA)	Accuracy (±% @ 25°C / ±% Full)	Package (All SO-8 are Thermal coastline)	Comment (Singles have NR, SD, ERR; Dual no NR)
ADP3300	0.08 / 0.17	50	0.8 / 1.4	SOT-23-6	Single
ADP3301	0.10 / 0.2	100	0.8 / 1.4	SO-8	Single
ADP3302	0.10 / 0.2	100	0.8 / 1.4	SO-8	Dual
ADP3303	0.18 / 0.4	200	0.8 / 1.4	SO-8	Single
ADP3307	0.13 / 0.22	100	0.8 / 1.4	SOT-23-6	Single

Figure 2.35

Functional Diagram and Basic 50 mA LDO Regulator

A functional diagram common to the various devices of the ADP330X series LDO regulators is shown by Figure 2.36. Operation of the various pins and internal functions is discussed below.

anyCAP™ SERIES LDO REGULATORS
FUNCTIONAL DIAGRAM

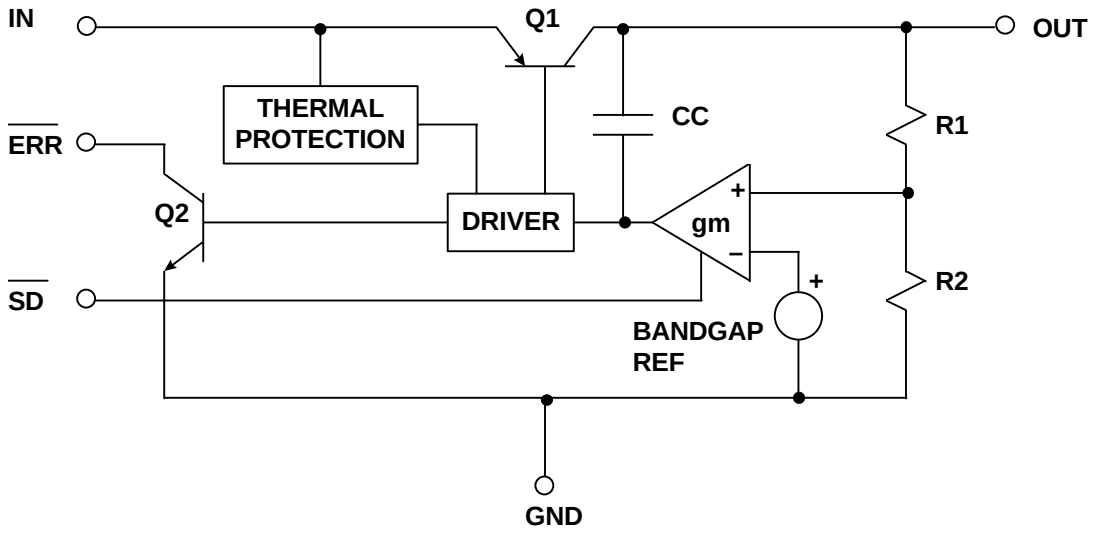


Figure 2.36

In application, the use of the anyCAP™ series of LDOs is simple, as shown by a basic 50mA ADP3300 regulator, in Figure 2.37. This circuit is a general one, to illustrate points common to the entire device series. The ADP3300 is a basic LDO regulator device, designed for fixed output voltage applications while operating from sources over a range of 3 to 12V and a temperature range of –40 to +85°C. The actual ADP3300 device ordered would be specified as ADP3300ART-YY, where the "YY" is a voltage designator suffix such as 2.7, 3, 3.2, 3.3, or 5, for those respective voltages. The "ART" portion of the part number designates the SOT23 6-lead package. The example circuit shown produces 5.0V with the use of the ADP3300-5.

In operation, the circuit will produce its rated 5V output for loads of 50mA or less, and for input voltages above 5.3V (V_{OUT} + 0.3V), when the shutdown input is in a HIGH state. This can be accomplished either by a logic HIGH control input to the $\overline{SD}$ pin, or by simply tying this pin to V_{IN}. When $\overline{SD}$ is LOW (or tied to ground), the regulator shuts down, and draws a quiescent current of 1μA or less.

A BASIC ADP3300 50mA LDO REGULATOR CIRCUIT

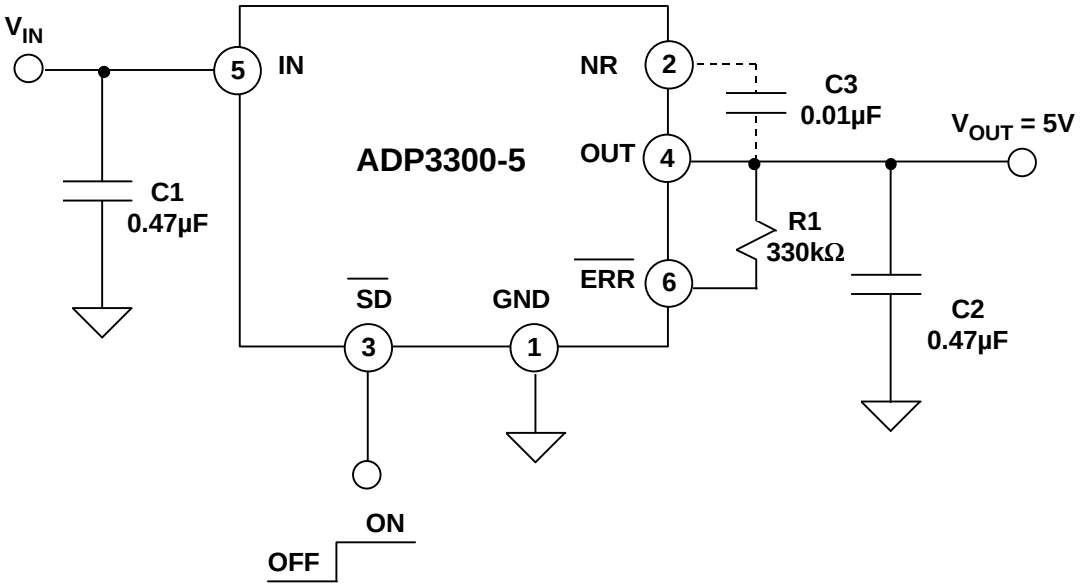


Figure 2.37

The ADP3300 and other anyCAP™ series devices maintain regulation over a wide range of load, input voltage and temperature conditions. However, when the regulator is overloaded or entering the dropout region (for example, by a reduction in the input voltage) the open collector $\overline{\text{ERR}}$ pin becomes active, by going to a LOW or conducting state. Once set, the $\overline{\text{ERR}}$ pin's internal hysteresis keeps the output low, until some margin of operating range is restored. In the circuit of Fig. 2.37, R1 is a pullup resistor for the $\overline{\text{ERR}}$ output, E_{OUT}. This resistor can be eliminated if the load being driven provides a pullup current.

The $\overline{\text{ERR}}$ function can also be activated by the regulator's over temperature protection circuit, which trips at 165°C. These internal current and thermal limits are intended to protect the device against accidental overload conditions. For normal operation, device power dissipation should be externally limited by means of heat sinking, air flow, etc. so that junction temperatures will not exceed 125°C.

A capacitor, C3, connected between pins 2 and 4, can be used for an optional noise reduction (NR) feature. This is accomplished by AC-bypassing a portion of the regulator's internal scaling divider, which has the effect of reducing the output noise ~10 dB. When this option is exercised, only low leakage 10 -100nF capacitors should be used. Also, input and output capacitors should be changed to 1 and 4.7µF values respectively, for lowest noise and the best overall performance. Note that the noise reduction pin is internally connected to a high impedance node, so connections to it should be carefully done to avoid noise. PC traces and pads connected to this pin should be as short and small as possible.

LDO Regulator Thermal Considerations

To determine a regulator's power dissipation, calculate it as follows:

$$P_D = (V_{IN} - V_{OUT})(I_L) + (V_{IN})(\text{Iground}),$$

where I_L and Iground are load and ground current, and V_{IN} and V_{OUT} are the input and output voltages respectively. Assuming I_L = 50mA, Iground = 0.5mA, V_{IN} = 8V, and V_{OUT} = 5V, the device power dissipation is:

$$P_D = (8 - 5)(0.05) + (8)(0.0005) = 0.150 + .004 = 0.154 \text{ W}.$$

To determine the regulator's temperature rise, ΔT, calculate it as follows:

$$\Delta T = T_J - T_A = P_D \times \theta_{JA} = 0.154\text{W} \times 165°\text{C/W} = 25.4°\text{C}.$$

With a maximum junction temperature of 125°C, this yields a calculated maximum safe ambient operating temperature of 125 – 25.4°C, or just under 100°C. Since this temperature is in excess of the device's rated temperature range of 85°C, the device will then be operated conservatively at an 85°C (or less) maximum ambient temperature.

These general procedures can be used for other devices in the series, substituting the appropriate θ_{JA} for the applicable package, and applying the remaining operating conditions. For reference, a complete tutorial section on thermal management is contained in Chapter 8.

In addition, layout and PCB design can have a significant influence on the power dissipation capabilities of power management ICs. This is due to the fact that the surface mount packages used with these devices rely heavily on thermally conductive traces or pads, to transfer heat away from the package. Appropriate PC layout techniques should then be used to remove the heat due to device power dissipation. The following general guidelines will be helpful in designing a board layout for lowest thermal resistance in SOT-23 and SO-8 packages:

1. *PC board traces with large cross sectional areas remove more heat. For optimum results, use large area PCB patterns with wide and heavy (2 oz.) copper traces, placed on the uppermost side of the PCB.*

2. *Electrically connect dual V_{IN} and V_{OUT} pins in parallel, as well as to the corresponding V_{IN} and V_{OUT} large area PCB lands.*

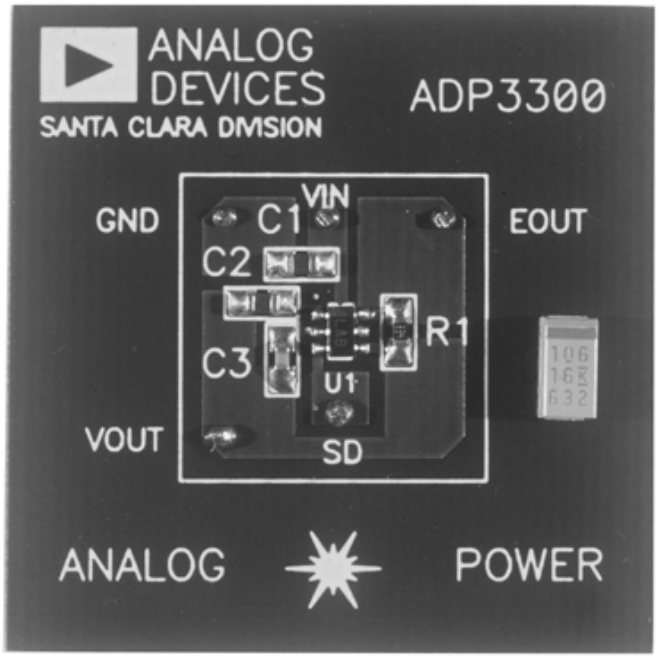
3. *In cases where maximum heat dissipation is required, use double-sided copper planes connected with multiple vias.*

4. *Where possible, increase the thermally conducting surface area(s) openly exposed to moving air, so that heat can be removed by convection (or forced air flow, if available).*

5. *Do* not *use solder mask or silkscreen on the heat dissipating traces, as they increase the net thermal resistance of the mounted IC package.*

A real life example visually illustrates a number of the above points far better than words can do, and is shown in Figure 2.38, a photo of the ADP3300 1.5" square evaluation PCB. The boxed area on the board represents the actual active circuit area.

ADP3300 EVALUATION BOARD:
CAPACITOR SIZE CAN MAKE A DIFFERENCE!



TOTAL BOARD SIZE: 1.5" X 1.5"

10µF / 16V TANTALUM CAPACITOR (KEMET T491C SERIES)

Figure 2.38

In this figure, a large cross section conductor area can be seen associated with pin 4 and V_{OUT}, the large "U" shaped trace at the lower part within the boxed outline.

Also, the effect of the anyCAP™ design on capacitor size can be noted from the tiny size of the C1 and C2 0.47µF input and output capacitors, near the upper left of the boxed area. For comparison purposes, a 10µF/16V tantalum capacitor (Kemet T491C-series) is also shown outside the box, as it might be used on a more conventional LDO circuit. It is several times the size of output capacitor C2.

Recent developments in packaging have led to much improved thermal performance for power management ICs. The anyCAP™ LDO regulator family capitalizes on this most effectively, using a thermally improved leadframe as the basis for all 8 pin devices. This package is called a "Thermal Coastline" design, and is shown in Figure. 2.39. The foundation of the improvement in heat transfer is related to two key parameters of the leadframe design, distance and width. The payoff comes in the reduced thermal resistance of the leadframe based on the Thermal Coastline, only 90°C/W versus 160°C/W for a standard SO-8 package. The increased dissipation of the Thermal Coastline allows the anyCAP™ series of SO-8 regulators to support more than one watt of dissipation at 25°C.

anyCAP™ SERIES REGULATORS IN SO-8 USE THERMAL COASTLINE PACKAGES

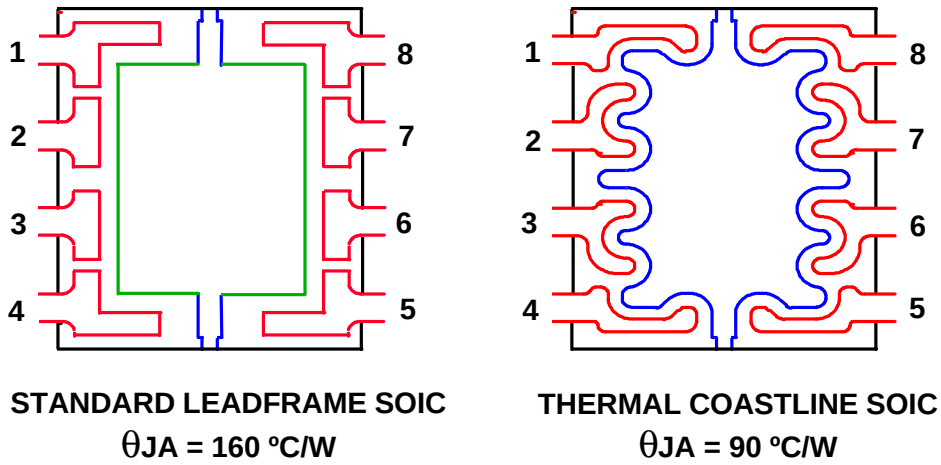


Figure 2.39

Additional insight into how the new leadframe increases heat transfer can be appreciated by Figure. 2.40. In this figure, it can be noted how the spacing of the Thermal Coastline paddle and leads shown on the right is reduced, while the width of the lead ends are increased, versus the standard leadframe, on the left.

DETAILS OF THERMAL COASTLINE PACKAGE

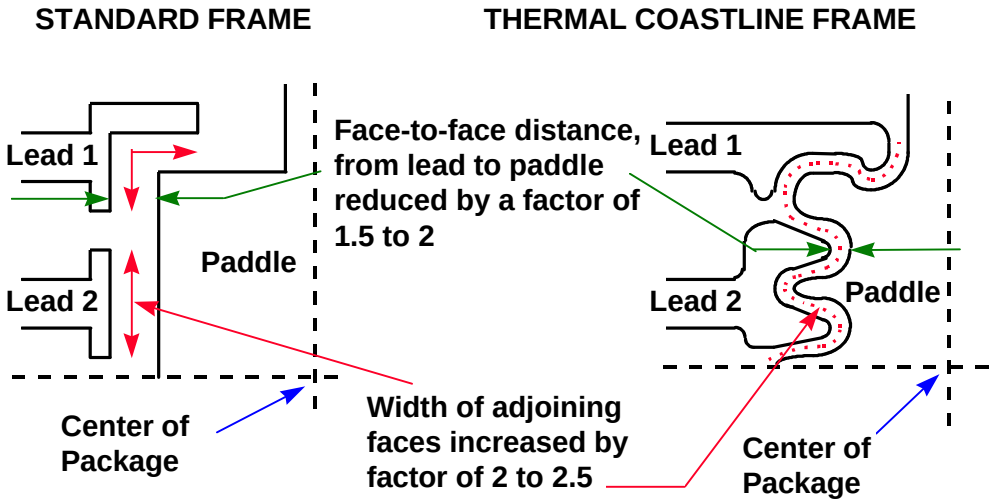


Figure 2.40

LDO REGULATOR CONTROLLERS

To complement the anyCAP™ series of standalone LDO regulators, there is also the LDO *regulator controller*. The regulator controller IC picks up where the standalone regulator IC is no longer useful in either load current or power dissipation terms, and uses an external PMOS FET for the pass device. The ADP3310 is a basic LDO regulator controller device, designed for fixed output voltage applications while operating from sources over a range of 3.8 to 15V and a temperature range of –40 to +85°C. The actual ADP3310 device ordered would be specified as ADP3310AR-YY, where the "YY" is a voltage designator suffix such as 2.8, 3, 3.3, or 5, for those respective voltages. The "AR" portion of the part number designates the SO-8 Thermal Coastline 8-lead package. A summary of the main features of the ADP3310 device is listed in Figure 2.41.

anyCAP™ ADP3310 LDO REGULATOR CONTROLLER FEATURES

- **Controller drives external PMOS power FETs**
  - **User FET choice determines I_L and V_{MIN} performance**
  - **Small, 2 chip regulator solution handles up to 10A**
- **Advantages compared to integrated solutions**
  - **High accuracy (1.5%) fixed voltages; 2.8, 3, 3.3, or 5V**
  - **User flexibility (selection of FET for performance)**
  - **Small footprint with anyCAP™ controller and SMD FET**
  - **Kelvin output sensing possible**
  - **Integral, low-loss current limit sensing for protection**

Figure 2.41

Regulator Controller Differences

An obvious basic difference of the regulator controller versus a stand alone regulator is the removal of the pass device from the regulator chip. This design step has both advantages and disadvantages. A positive is that the external PMOS pass device can be chosen for the exact size, package, current rating and power handling which is most useful to the application. This approach allows the same basic controller IC to be useful for currents of several hundred mA to more than 10A, simply by choice of the FET. Also, since the regulator controller IC's Iground of 800µA results is very little power dissipation, its thermal drift will be enhanced. On the downside, there are two packages now used to make up the regulator function. And, current limiting (which can be made completely integral to a standalone IC LDO regulator) is now a function which must be split between the regulator controller IC and an external sense resistor. This step also increases the dropout voltage of the LDO regulator controller somewhat, by about 50mV.

A functional diagram of the ADP3310 regulator controller is shown in Figure 2.42. The basic error amplifier, reference and scaling divider of this circuit are similar to the standalone anyCAP™ regulator, and will not be described in detail. The regulator controller version does share the same cap load immunity of the standalone versions, and also has a shutdown function, similarly controlled by the EN (enable) pin.

The main differences in the regulator controller IC architecture is the buffered output of the amplifier, which is brought out on the GATE pin, to drive the external PMOS FET. In addition, the current limit sense amplifier has a built in 50mV threshold voltage, and is designed to compare the voltage between the V_{IN} and IS pins. When this voltage exceeds 50mV, the current limit sense amplifier takes over control of the loop, by shutting down the error amplifier and limiting output current to the preset level.

FUNCTIONAL BLOCK DIAGRAM OF anyCAP™ SERIES LDO REGULATOR CONTROLLER

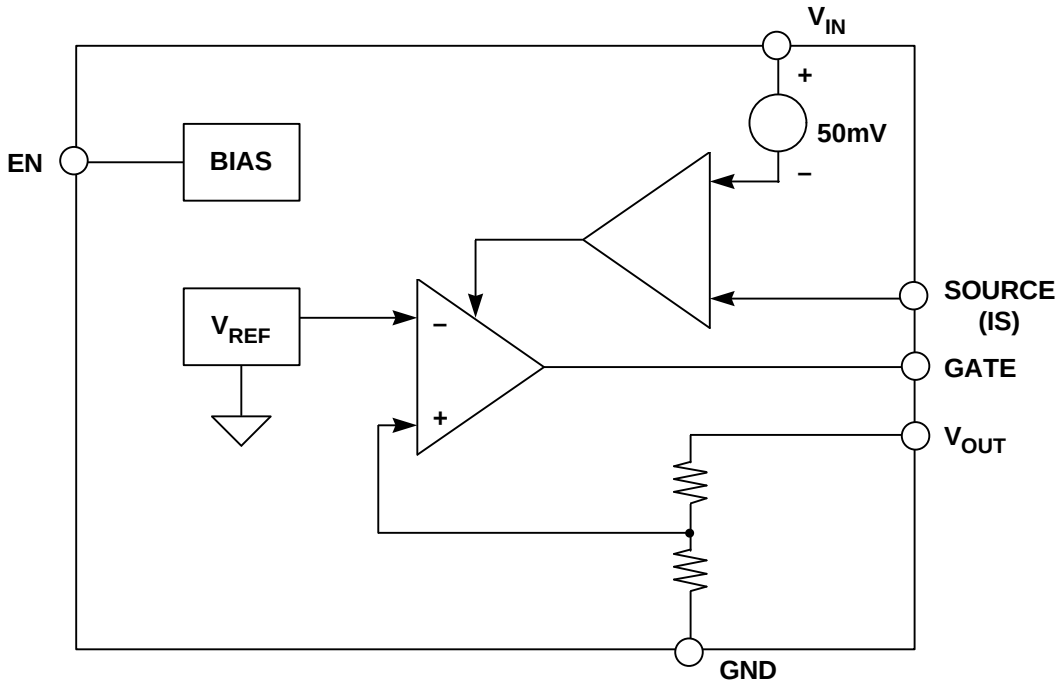


Figure 2.42

A Basic 5V/1A LDO Regulator Controller

An LDO regulator controller is easy to use, since a PMOS FET, a resistor and two relatively small capacitors (one at the input, one at the output) is all that is needed to form an LDO regulator. The general configuration is shown by Figure 2.43, an LDO suitable as a 5V/1A regulator operating from a V_{IN} of 6V, using the ADP3310-5 controller IC.

This regulator is stable with virtually any good quality output capacitor used for C_L (as is true with the other anyCAP™ devices). The actual C_L value required and its associated ESR depends on the gm and capacitance of the external PMOS device. In

general, a 10µF capacitor at the output is sufficient to ensure stability for load currents up to 10A. Larger capacitors can also be used, if high output surge currents are present. In such cases, low ESR capacitors such as OS-CON electrolytics are preferred, because they offer lowest ripple on the output. For less demanding requirements, a standard tantalum or aluminum electrolytic can be adequate. When an aluminum electrolytic is used, it should be qualified for adequate performance over temperature. The input capacitor, C_{IN}, is only necessary when the regulator is several inches or more distant from the raw DC filter capacitor. However, since it is a small type, it is usually prudent to use it in most instances, located close to the V_{IN} pin of the regulator.

A BASIC ADP3310 PMOS FET 1A LDO REGULATOR CONTROLLER CIRCUIT

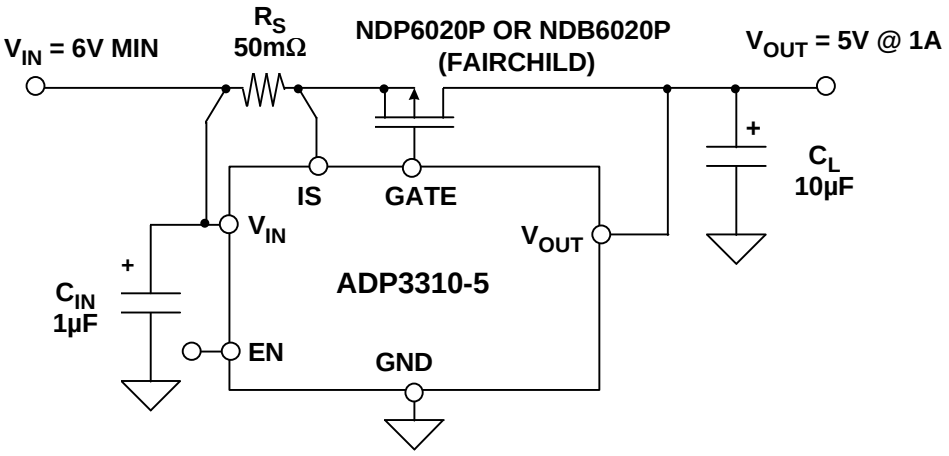


Figure 2.43

Selecting the Pass Device

The type and size of the pass transistor are determined by a set of requirements for threshold voltage, input-output voltage differential, load current, power dissipation, and thermal resistance. An actual PMOS pass device selected must satisfy all of these electrical requirements, plus physical and thermal parameters. There are a number of manufacturers offering suitable devices in packages ranging from SO-8 up through TO-220 in size.

To ensure that the maximum available drive from the controller will adequately drive the FET under worst case conditions of temperature range and manufacturing tolerances, the maximum drive from the controller ($V_{GS(DRIVE)}$) to the pass device must be determined. This voltage is calculated as follows:

$$V_{GS(DRIVE)} = V_{IN} - V_{BE} - \left(I_{L(MAX)}\right)\left(R_S\right),$$

where V_{IN} is the minimum input voltage, $I_{L(MAX)}$ is the maximum load current, R_S the sense resistor, and V_{BE} is a voltage internal to the ADP3310 (~ 0.5 @ high temp, 0.9 cold, and 0.7V at room temp). Note that since $I_{L(MAX)} \times R_S$ will be no more than 75mV, and V_{BE} at cold temperature ≅0.9V, this equation can be further simplified to:

$$V_{GS(DRIVE)} \cong V_{IN} - 1V .$$

In the Figure 2.43 example, V_{IN} = 6V and V_{OUT} = 5V, so $V_{GS(DRIVE)}$ is 6 – 1 = 5V.

It should be noted that the above two equations apply to FET drive voltages which are *less* than the typical gate-to-source clamp voltage of 8V (built into the ADP3310, for the purposes of FET protection).

An overall goal of the design is to then select an FET which will have an $R_{DS(ON)}$ sufficiently low so that the resulting dropout voltage will be less than $V_{IN} - V_{OUT}$, which in this case is 1V. For the NDP6020P used in Fig. 2.43 (see Reference 10), this device achieves an $R_{DS(ON)}$ of 70 milliohms (max) with a V_{GS} of 2.7V, a voltage drive appreciably less than the ADP3310's $V_{GS(DRIVE)}$ of 5V. The dropout voltage V_{MIN} of this regulator configuration is the sum of two series voltage drops, the FET's drop plus the drop across R_S, or:

$$V_{MIN} = I_{L(MAX)} \left(R_{DS(ON)} + R_S \right).$$

In the design here, the two resistances are roughly comparable to one another, so the net V_{MIN} will be 1A × (50+70 milliohms) = 120mV.

For a design safety margin, use a FET with a rated V_{GS} at the required R_{DS}, with a substantial headroom between the applicable ADP3310 $V_{GS(DRIVE)}$ and the applicable V_{GS} rating for the FET. In the case here, there is ample margin, with 5V of drive and a V_{GS} of 2.7V. It should be borne in mind that the FET's V_{GS} and $R_{DS(ON)}$ will change over temperature, but for the NDP6020P device even these variations and a V_{GS} of 4.5V are still possible with the circuit as shown. With a rated minimum DC input of 6V, this means that the design is conservative with 5V output. In practice, the circuit will typically operate with input voltage minimums on the order of V_{OUT} plus the dropout of 120mV, or ~ 5.12V. Since the NDP6020P is also a fairly low threshold device, it will typically operate at lower output voltages, down to about 3V.

In the event the output is shorted to ground, the pass device chosen must be able to conduct the maximum short circuit current, both instantaneously and longer term.

Thermal Design

The maximum allowable thermal resistance between the FET junction and the highest expected ambient temperature must be taken into account, to determine the type of FET package and heat sink used (if any).

Whenever possible to do so reliably, the FET pass device can be directly mounted to the PCB, and the available PCB copper lands used as an effective heat sink. This heat sink philosophy will likely be adequate when the power to be dissipated in the FET is on the order of 1-2W or less. Note that the very nature of an LDO helps this type of design immensely, as the lower voltage drop across the pass device reduces the power to be dissipated. Under normal conditions for example, Q1 of Figure 2.43 dissipates less than 1W at a current of 1A, since the drop across the FET is less than 1V.

To use PCB lands as effective heat sinks with SO-8 and other SMD packages, the pass device manufacturer's recommendations for the lowest θ_{JA} mounting should be followed (see References 11 and 12). In general these suggestions will likely parallel the 5 rules noted above, under "LDO regulator thermal considerations" for SO-8 and SOT-23 packaged anyCAP™ LDOs. For lowest possible thermal resistance, also connect multiple FET pins together, as follows:

Electrically connect multiple FET source and drain pins in parallel, as well as to the corresponding R_S and V_{OUT} large area PCB lands.

Using 2 oz. copper PCB material and one square inch of copper PCB land area as a heatsink, it is possible to achieve a net thermal resistance, θ_{JA}, for mounted SO-8 devices on the order of 60°C/W or less. Such data is available for SO-8 power FETs (see Reference 11). There are also a variety of larger packages with lower thermal resistance than the SO-8, but still useful with surface mount techniques. Examples are the DPAK and D^2PAK, etc.

For higher power dissipation applications, corresponding to thermal resistance of 50°C/W or less, a bolt-on external heat sink is required to satisfy the θ_{JA} requirement. Compatible package examples would be the TO-220 family, which is used with the NDP6020P example of Fig. 2.43.

Calculating thermal resistance for V_{IN} = 6.7V, V_{OUT} = 5V, and I_L = 1A:

$$\theta_{JA} = \frac{T_J - T_{A(MAX)}}{V_{DS(MAX)} \cdot I_L},$$

where T_J is the pass device junction temperature limit, $T_{A(MAX)}$ is the maximum ambient temperature, $V_{DS(MAX)}$ is the maximum pass device drain-source voltage, and $I_{L(MAX)}$ is the maximum load current.

Inserting some example numbers of 125°C as a max. junction temp for the NDP6020P, a 75°C expected ambient, and the $V_{DS(MAX)}$ and $I_{L(MAX)}$ figures of 1.7V and 1A, the required θ_{JA} works out to be 125 – 75/1.7 = 29.4°C/W. This can be met with a very simple heat sink, which is derived as follows.

The NDP6020P in the TO-220 package has a junction-case thermal resistance, θ_{JC}, of 2°C/W. The required external heatsink's thermal resistance, θ_{CA}, is determined as follows:

$$\theta_{CA} = \theta_{JA} - \theta_{JC},$$

where θ_{CA} is the required heat sink case-to-ambient thermal resistance, θ_{JA} is the calculated *overall* junction-to-ambient thermal resistance, and θ_{JC} is the pass device junction-to-case thermal resistance, which in this case is 2°C/W typical for TO-220 devices, and NDP6020P.

$$\theta_{CA} = 29.4°C/W - 2°C/W = 27.4°C/W.$$

For a safety margin, select a heatsink with a θ_{CA} *less* than the results of this calculation. For example, the Aavid TO-220 style clip on heat sink # 576802 has a θ_{CA} of 18.8°C/W, and in fact many others have performance of 25°C/W or less. As an alternative, the NDB6020P D^2PAK FET pass device could be used in this same design, with an SMD style heat sink such as the Aavid 573300 series used in conjunction with an internal PCB heat spreader.

Note that many LDO applications like the above will calculate out with very modest heat sink requirements. This is fine, as long as the output never gets shorted! With a shorted output, the current goes to the limit level (as much as 1.5A in this case), while the voltage across the pass device goes to V_{IN} (which could also be at a maximum). In this case, the new pass device dissipation for short circuit conditions becomes 1.5A × 6.7V, or 10W. Supporting this level of power continuously will require the entire heat sink situation to be re-evaluated, as what was adequate for 1.7W will simply not be adequate for 10W. In fact, the required heat sink θ_{CA} is about 3°C/W to support the 10W safely on a continuous basis, which requires a much larger heat sink.

Note that a general overview of thermal design and heat sink selection is included in section 8.

Sensing Resistors for LDO Controllers

Current limiting in the ADP3310 controller is achieved by choosing an appropriate external current sense resistor, R_S, which is connected between the controller's V_{IN} and IS (source) pins. An internally derived 50 mV current limit threshold voltage appears between these pins, to establish a comparison threshold for current limiting. This 50mV determines the threshold where current limiting begins. For a continuous current limiting, a foldback mode is established, with dissipation controlled by reducing the gate drive. The net effect is that the ultimate current limit level is a factor of 2/3 of maximum. The foldback limiting reduces the power dissipated in the pass transistor substantially.

To choose a sense resistor for a maximum output current I_L, R_S is calculated as follows:

$$R_S = \frac{0.05}{K_F \cdot I_L}.$$

In this expression, the nominal 50mV current limit threshold voltage appears in the numerator. In the denominator appears a scaling factor K_F, which can be either 1.0 or 1.5, plus the maximum load current, I_L. For example, if a scaling factor of 1.0 is to be used for a 1A I_L, the R_S calculation is straightforward, and 50 milliohms is the correct R_S value.

However, to account for uncertainties in the threshold voltage and to provide a more conservative output current margin, a scaling factor of K_F = 1.5 can alternately be used. When this approach is used, the same 1A I_L load conditions will result in a 33 milliohm R_S value. In essence, the use of the 1.5 scaling factor takes into account the foldback scheme's reduction in output current, allowing higher current in the limit mode.

The simplest and least expensive sense resistor for high current applications such as Figure 2.43 is a copper PCB trace controlled in both thickness and width. Both the temperature dependence of copper and the relative size of the trace must be taken into account in the resistor design. The temperature coefficient of resistivity for copper has a positive temperature coefficient of +0.39%/°C. This natural copper TC, in conjunction with the controller's PTAT based current limit threshold voltage, can provide for a current limit characteristic which is simple and effective over temperature.

The table of Figure 2.44 provides resistance data for designing PCB copper traces with various PCB copper thickness (or weight), in ounces of copper per square foot area. To use this information, note that the center column contains a resistance coefficient, which is the conductor resistance in milliohms/inch, divided by the trace width, W. For example, the first entry, for 1/2 ounce copper is 0.983 milliohms/inch/W. So, for a reference trace width of 0.1", the resistance would be 9.83 milliohms/inch. Since these are all linear relationships, everything scales for wider/skinnier traces, or for differing copper weights. As an example, to design a 50 milliohm R_S for the circuit of Fig. 2.43 using 1/2 ounce copper, a 2.54" length of a 0.05” wide PCB trace could be used.

PRINTED CIRCUIT COPPER RESISTANCE DESIGN FOR LDO CONTROLLERS

Copper Thickness	Resistance Coefficient, Milliohms / inch/ W (trace width W in inches)	Reference 0.1 Inch wide trace, Milliohms / inch
1/2 oz / ft^2	0.983 / W	9.83
1 oz / ft^2	0.491 / W	4.91
2 oz / ft^2	0.246 / W	2.46
3 oz / ft^2	0.163 / W	1.63

Figure 2.44

To minimize current limit sense voltage errors, the two connections to R_S should be made four-terminal style, as is noted in Figure 2.43 (again). It is not absolutely

necessary to actually use four-terminal style resistors, except for the highest current levels. However, as a minimum, the heavy currents flowing in the source circuit of the pass device should not be allowed to flow in the ADP3310 sense pin traces. To minimize such errors, the V_{IN} connection trace to the ADP3310 should connect close to the body of R_S (or the resistor's input sense terminal), and the IS connection trace should also connect close to the resistor body (or the resistor's output sense terminal). Four-terminal wiring is increasingly important for output currents of 1A or more.

Alternately, an appropriate selected sense resistor such as surface mount sense devices available from resistor vendors can be used (see Reference 13). Sense resistor R_S may not be needed in all applications, if a current limiting function is provided by the circuit feeding the regulator. For circuits that don't require current limiting, the IS and V_{IN} pins of the ADP3310 must be tied together.

PCB-Layout Issues

For best voltage regulation, place the load as close as possible to the controller device's V_{OUT} and GND pins. Where the best regulation is required, the V_{OUT} trace from the ADP3310 and the pass device's drain connection should connect to the positive load terminal via separate traces. This step (Kelvin sensing) will keep the heavy load currents in the pass device's drain out of the feedback sensing path, and thus maximize output accuracy. Similarly, the unregulated input common should connect to the common side of the load via a separate trace from the ADP3310 GND pin.

These points are summarized in the "Techniques" discussion of section 8, around Figures. 8.10 and 8.11 specifically.

A 2.8V/8A LDO Regulator Controller

With seemingly minor changes to the basic 1A LDO circuit used in Fig. 2.43, an 8A LDO regulator controller can be configured, as shown in Figure 2.45. This circuit uses an ADP3310- 2.8, to produce a 2.8V output. The sense resistor is dropped to 5 milliohms, which supports currents of up to 10A (or about 6.7A, with current limiting active). Four-terminal wiring should be used with the sense resistor to minimize errors.

The most significant change over the more generic schematic of Fig. 2.43 is the use of multiple, low ESR input and output bypass capacitors. At the output, C2 is a bank of 4 × 220µF OS-CON type capacitors, in parallel with 2 × 10µF MLCC chip type capacitors. These are located right at the load point with minimum inductance wiring, plus separate wiring back to the V_{OUT} pin of the ADP3310 and the drain of the pass device. This wiring will maximize the DC output accuracy, while the multiple capacitors will minimize the transient errors at the point-of-load. In addition, multiple bypasses on the regulator input in the form of C1 minimizes the transient errors at the regulator's V_{IN} pin.

A 2.8V/8A LDO REGULATOR CONTROLLER

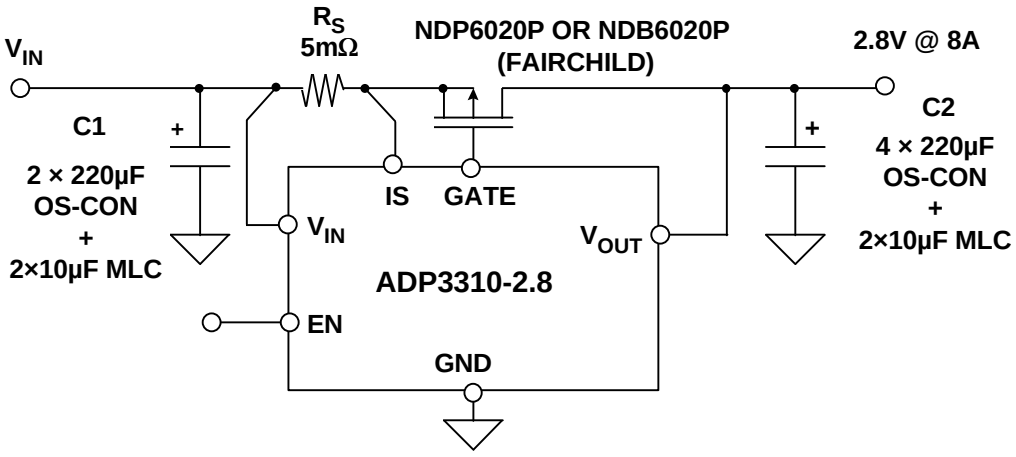


Figure 2.45

Heat sink requirements for the pass device in this application will be governed by the loading and input voltage, and should be calculated by the procedures discussed above.

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