DP83956EB-SA Stand Alone Hub

National Semiconductor
Application Note 896
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July 1993

1.0 INTRODUCTION

The DP83956EB-SA board is a low cost, stand alone, local area network repeater hub with minimal status display. The board is designed to demonstrate National Semiconductor's LitE Repeater Interface Controller (LERIC™—DP83956). This stand alone hub solution contains 12 twisted pair ports, an Attachment Unit Interface (AUI) port, and a coaxial transceiver interface (CTI) port. The board allows for cascading with another DP83956EB-SA or a DP83956EB-AT board (6 port repeater hub card for use in an AT-Bus). The board requires a single +12V supply to become operational. The DP83956EB-SA board uses surface mount components to minimize size. Below is a list of the major features of the DP83956EB-SA board:

- 14 ports: 12 twisted pair ports, 1 CTI port, and a AUI port
- Powered by single +12V DC supply
- Jumper for easy termination of coax port
- 4 LEDs for real-time hub status
- Surface mount components for small size
- Designed for minimal EMI radiation
- Cascading headers for daisy chaining with another DP83956EB-SA or a DP83956EB-AT board
- Designed for low cost
- Stand alone
- Expansion header for full LED status, LERIC register access, or hub status counters
- Easy to operate with a single switch for LERIC mode load

2.0 USER'S GUIDE

2.1 Start Up

The DP83956EB-SA board should be connected to a 12V DC supply at right-angle header J1. The polarity of the input power should match 12V and GND markings next to J1. For proper operation of the coax port the jumper shunt on JP19 should be removed. The RESET button, S1 forces the LERIC controllers to restart, which will reset the consecutive collision counters, unpartition all ports, and perform a mode load with the options on switch S1. When the DP83956EB-SA is powered up or the RESET button is pushed, all four status LEDs will light up for one second.

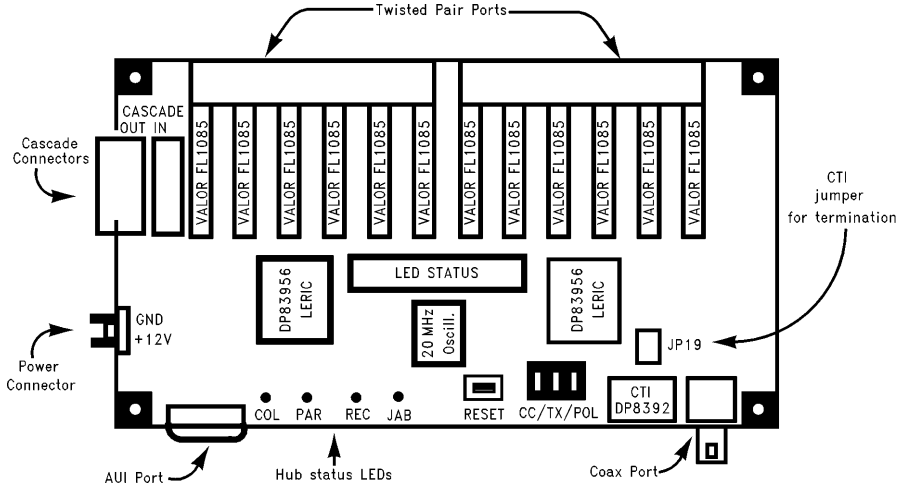

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FIGURE 1. DP83956EB-SA Board

RRD-B30M75/Printed in U. S. A.

2.2 Mode Load Options

Three of the LERIC mode load options are available to the user on switch S2. This switch configures both of the LERICs upon reset or power up. S2 is labelled CC/TX/POL corresponding to the options in that order. The CC switch sets the consecutive collision limit for the LERICs. The LERICs will partition a port after 31 or 63 consecutive collisions on that port, depending on the CC switch value. The CC switch allows the user to set the consecutive collision limit for all fourteen ports on the board. When in the OFF position, the LERICs will partition after 31 consecutive collisions. The ON position will configure the LERICs for 63 consecutive collisions.

The switch labelled TX configures the unpartition on transmit only bit ($\overline{\text{TXONLY}}$). If this bit is selected the LERICs will only unpartition a port after a good packet (532 bits or more without a collision) has been transmitted on that port. Without this bit set, the LERICs will unpartition a port after a good packet is transmitted or received. When the switch is in the OFF position, unpartition on transmit only is not selected, while in the ON position, $\overline{\text{TXONLY}}$ is selected on all fourteen ports. Switch number 3, POL enables or disables the polarity reversal option on the twisted pair ports (ports 2–13). This switch has no effect on ports 1 and 14. When the POL switch in the OFF position, the twisted pair ports will switch the polarity of the receive lines when inverted packets or link pulses are received on that port. If this switch is in the ON position, only packets and link pulses with the correct polarity will be recognized by the LERICs. More information on these functions is contained in the LERIC data sheet under mode load. Below is a table of the MLOAD options.

TABLE I. MLOAD Quick Reference Guide

SWITCH	LERIC Data Sheet Name	ON Position	OFF Position
CC	CCLIM	63 Consecutive Collisions to partition a port.	31 Consecutive Collisions to partition a port.
TX	$\overline{\text{TXONLY}}$	Ports unpartition on good transmissions only.	Ports can unpartition on good receptions or transmissions.
POL	EPOLSW	Polarity reversal on ports 2-13 is disabled.	Polarity reversal on ports 2-13 is enabled.

Note: Options are loaded only during power up or reset.

2.3 CTI Termination Jumper (JP19)

Included in the coaxial transceiver logic is a jumper (JP19) and a shunt for terminating the coax transceiver. When not connected to a coax cable with proper termination, the CTI will continuously detect collision and the LERIC will partition the port. To avoid receiving these false collisions and prevent the unnecessary partitioning of the port, JP19 was included to allow for termination of the CTI when it is not connected to a network segment. Placing a shunt on JP19 will terminate the CTI. When the coax port is going to be connected to a properly terminated network segment, the jumper shunt should be removed.

2.4 Cascading Boards

Cascading the DP83956EB-SA board with more DP83956EB-SA boards is as simple as connecting the ribbon cable and standoffs. No additional configuration is required. A short ribbon cable should be connected to the connector marked ''CASCADE OUT'' with the other end connected to the ''CASCADE IN'' of the board below in the stack. (See *Figure 2.*)

When cascaded, the repeater functions as a single hub. A packet received on any of the cascaded boards will be transmitted on all boards at the same time, so cascading boards via the interLERIC bus adds no additional delay to the network. The hub status LEDs will only monitor the status of activity on its board's ports with the exception of the jabber LED. The jabber LED will light up on all cascaded boards when jabber is detected, regardless of the port receiving the packet.

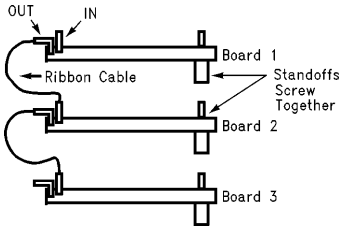

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FIGURE 2. Cascading Structure

2.5 LED Display

The LED display shows hub status for the board. If any port is receiving on the board, the green REC LED will light up. If any port on either chip is experiencing a transmit or receive collision the COL LED will be on. The APART LED will be on when any of the 14 ports on the DP83956EB-SA is partitioned. If the CTI is not properly terminated and the termination jumper (JP19) is off, the CTI port will be partitioned and the APART will go on. The jabber (JAB) LED will go on when a packet of excessive length has been received by any of the 14 ports. When boards are cascaded, the jabber LED will be lit on all boards when a jabber packet is received. Below is a quick reference chart for the LED status display.

TABLE II. LED Display Quick Reference

LED	OFF	ON
Any Partition (APART)	None of the ports on the board are partitioned.	One or more ports are partitioned on the board.
Any Collision (ACOL)	None of the ports on the board are experiencing collision.	A collision is occurring on one or more of the ports.
Any Receive (AREC)	None of the ports are receiving activity.	One or more ports are receiving activity on the board.
Jabber (JAB)	A jabber packet is not being received or transmitted.	A jabber packet is being received or transmitted.

3.0 A REVIEW OF THE DESIGN

The schematic for the DP83956EB-SA board is divided into functional blocks that appear on the different pages. The first page shows the interconnection of the functional blocks that make up the board along with the +12V power connector, power regulator for +5V output, and the decoupling capacitors. *Figure 4* shows a simplified block diagram of the DP83956EB-SA board. A daisy chain structure is required for the acknowledge in ($\overline{\text{ACKI}}$) and the acknowledge out ($\overline{\text{ACKO}}$) signals, while the remaining inter-LERIC bus signals are in a parallel bus configuration. The interacknowledge ($\overline{\text{INTACK}}$) signal connects the LERICs on a single board.

3.1 Twisted Pair Ports 2–13

The logic to construct a twisted pair port begins at the LERICs (Schematic sheet 2-LERIC connections). Each port contains 6 pins (+TX, −TX, +TXOP, −TXOP, +RX, −RX). The four transmit pins ±TX and ±TXOP are filtered by a simple RC low pass filter to reduce noise (Schematic sheet 9). The four transmit lines then enter a simple TTL line driver (74HCT245) which provides the power to drive the twisted pair line (Schematic sheet 10). The transmit signals are then connected to Pulse Engineering's PE-65438 (Valor FL1085) which provides the magnetic materials for shaping the waves and an isolation transformer. The PE-65438 contains wave shaping resistors selected for use with a 74HCT driver to reduce signal jitter, provide a 100Ω input impedance, and provide the proper output signal. The 245 was used because its pinout allowed for a cleaner layout (See layout sheet 1). *Figure 4* shows the path for the twisted pair ports and the items contained in the PE-65438. The receive path uses a common mode to reduce noise, a low pass filter to remove high frequency noise, and a 1:1 transformer for isolation. After the PE-65438, the twisted pair port is connected to a shielded modular jack. The shield of the modular jack is connected to chassis ground, which connects to the mounting holes for the board.

3.2 AUI Port 14

The connections for a full AUI port are shown on *Figure 11* of the schematic. From the LERIC's AUI port to the D connector only a 1:1 isolation transformer and some pull down resistors are required to construct the AUI port. The differential pairs are the same length and run in parallel as can be seen on *Figure 5*. To make the full AUI port of the LERICs into a twisted pair port, a twisted pair transceiver such as National's DP83922 would be required along the support logic. See the DP83922 data sheet for more information.

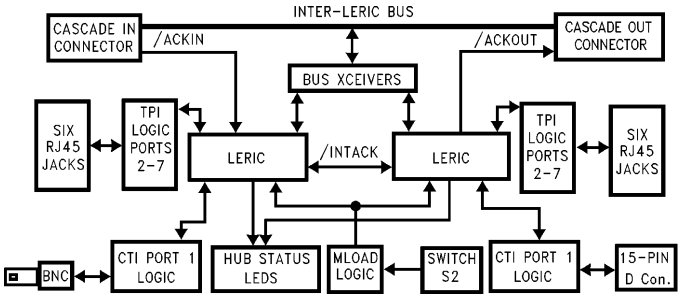

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FIGURE 3. Block Diagram of the DP83956EB-SA

3.3 CTI Port 1

The construction of the coax port is a copy of the sample schematic shown in the CTI data sheet and the LERIC data sheet. The schematic shows no termination on the BNC connector. For this reason, the repeater can only be connected to a coax line as a center tap. If a 50Ω resistor was inserted between the lines connected to the BNC, the coax port could be used as the end of a coax network. JP19 connects a 25Ω resistor in parallel with the BNC connector thus providing termination when the coax port is disconnected from the network. The PM6512 provides the isolated −9V supply needed to properly operate the CTI.

3.4 Cascading

Unlike the DP83955, the DP83956's bus signals allow for external transceivers for cascading via ribbon cable. TTL drivers are used in this design. Open collector non-inverting bus drivers (74ALS1035) are used to drive the $\overline{\text{ACTN}}$ and $\overline{\text{ANYXN}}$ signals. A 4-bit transceiver (74ALS243) is used to drive the $\overline{\text{IRE}}$, IRC, $\overline{\text{COLN}}$, and IRD lines. A 14 pin header is used to connect boards via ribbon cable in a daisy chain. An input and output connector are positioned on the board for easy stacking and connecting. Since pull up resistors are only needed on one board when multiple boards are cascaded, a TRI-STATE® buffer (74ALS241) is used to control the connection of the pull up resistors. With no boards cascaded, the buffer pulls up all of the bus resistors to V_{OH}. Two boards can be cascaded by simply connecting the output connector of one board to the input connector of another board. The pull up resistors will only be active when the input connector is not connected to an output connector. In a chain of boards, this only occurs for the board at the top of the chain. The top board will have its pull up resistors pulled high, while the lower boards will have high impedance connected to their pull up resistors. Pin 1 of input connector will trigger the 74ALS241 to connect the pull up resistors to a high impedance output.

3.5 LED Display

The LED display on the DP83956EB-SA board consists of 4 LEDs that represent real time status for the hub. The LED status is continuously strobed out from the data bus of both LERIC controllers. *Figure 8* shows the logic required for a minimum mode display. Since the DP83956EB-SA contains two controllers, the hub status is obtained from both controllers. The status displayed on the board is jabber (packet longer than 5 ms), collision, reception, and port partitioned. A 74ALS874 is used to latch in the strobed data since its dual 4-bit design allows for separate clock signals. The status for two controllers are active low ORed by the 74ALS09 AND gate. The open collector output on the 74ALS09 allows for the construction of a pulse stretcher on the jabber signal. The 10 ms jabber signal is invisible to the user, so a pulse stretcher is necessary to make that signal visible. The Schmitt trigger inverters that are used for the output of the jabber signal, are in the same package as the inverters used in the mode lode logic, so no additional chips are required to make the pulse stretcher. The LERIC controllers hold the receive and collision lights for 30 ms or until the next activity. The any partition LED remains lit as long as any port on either of the LERICs is partitioned.

3.6 Mode Load Logic

The mode load (mload) logic *(Figure 9)* configures the two LERIC controllers on the board upon power-on and when the reset button is pushed. Many configuration bits are hard wired since the board only allows for one setting (see the DP83955/56 data sheet for more details on mload). Three configuration bits are accessible by the user by a three position DIP switch on the board. The user guide section explains these options in further detail. Both LERIC controllers on the board will get the same configuration as can be seen in the schematic. The board also contains a reset button for resetting the controllers and performing a mload. The

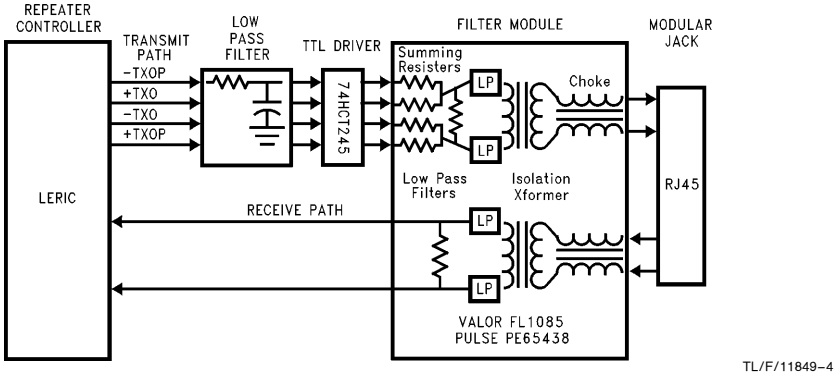

FIGURE 4. A Twisted Pair Interface for a Single Port

74HC14 is used to make a clean edge out of the discharging capacitor when reset is pushed and provide delay between the $\overline{\text{RESET}}$ signal to the LERIC controllers and the control of the buffers.

3.7 LED Status Header

This 32-pin connector was placed on the board to allow the user to build additional circuitry for displaying per port status, counting hub events, or accessing the LERIC registers.

TABLE III. LED Status Header

JP #	1	2	
3	DA7	DB7	Input/ Output
4	DA6	DB6	
5	DA5	DB5	
6	DA4	DB4	
7	DA3	DB3	
8	DA2	DB2	
9	DA1	DB1	
10	DA0	DB0	
11	$\overline{\text{WRA}}$	$\overline{\text{WRB}}$	Input Only
12	$\overline{\text{RDA}}$	$\overline{\text{RDB}}$	
13	$\overline{\text{BUFENA}}$	$\overline{\text{BUFENB}}$	Output Only
14	DFSA	DFSB	
15	$\overline{\text{STRA}}$	$\overline{\text{STRB}}$	Output Only
16	MIN/MAX	+5V	
17	GND	+5V	
18	GND	+5V	

The DP83956EB-SA is made of two LERICs that are labeled LERIC A and LERIC B. LERIC A contains twisted pair ports 2–7 and CTI port, while LERIC B contains twisted pair ports 8–13 and AUI port 14. The data bus for both chips must be isolated from each other, since the LERICs will strobe out different status information on the data pins. To construct a per-port (max mode) LED display, the MIN/MAX mode pin (JP14 pin 1) should be tied to 5V. This will change both LERICs mode load configuration for max mode when the board is powered on or reset. The data strobed on the data pins will now contain an address (D7–D5) and data (D4–D0) that will represent status for the individual ports. An addressable latch (74LS259) can be used to easily decode the status information and drive the LEDs. Table IV shows the port number mapping from the board to the specific LERIC chip port numbers. The LERIC data sheet shows a sample configuration for the max mode display.

TABLE IV. Port Number Conversion

LERIC Board Number	LERIC Port #
1 — CTI	Port 1 — LERIC A
2	Port 2 — LERIC A
3	Port 3 — LERIC A
4	Port 4 — LERIC A
5	Port 5 — LERIC A
6	Port 6 — LERIC A
7	Port 7 — LERIC A
8	Port 2 — LERIC B
9	Port 3 — LERIC B
10	Port 4 — LERIC B
11	Port 5 — LERIC B
12	Port 6 — LERIC B
13	Port 7 — LERIC B
14 — AUI	Port 1 — LERIC B

To construct event counters with the LED Status Header, the status should be decoded from the data strobed to the LEDs. Simple logic can then be trigger off the display freeze strobe (DFS) signal going true and the event being true. DFS will go high after activity has stopped on the repeater. DFS will remain high until the next activity or for a maximum of 30 ms. While DFS is high, the status for the last activity is held constant on the data bus. This is when the activity should be counted.

The construction of a register read or write module is possible since the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ pins are available. The buffer enable signal is also included to allow for controlling buffers to perform read or writes. The LERIC data sheet contains more information on the signals needed to construct a register read/write module.

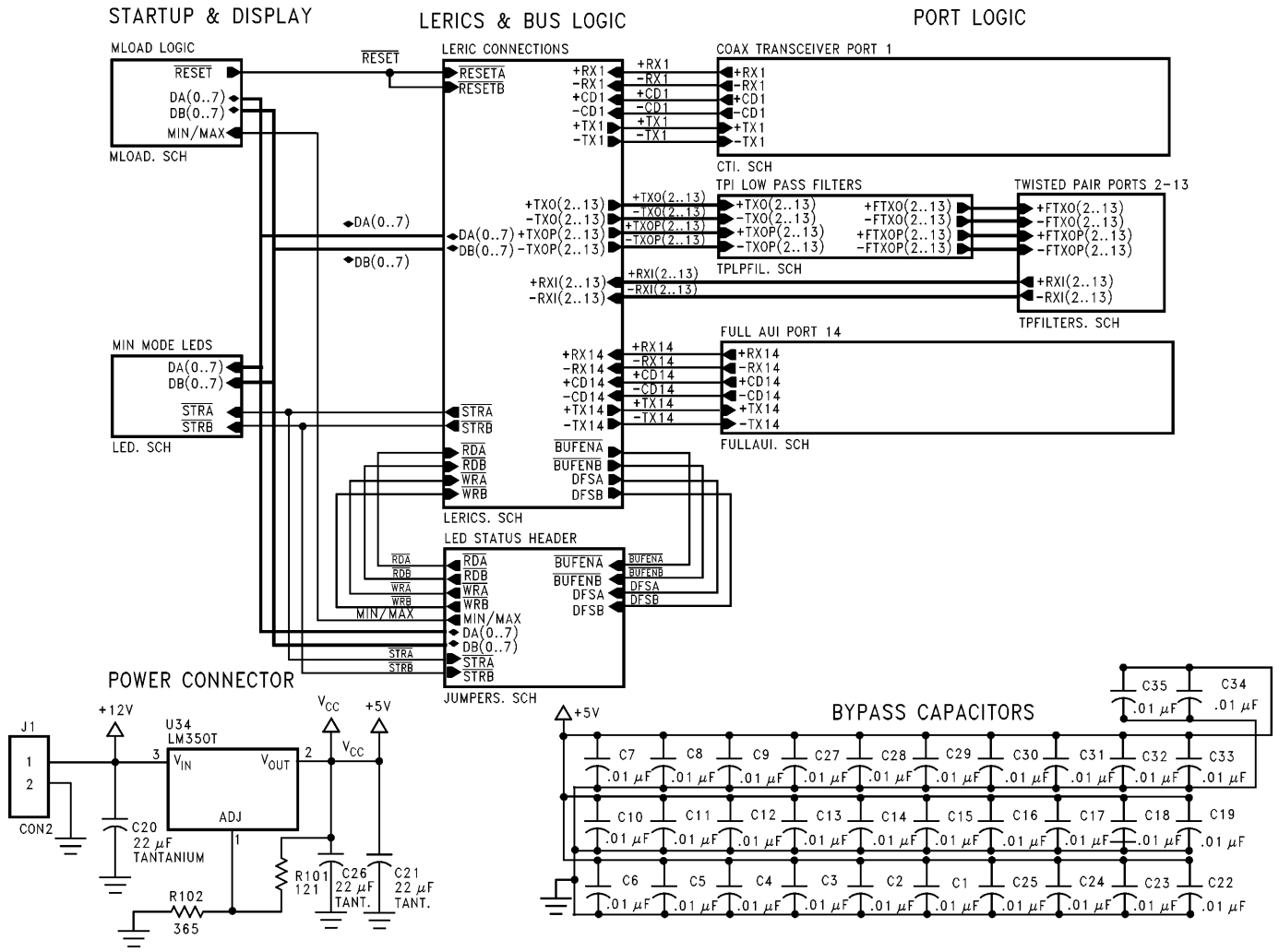

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FIGURE 5. LERIC DP83956EB-SA Demonstration Board

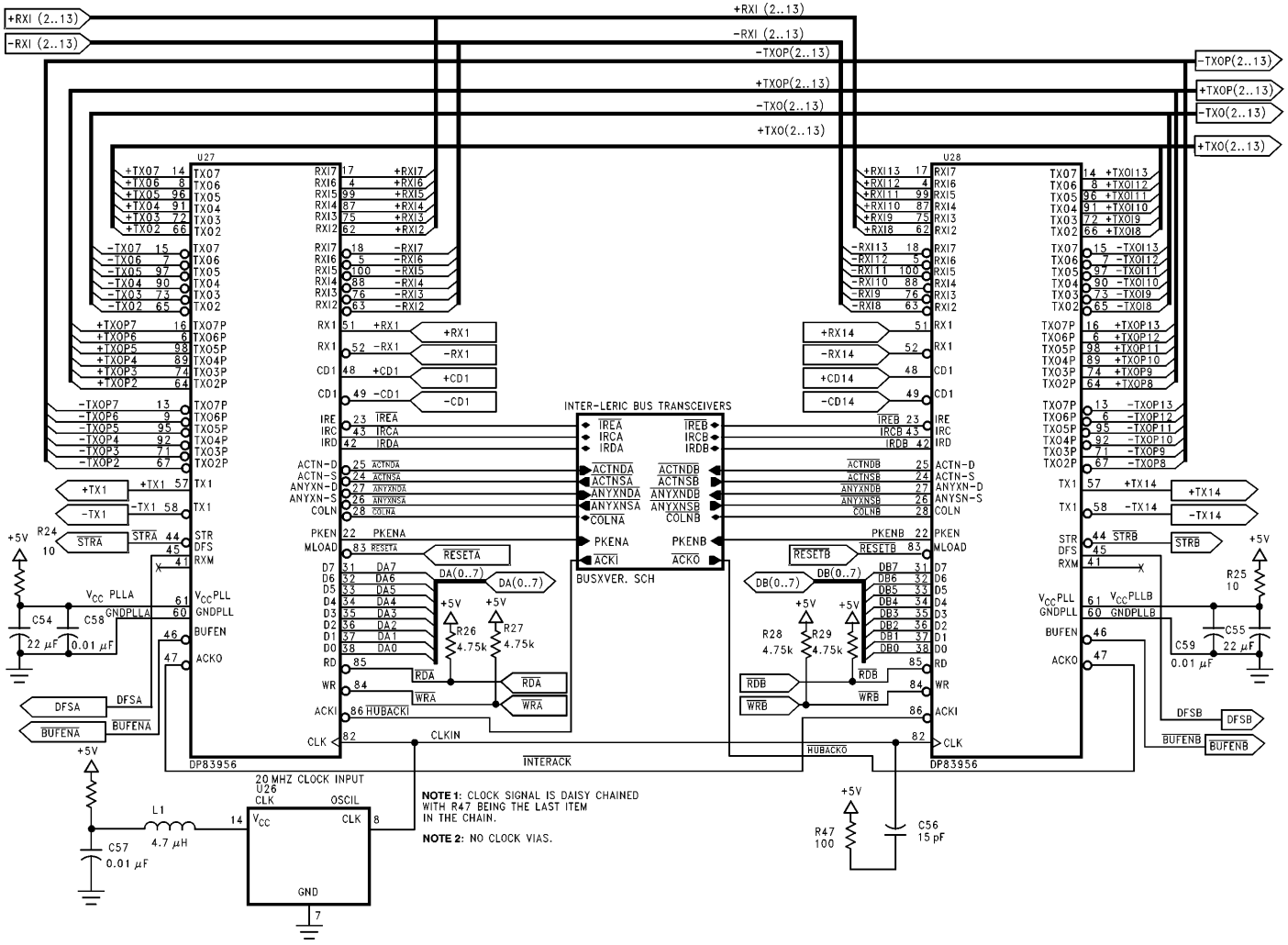

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FIGURE 6. LERIC Connections

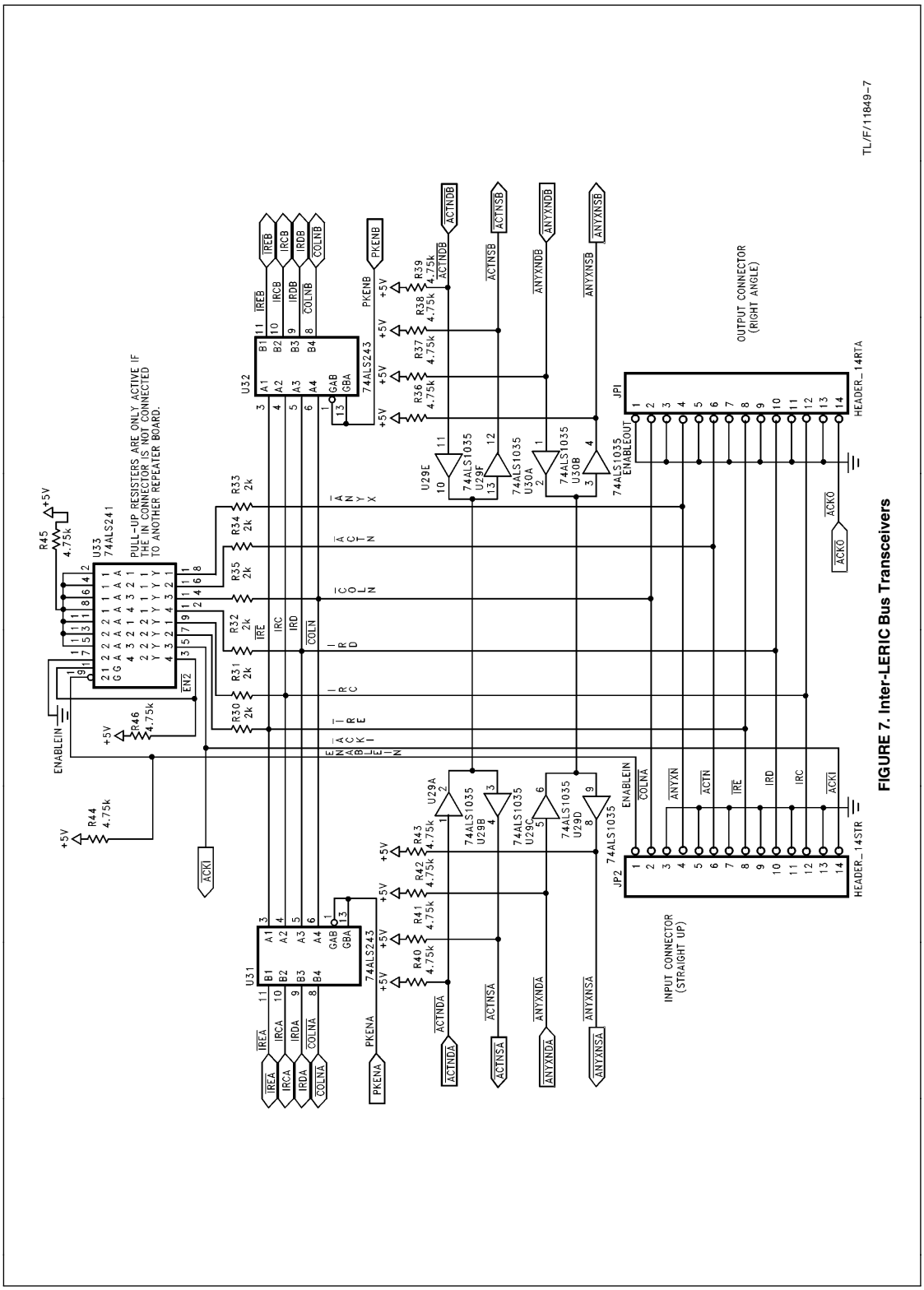

FIGURE 7. Inter-LERIC Bus Transceivers

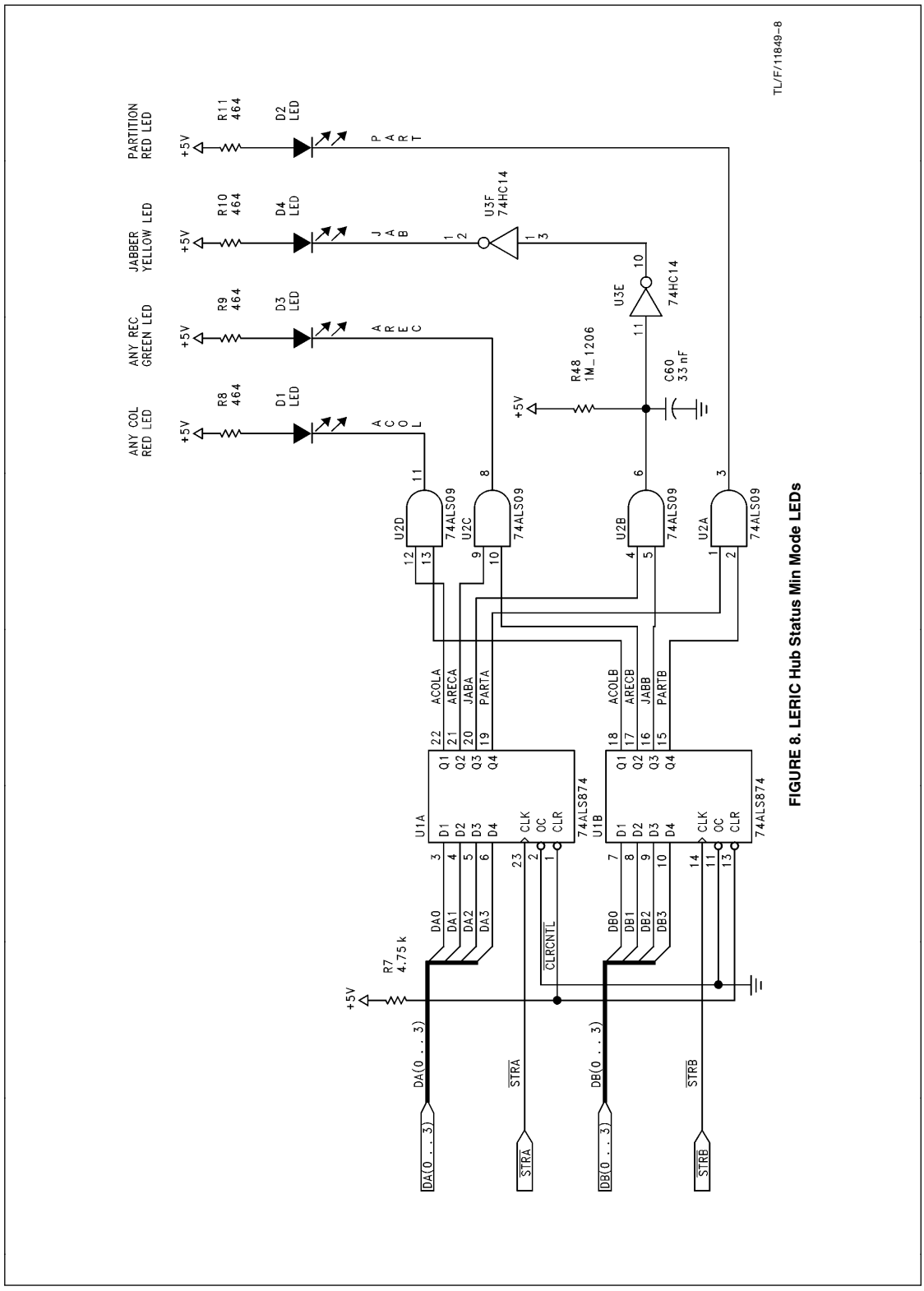

FIGURE 8. LERIC Hub Status Min Mode LEDs

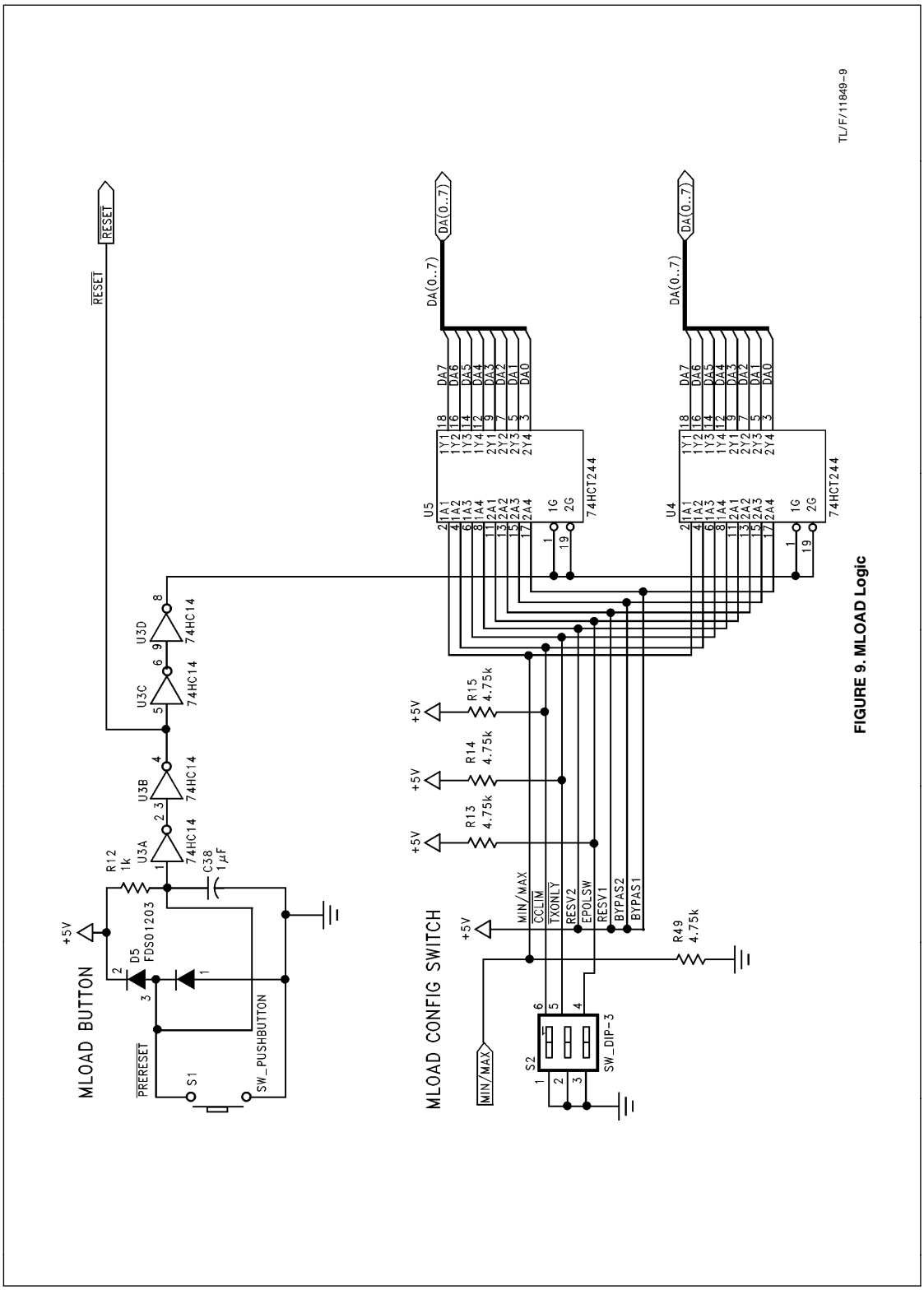

FIGURE 9. MLOAD Logic

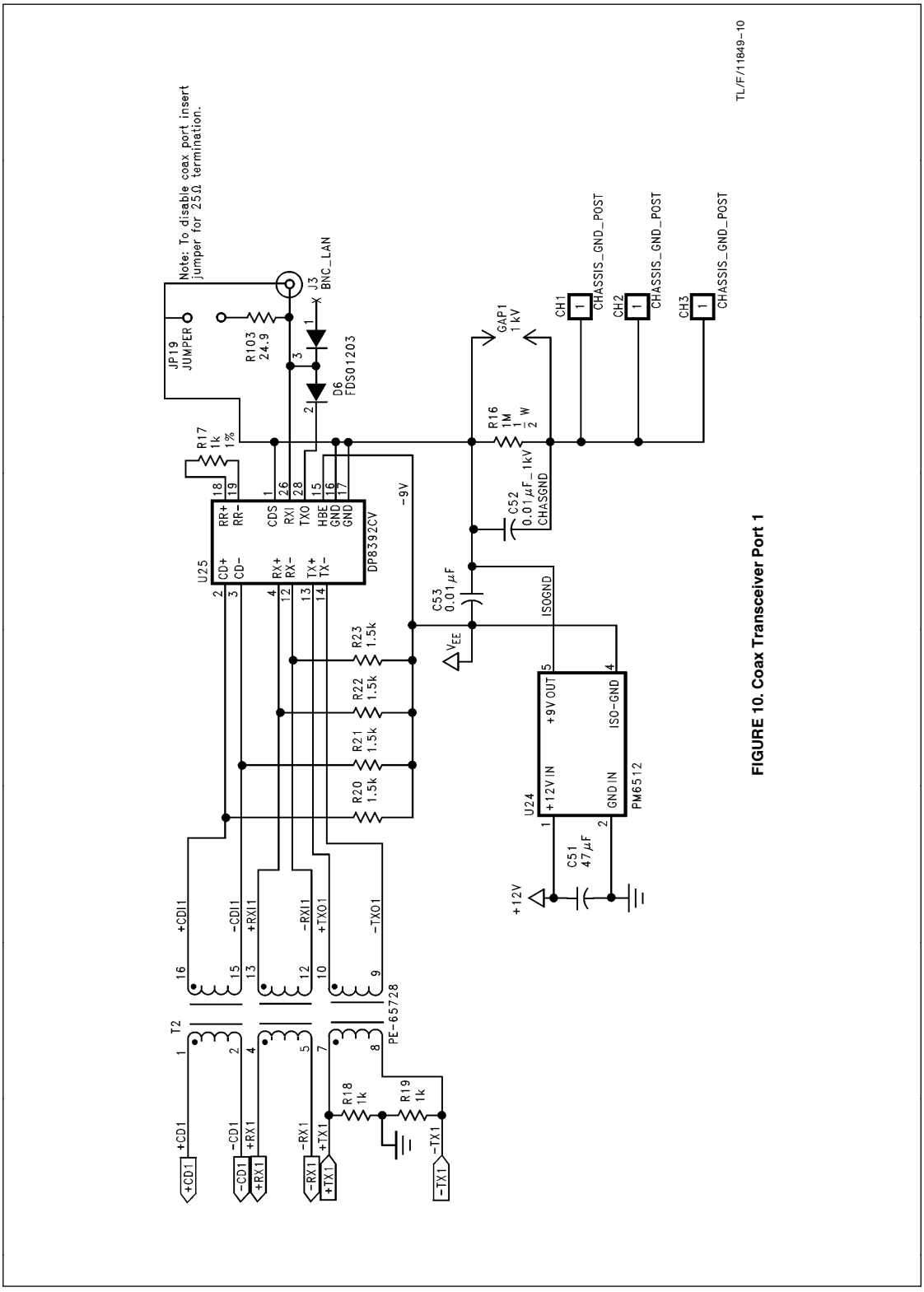

FIGURE 10. Coax Transceiver Port 1

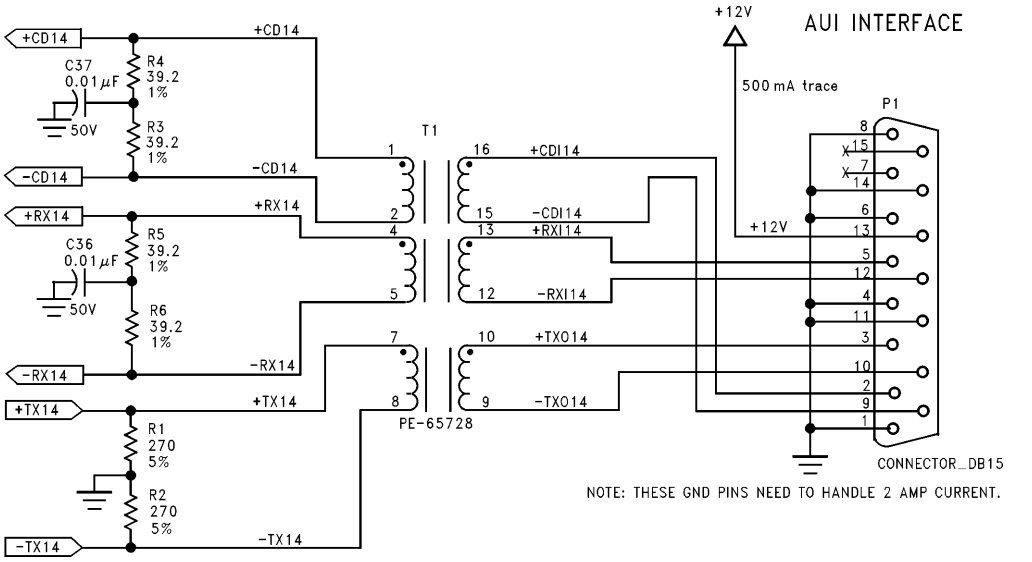

FIGURE 11. Full AUI Port 14

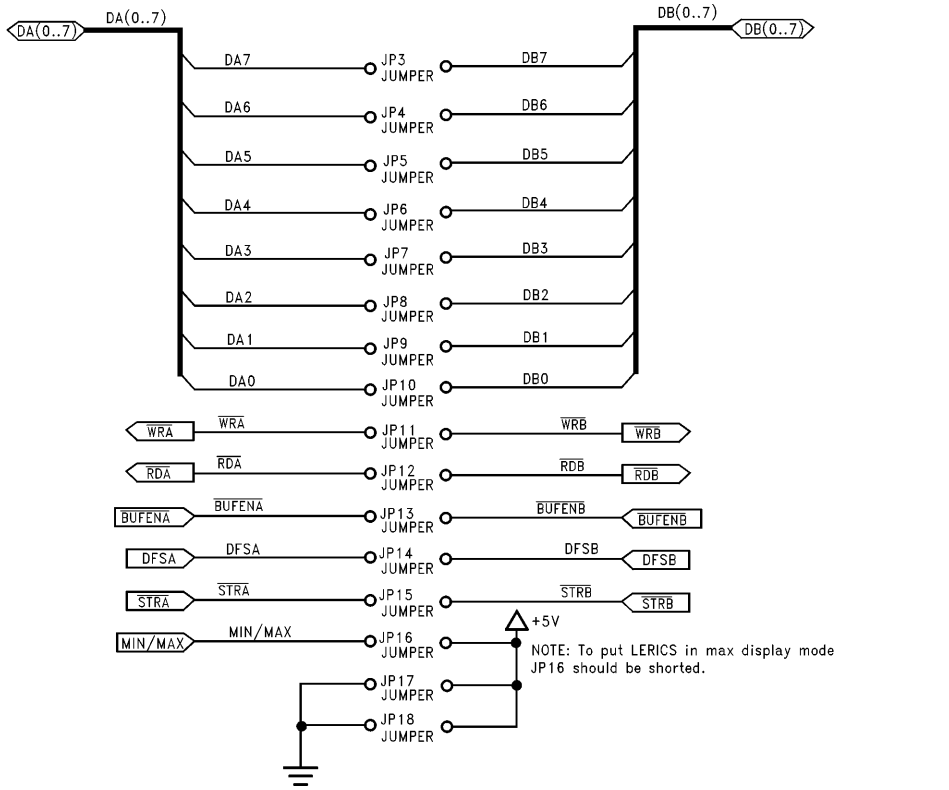

FIGURE 12. LED Status Header

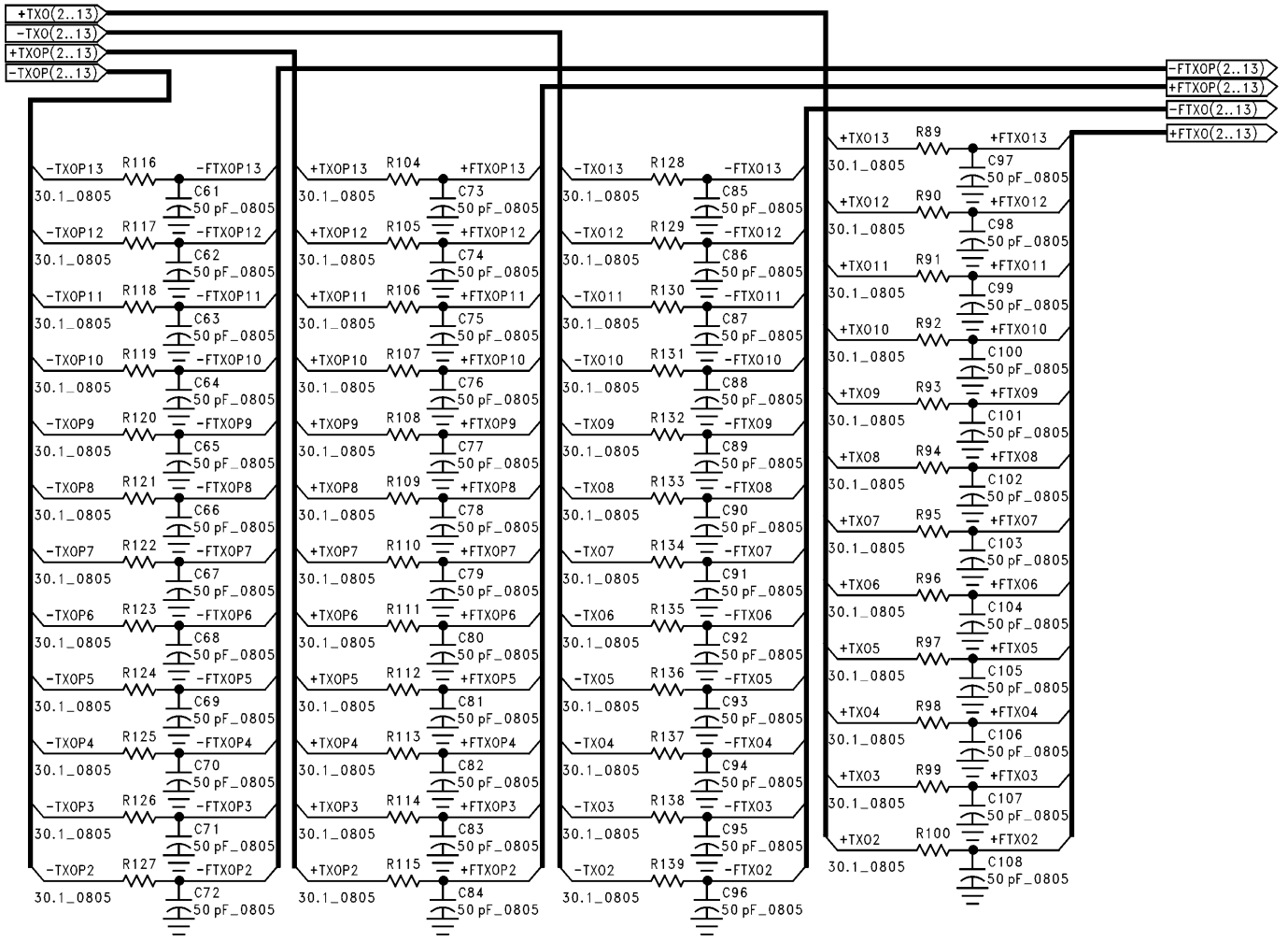

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FIGURE 13.

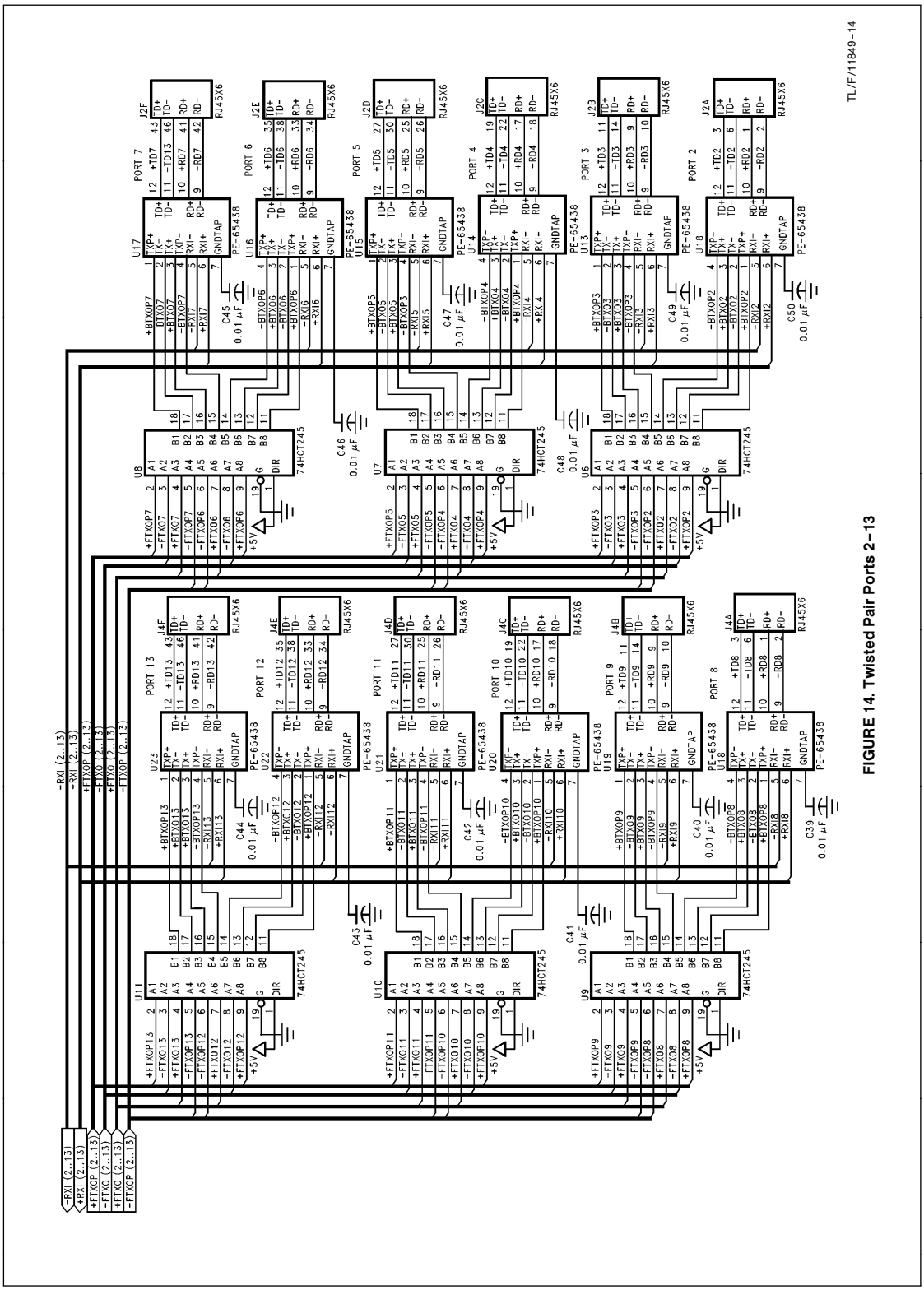

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FIGURE 14. Twisted Pair Ports 2–13

4.0 BILL OF MATERIALS

Item #	Reference (Location)	Description	Manufacturer and Manufacturer Part #	Qty. per Brd.
1	U3	HC Inverter	MM74HC14M	1
2	U33	ALS Line Buffer/Driver Non-Invert	DM74ALS241AWM	1
3	U31, U32	ALS 4X Bus Transceiver— Non-Inverting TRI-STATE	DM74ALS243AM	2
4	U29, U30	ALS Hex Buffer Open Collector	DM74ALS1035M	2
5	U4, U5	HCT 8X Buffer/Driver TRI-STATE	MM74HCT244M	2
6	U6 thru U11	8X Bus Transceiver— Non-Inverting TRI-STATE	MM74HCT245M	6
7	U2	4x2 in AND Gate—Open Collector	DM74ALS09M	1
8	U1	Dual 4X D Latch	DM74ALS874BWM	1
9	U25	Ethernet Coaxial Transceiver, CTI™	DP8392CV	1
10	U27, U28	LERIC—100-Pin	DP83956AVLY	1
11	U34	Voltage Regulator—Variable—Hi Current	LM350T	1
12	U24	12V to 9V Converter	PM6512	1
13	T1, T2	PULSE SMT AUI Transformer	PE-65728	2
14	U12 thru U23	TP Filter, Transformer and Summing Resistors	Valor-FL1085	12
DIODES/LEDS				
15	D5, D6	Rect. 1V Dual SMD SOT 23	FDS1203	2
16	D3	LED Green 3mm, 0.1 sp Diffused	IEE #LL231G	1
17	D1, D2	LED Red 3mm, 0.1 sp Diffused (hi eff.)	IEE #LL221R	2
18	D4	LED Yellow 3mm, 0.1 sp Diffused	IEE #LL251Y	1
CONNECTORS				
19	J3	CONN-BNC Pc/Mt, Low Profile Black	AMP-227161-9	1
20	P1	CONN-DSUB Female 15P w/Solder Tab	AMP-747845-4	1
21	JP2	CONN—14-Pin Header Straight—4 Wall	3M-3598-6002	1
22	JP1	CONN—14-Pin—Right Angle—4 Wall	3M-3598-5002	1
23	Cable Diagram	CONN Receptacle—Center Polarized Female—14 Position	3M #3385 Series	4
24	Cable Diagram	Ribbon Cable—14 Conductor, 28AWG	3M #3539/14	1
25	J1	CONN PWR 2-Pin Angled—Male	AMP—#640389-2	1
26	J2	CONN—RJ45 x 6—6 Port TP Conn Shielded	Stewart #SS-6688065	2
27	JP3 thru JP18	PIN Strip v/mt Brkway 16p 2 Row		1
28	JP19	Pin Strip v/mt Brkway 2p 1 Row		1
29	Assembly Diagram	1 Inch Aluminum Standoff—Hex Shape	Amatom #9743-A-0632	4
29A	Assembly Diagram	NUT #6-32 Hex Std S Steel		4
CAPACITORS				
30	C1 thru C19, C22 thru C25, C27 thru C37, C40 thru C50, C53, C57 thru C59	0.01 μF + 80 − 20 1206 50V C/C/SMD		50
32	C61 thru C108	47 pF ±10% 0805 50V C/C/SMD		48
33	C20, 21, 26, 54, 55	22 μF ±20% 7343 16V C/T/SMD		5

4.0 BILL OF MATERIALS (Continued)

Item #	Reference (Location)	Description	Manufacturer and Manufacturer Part #	Qty. per Brd.
CAPACITORS (Continued)				
34	C51	47 μF ±20% 7343 10V C/T/SMD		1
35	C38	1 μF ±20% 3216 16V C/T/SMD		1
36	C52	0.01 μF Radial ±20% 7343 1 kV		1
37	C56	15 pF ±10% 0805 50V C/C/SMD		1
38	C60	0.33 μF +80/−20 1206 50V C/C/SMD		1
39	GAP1	0.75 pF Spark Gap 1 kV DC		1
MISC				
29B	Assembly Diagram	Lock Washer #6 Ex-Tooth Std		5
29C	Assembly Diagram	Washer #6 Std		9
28A	JP19	Jumper Shunt 2p 1 Row 0.1 0.250 Hi		1
RESISTORS				
40	R3 thru R6	39.2 R 1% 1206 ⅛W R/F/SM		4
41	R8 thru R11	464 R 1% 1206 ⅛W R/F/SM		4
42	R12, R17 thru R19	1.0k R 1% 1206 ⅛W R/F/SM		4
43	R20 thru R23	1.5k R 1% 1206 ⅛W R/F/SM		4
44	R30 thru R35	2.0k R 1% 1206 ⅛W R/F/SM		6
45	R7, R13 thru R15 R26 thru R29 R36 thru 46, R49	4.75k R 1% 1206 ⅛W R/F/SM		20
46	R1, R2	270 R 1% 1206 ⅛W R/F/SM		2
47	R48	1.0M R 5% 1206 ⅛W R/F/SM		1
48	R16	1.0M R 5% ½W Radial Comp		1
49	R24, R25	10 R 1% 1206 ⅛W R/F/SM		2
50	R89 thru R139	30.1 R 1% 0805 R/F/SM		48
51	R101	121 R 1% 1206 ⅛W R/F/SM		1
52	R102	365 R 1% 1206 ⅛W R/F/SM		1
53	R103	24.9 R 1% 1206 ⅛W R/F/SM		1
54	R47	100 R 1% 1206 ⅛W R/F/SM		1

4.0 BILL OF MATERIALS (Continued)

Item #	Reference (Location)	Description	Manufacturer and Manufacturer Part #	Qty. per Brd.
INDUCTORS				
55	L1	4.7 μH/ ±10% 1210 Induct/SMD		1
SWITCHES				
56	S2	DIP Switch—3 Position Rocker Unsealed	AMP-3-435166-0	1
57	S1	Push Button—2 Pole N.O. Momentary	Alco TP11CG-PC-0	1
OSCILLATORS				
58	U26	Crystal 20.0 MHz Osc 100 ppm 14p 4 Conn		1
59	U34B	Screw—6-32 x 0.250 P/Head SS		1
60	U34C	Nut-Hex Std SS		1
61	Assembly Diagram	Std IDT Connector—0.156C Double Cantalever Contact Crimp Style Contact	MOLEX: 09-06-5027	1
62	Stancor	Power Supply—Wall Mnt. AC Adaptor +12 @1A Unregulated Plug Compatible: Switchcraft #PC-722A	Stancor: STA-4812A	1

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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