Battery Operation of the INA-03184

Application Note 1071

Introduction

The recent proliferation of “wireless” applications at RF and low microwave frequencies has created a demand for integrated circuits (ICs) that can be powered by batteries. One such device is Hewlett- Packard’s INA-03184 Gain Block.

Common single cell batteries produce a nominal 1.2 volts, which reduces to 1.0 - 1.1 volts when regulated, and further decreases to 0.9 volts at end of life. Systems typically use either 3, 4, or 5 cells as the power supply. Thus the voltages of interest for many new systems are as shown in Table 1. This Application Note characterizes the performance of the INA-03184 Gain Block at these supply voltages.

Table 1. Supply Voltage vs. Number of Battery Cells.

	Number of cells		
	3	**4**	**5**
V nom. (V)	3.6	4.8	6.0
V reg. (V)	3.0	4.0	5.0
V min. (V)	2.7	3.6	4.5

5 Cell Operation

A 5 cell power supply will result in a nominal 5.0 V bias rail. Conventional biasing of the INA-03184 uses a resistor to drop the 5.0 V of the regulated supply line (V_{ps}) to a 4.0 V nominal device voltage (V_d) on the output terminal of the RFIC. The proper value for the resistor (R) can be calculated using the bias current (I_d) and the voltage drop:

$$R = [V_{ps} - V_d]/I_d \qquad (1)$$

From the data sheet,

$V_d = 4.0$ V
$I_d = 10$ mA

so for a 5 V power supply,
R = [5.0 V - 4.0 V] / 10 mA
= 100 Ω.

Since 100 Ω is not large compared to the 50 Ω AC load, a high-valued inductor (e.g., a 1 µH chip inductor) needs to be added in series with R to prevent the bias circuit from loading the output of the RFIC. The circuit board layout is as shown in Figure 1. See AN-S012 for the derivation of this design.

Performance of this board is shown in the following diagrams. Figure 2 plots gain versus frequency; Figure 3 shows input and output VSWR. Output power at 1 dB compressed gain and input third order intercept point are listed versus frequency in Table 2. The circuit is usable for applications from low RF through the 2.4 GHz Industrial-Scientific-Medical (ISM) band.

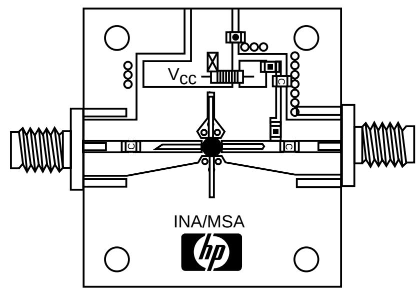

Figure 1. Circuit Board.

An interesting option with this circuit is to omit the high-valued inductor and allow the 100 Ω bias resistor to load the RFIC output. A high-valued capacitor (1000 pF typ.) needs to be added to the power supply side of the bias resistor R to provide a good AC ground. The resulting circuit will have improved output VSWR and stability, but at the cost of about 2.5 dB in both gain and output power. Figure 4 shows the gain performance of this amplifier; Figure 5 the input and output

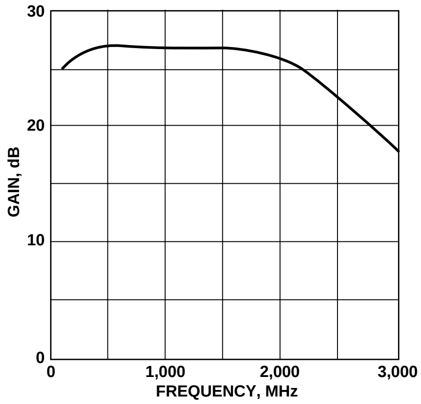

Figure 2. Gain vs. Frequency for V_{ps} = 5 V, R = 100 Ω.

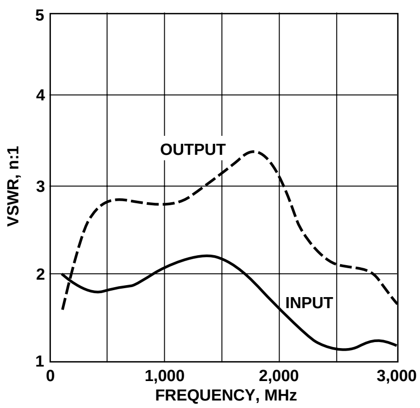

Figure 3. VSWR vs. Frequency for V_{ps} = 5 V, R = 100 Ω.

Table 2. P_{1dB} and Input IP3 for V_{ps} = 5 V, R = 100 Ω.

Freq. (GHz)	I_d (mA)	P_{1dB} (dBm)	$I_{P3\ i}$ (dBm)
0.9	10.0	+1.0	-16
1.9	10.0	-5.5	-20

VSWR. Table 3 gives power and intercept point information.

A third option is to omit the bias resistor and bias the INA-03184 at 5.0 volts. A choke will be needed (again 1 µH typ.) to prevent the bias from loading the output. The higher bias voltage will result in higher output power and 3 to 4 dB more gain. Stability and match are adversely affected; however, the resulting amplifier is only condi-

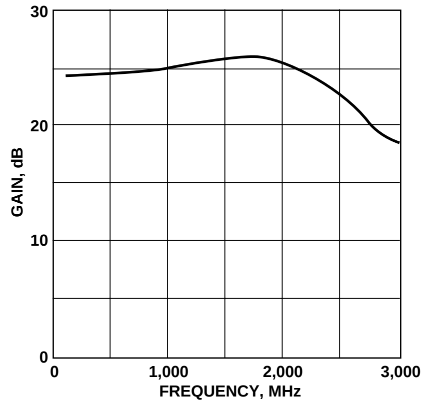

Figure 4. Gain vs. Frequency for V_{ps} = 5 V, R = 100 Ω, no choke.

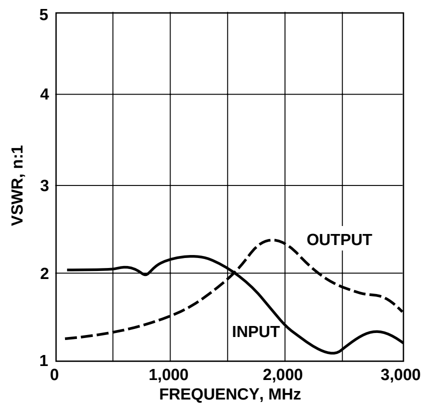

Figure 5. VSWR vs. Frequency for V_{ps} = 5 V, R = 100 Ω, no choke.

Table 3. P_{1dB} and Input IP3 for V_{ps} = 5 V, R = 100 Ω no choke.

Freq. (GHz)	I_d (mA)	P_{1dB} (dBm)	$I_{P3\ i}$ (dBm)
0.9	10.0	-1	-16
1.9	10.0	-7	-23

tionally stable from 900 MHz to 2.4 GHz and has a significantly degraded input match below 2 GHz. Gain versus frequency for this configuration is shown in Figure 6. VSWRs are shown in Figure 7. Power information is in Table 4. For reference, 5 V s-parameters for the INA-03184 are included in Appendix 1. Because of the reduced stability, this variation should be used with care.

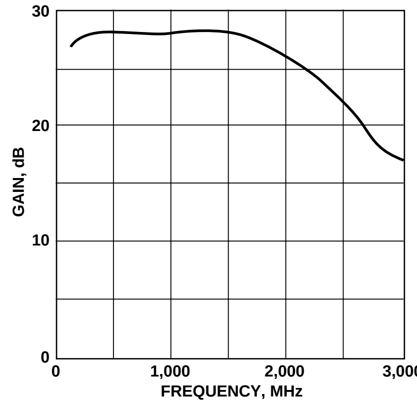

Figure 6. Gain vs. Frequency for V_{ps} = 5 V, R = 0 Ω.

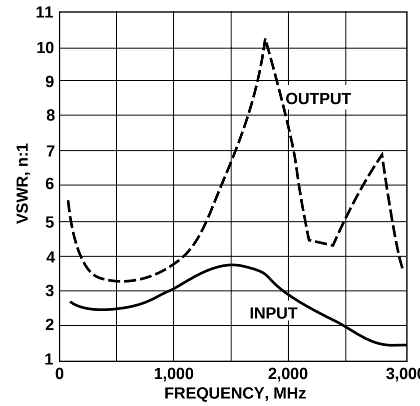

Figure 7. VSWR vs. Frequency for V_{ps} = 5 V, R = 0 Ω.

Table 4. P_{1dB} and Input IP3 for V_{ps} = 5 V, R = 0 Ω.

Freq. (GHz)	I_d (mA)	P_{1dB} (dBm)	$I_{P3\ i}$ (dBm)
0.9	11.9	+2.5	-15
1.9	11.9	-5	-21

Note that this variation is voltage-controlled. Measurements have shown that bias stability is approximately equal for both voltage-controlled and current-controlled biasing of the INA family of ICs. In general the variation in gain over a -25 to +85°C temperature range will be less than 2 dB for either implementation (see AN-S012, pg. 12).

4 Cell Operation

A 4 cell power supply will result in a nominal 4.0 V bias rail. Since 4.0 V is the nominal device voltage of the INA-03184, the most common biasing scheme would be to use a bias choke and omit the bias resistor. The resulting voltage controlled amplifier is physically identical to the third 5 V option discussed above, and has the performance shown in Figures 8 and 9. Power performance is as shown in Table 5. The 4.0 V s-parameters correspond to the 10 mA data in the catalog. Except for output match, this amplifier has very similar performance to that of the 5 V amplifier which used a 1 µH choke and R = 100 Ω.

It is also possible to use a bias resistor from the 4 V rail, and operate the INA-03184 below its normal operating current. For example, the 100 Ω bias resistor circuit discussed above would result in a device current of 8 mA, and have the performance shown in Figures 10 and 11 and Table 6. Operation at device currents below 7 mA is not recommended, as they can result in significant performance variations either over temperature or from device to device. The reduced bias current improves the match and stability of this amplifier when compared to standard 10 mA operation, but at the cost of about 1 dB of gain and reduced output power.

If the choke is omitted from this amplifier, then a very well matched structure results. This amplifier also has the best stability of any of the variations discussed in this note. Gain is approximately 3.5 dB less than the 10 mA bias version, and output power is similarly reduced. Figures 12 and 13 show gain and match performance, while Table 7 shows power performance.

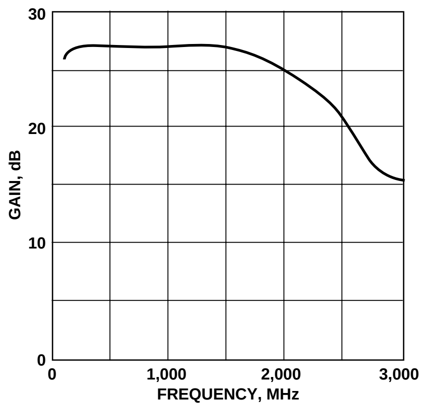

Figure 8. Gain vs. Frequency for V_{ps} = 4 V, R = 0 Ω.

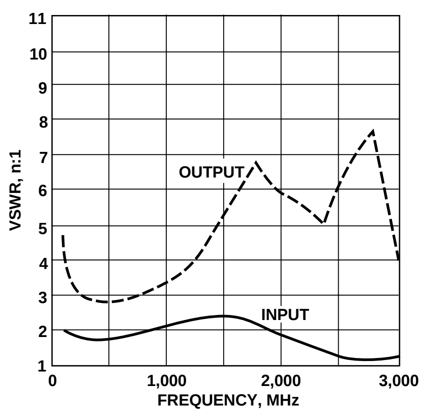

Figure 9. VSWR vs. Frequency for V_{ps} = 4 V, R = 0 Ω.

Table 5. P_{1dB} and Input IP3 for V_{ps} = 4 V, R = 0 Ω.

Freq. (GHz)	I_d (mA)	P_{1dB} (dBm)	$I_{P3\ i}$ (dBm)
0.9	10.0	-1	-18
1.9	10.0	-7	-22

3 Cell Operation

A 3 cell power supply will result in a nominal 3.0 V power supply. A V_d of 3.0 V will result in an I_d of 7.5 mA. This is on the low end of the recommended bias window. Since there is no voltage "headroom" to give up in the bias circuit, the best option available is a voltage controlled amplifier biased through a choke inductor (1 µH typ.). This circuit has the performance shown in Figures 12 and 13. The reduced bias current reduces device gain only slightly (about 1 dB typ.) but improves the input match.

For design purposes, 3 V s-parameters are shown in Appendix 2.

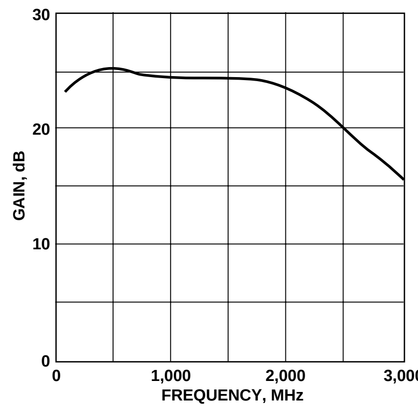

Figure 10. Gain vs. Frequency for V_{ps} = 4 V, R = 100 Ω.

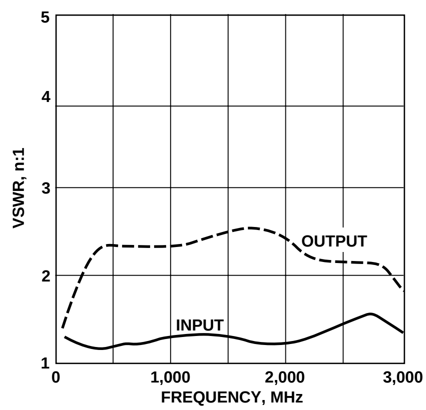

Figure 11. VSWR vs. Frequency for V_{ps} = 4 V, R = 100 Ω.

Table 6. P_{1dB} and Input IP3 for V_{ps} = 4 V, R = 100 Ω.

Freq. (GHz)	I_d (mA)	P_{1dB} (dBm)	$I_{P3\ i}$ (dBm)
0.9	8.2	-1.5	-17
1.9	8.2	-6.5	-21

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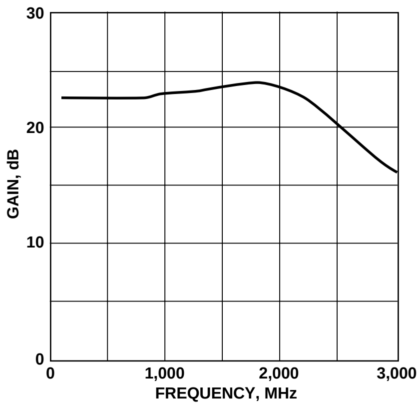

Figure 12. Gain vs. Frequency for V_{ps} = 4 V, R = 100 Ω, no choke.

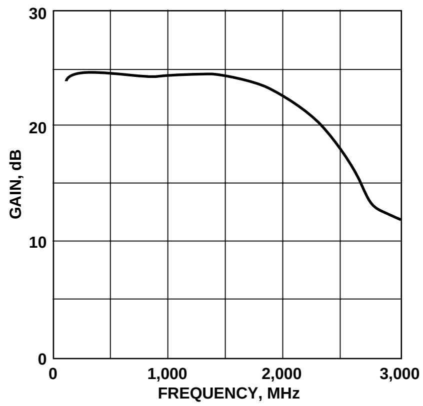

Figure 14. Gain vs. Frequency for V_{ps} = 3 V, R = 0 Ω.

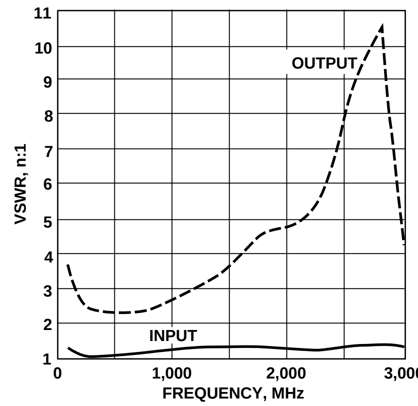

Figure 15. VSWR vs. Frequency for V_{ps} = 3 V, R = 0 Ω.

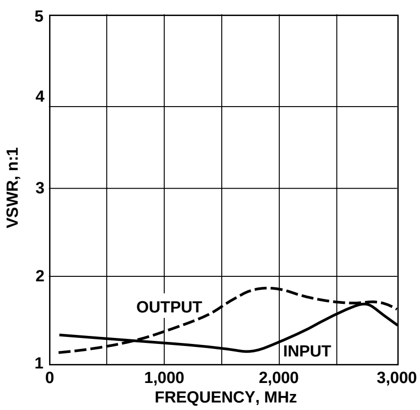

Figure 13. VSWR vs. Frequency for V_{ps} = 4 V, R = 100 Ω, no choke.

Table 7. P_{1dB} and Input IP3 for V_{ps} = 4 V, R = 100 Ω no choke.

Freq. (GHz)	I_d (mA)	P_{1dB} (dBm)	$I_{P3\,i}$ (dBm)
0.9	8.2	-3.5	-17
1.9	8.2	-8.5	-23

Table 8. P_{1dB} and Input IP3 for V_{ps} = 3 V, R = 0 Ω.

Freq. (GHz)	I_d (mA)	P_{1dB} (dBm)	$I_{P3\,i}$ (dBm)
0.9	7.9	-1.5	-16
1.9	7.9	-6.5	-20

Appendix 1. INA-03184 S-Parameters at 5.0 V (11.9 mA)

Freq.	S11		S21		S12		S22	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.1	.42	178	25.07	-7	.013	4	.59	-3
0.5	.44	166	25.20	-34	.010	10	.55	-13
0.7	.47	159	25.69	-47	.013	25	.54	-17
0.9	.50	151	26.25	-62	.014	50	.54	-22
1.0	.52	147	26.46	-69	.013	46	.54	-24
1.2	.56	136	27.76	-85	.017	44	.54	-30
1.5	.61	116	29.33	-114	.022	56	.50	-44
1.8	.59	91	27.70	-147	.028	60	.37	-57
2.0	.47	72	25.00	-166	.029	51	.33	-51
2.4	.27	62	18.61	152	.033	50	.18	-45
3.0	.21	88	9.90	115	.031	56	.19	-23

Appendix 2. INA-03184 S-parameters at 3.0 V (7.9 mA)

Freq.	S11		S21		S12		S22	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.1	.01	-171	17.17	-8	.024	-1	.42	-2
0.5	.02	-148	17.10	-37	.019	7	.40	-7
0.7	.03	-147	17.14	-51	.018	13	.39	-9
0.9	.05	-161	17.38	-67	.017	7	.39	-13
1.0	.06	-174	17.45	-75	.020	17	.40	-14
1.2	.07	-180	17.77	-91	.020	25	.39	-17
1.5	.08	167	17.92	-119	.019	28	.36	-23
1.8	.07	156	16.56	-150	.024	40	.30	-25
2.0	.04	-164	15.00	-168	.024	40	.32	-20
2.4	.16	-177	11.34	154	.024	43	.29	-21
3.0	.25	148	6.39	117	.025	50	.29	-24

www.hp.com/go/rf

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