CHAPTER 9

LOW-FREQUENCY AMPLIFIERS WITH STABILIZED GAIN

9·1. Problems Characteristic of Computer Amplifiers.—The design of many electronic computing devices involves the representation of functions by the magnitudes of alternating voltages. In these computers, amplifiers are needed either to transform the output and input impedances of the different computing elements within the device or as computing elements themselves. They can be used for the latter purpose for example, to multiply a particular function by an arbitrary and sometimes variable factor.

The gain of such an amplifier must be held constant within closely prescribed limits regardless of the variability of vacuum-tube parameters, the manufacturing tolerances of passive components such as resistors and capacitors, possible variations of the ambient temperature, etc. The variation in gain that can be tolerated depends upon the desired accuracy of computation (the figure of ± 0.1 per cent was usually specified by the Radiation Laboratory).

Economy requires that the desired constancy of gain be achieved without using circuit components whose characteristics must themselves be maintained within narrow tolerances. The specified tolerances for resistors and condensers, for instance, are usually not narrower than 5 and 10 per cent respectively, although in some obvious cases resistance values must be more closely specified.

Inverse feedback can be employed to render the gain of computer amplifiers less sensitive to the variations in the values of the circuit parameters. Variations in gain due to changes in tube parameters can be reduced by local feedback methods such as the use of unbypassed cathode resistors or d-c feedback from plate to grid (see Chap. 3). The principal design problems, then, derive from the fact that the feedback circuit requires high gain, which tends to make the amplifier oscillate at frequencies often far removed from the frequency band that it is designed to amplify.[1]

The decision as to the number of stages of amplification necessary to obtain the desired reduction of gain sensitivity to component variability is determined not only by the general requirements of the system but also by the tolerances of the circuit components, the gain attainable from each stage, the bandpass requirements set by the feedback circuit, and the polarity of feedback, which determines for certain feedback circuits whether the number of stages should be even or odd.

The following criteria determine the choice of the particular feedback circuit:

1. The fraction β of the output signal which is to be fed back at the computing frequency must be maintained within the prescribed tolerance.
2. The circuit shall require the minimum number of precision components (e.g., ± 1 per cent resistors).
3. Preferably there should be no need for an amplitude control to compensate for the variability of any of the components used in the amplifier; if such a control is necessary, its required range of adjustment should be kept small in order to minimize effects of maladjustment.
4. The feedback circuit used should cause the amplifier to have the desired input and output impedances.

The choice of feedback methods for computer amplifiers is more restricted than for audio amplifiers or for most filter amplifiers because of the small permissible variability of β; the feedback circuit therefore cannot usually involve tubes. The simplest type of feedback circuit satisfying this requirement is that for which $|\beta| = 1$, that is, a circuit in which the output voltage may either be subtracted from the input voltage and the difference applied to the first grid or be applied directly to the first cathode. Possible subtracting methods include resistive mixing (with an odd number of stages) and subtraction of output voltage from input voltage by means of a transformer. Feedback to the first cathode is most easily accomplished when the load is inductive; if the load is resistive, cathode feedback can be accomplished by the use of an auxiliary inductance to provide a d-c return for the first cathode, or by the use of a transformer. By modifications of these methods, any desired fraction of the output voltage can be fed back to the input terminals: In Circuit *a* of Fig. 9·1 (resistive mixing) the resistors R_1 and R_2 can be varied; in Circuit *b* the transformer T can be designed to have any desired ratio, or a potentiometer can be incorporated so as to add a variable fraction of the output voltage to the input voltage; in Circuits *c* and *d* an extra tap can be designed into the inductance or transformer. For relatively low-precision applications, each of these circuits can be reduced to a single-stage amplifier: Circuit *c* will simply become a cathode follower if the amplifier "box" is made an open circuit; in other cases the amplifier is made a short-circuit or zero-stage amplifier.

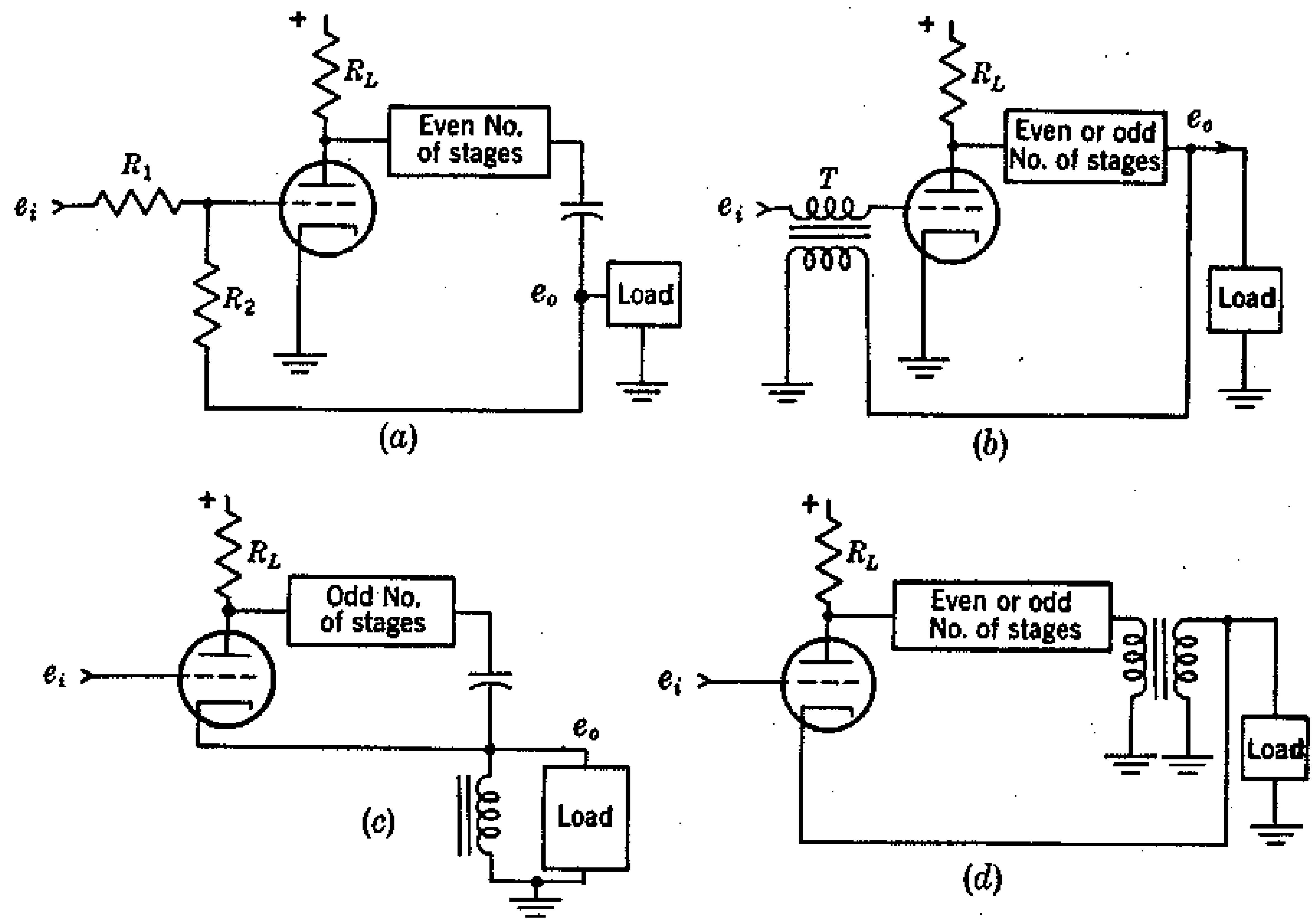

FIG. 9·1.—Feedback circuits. (*a*) Resistive mixing at grid; (*b*) transformer subtraction at grid; (*c*) cathode feedback with auxiliary inductance; (*d*) cathode feedback with transformer.

9·2. Analysis of Types of Feedback. *Resistive Mixing.*—In the analysis of the resistive-mixing type of feedback circuit (Fig. 9·1*a*), it is assumed that the source is a generator of voltage e_i having an output impedance Z_s, that the amplifier can be replaced by a generator $-\alpha e_g$ having an output impedance Z_0 in the absence of feedback, and that the first-stage grid is connected to ground through an impedance Z_g (Fig. 9·2). The gain and the output impedance of this circuit can be calculated by writing the circuit equations with e_i and i as the two independent variables. The gain will then be $\partial e_0/\partial e_i$ and the output impedance will be $\partial e_0/\partial i$. Because the equations are linear, these quantities are respectively $(e_0/e_i)_{i=0}$ and $(e_0/i)_{e_i=0}$. Using nodal equations,

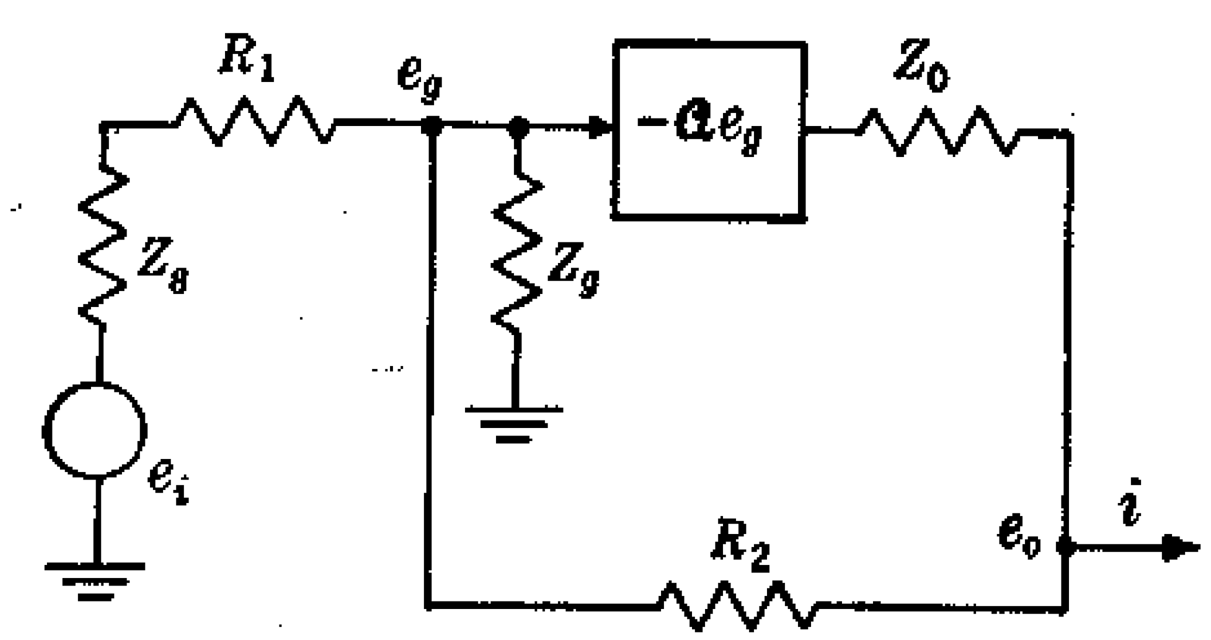

FIG. 9·2.—Schematic circuit for resistive-mixing feedback.

$$-\left(\frac{1}{R_2}\right)e_0 + \left(\frac{1}{R_1 + Z_s} + \frac{1}{R_2} + \frac{1}{Z_g}\right)e_g = \frac{e_i}{R_1 + Z_s}, \qquad (1a)$$

and

$$\left(\frac{1}{R_2} + \frac{1}{Z_0}\right) e_0 - \left(\frac{1}{R_2} - \frac{\mathcal{a}}{Z_0}\right) e_g = i. \tag{1b}$$

Then the voltage gain is

$$\mathcal{G} = \left(\frac{e_0}{e_i}\right)_{i=0} = \frac{(-\mathcal{a}R_2 + Z_0)}{(1 + \mathcal{a})(R_1 + Z_s) + \left[\frac{(R_1 + Z_s)}{Z_g} + 1\right](R_2 + Z_0)}. \tag{2}$$

Now if

$$Z_g \geqq R_1 + Z_s,$$
$$R_2 + Z_0 \leqq R_1 + Z_s,$$

and $\mathcal{a} \gg 1$,

$$\mathcal{G} = \frac{-\mathcal{a}R_2 + Z_0}{\mathcal{a}(R_1 + Z_s)} = -\frac{R_2}{R_1 + Z_s} + \frac{Z_0}{\mathcal{a}(R_1 + Z_s)}. \tag{3}$$

But usually $R_1 + Z_s \geqq Z_0$; and since $\mathcal{a} \gg 1$, Eq. (3) becomes, to a very good approximation,

$$\mathcal{G} = -\frac{R_2}{R_1 + Z_s}.$$

Then

$$\frac{d\mathcal{G}}{\mathcal{G}} = \frac{-dR_2}{R_2} + \frac{dR_1}{R_1}\left(\frac{R_1}{R_1 + Z_s}\right) + \frac{dZ_s}{Z_s}\left(\frac{Z_s}{R_1 + Z_s}\right), \tag{4}$$

which makes it evident that in order for variations in source impedance to have little effect on the gain of the amplifier, Z_s must be very much less than R_1; thereupon fractional variations in R_1 and R_2 affect the gain equally.

The output impedance is given by the following equation:

$$Z_{\text{out}} = \left(\frac{e_0}{i}\right)_{e_i=0} = \frac{\left(\frac{1}{R_1 + Z_s} + \frac{1}{R_2} + \frac{1}{Z_g}\right)}{\left(\frac{1}{R_2} + \frac{1}{Z_0}\right)\left(\frac{1}{R_1 + Z_s} + \frac{1}{R_2} + \frac{1}{Z_g}\right) - \frac{1}{R_2}\left(\frac{1}{R_2} - \frac{\mathcal{a}}{Z_0}\right)}. \tag{5}$$

As $\mathcal{a}$ grows indefinitely, and if

$$Z_s \ll R_1,$$
$$Z_g \gg R_1,$$
$$Z_{\text{out}} \approx \frac{(R_1 + R_2)Z_0}{\mathcal{a}R_1}, \tag{6}$$

which is simply Z_0 divided by the loop gain. A reduction of output impedance is a general property of voltage-feedback amplifiers.

Cathode Feedback.—When cathode feedback is used, the sensitivity of the over-all gain $\mathcal{G}$ to the μ of the first stage cannot be made appreciably less than $1/\mu$, i.e., $d \ln \mathcal{G}/d \ln \mu \geqq 1/\mu$. To prove this, assume the operating characteristics of the first stage of the amplifier shown in Fig. 9·1c to be given by the usual relation

$$i_p = g_m\left(e_{gk} + \frac{e_{pk}}{\mu}\right) \tag{7}$$

and the remaining stages to have a gain of $-\mathcal{G}_b$. Then

$$e_{pk} = -R_L i_p - e_k, \tag{8a}$$

where e_{pk} = a-c plate-to-cathode voltage,
e_k = a-c cathode-to-ground voltage;

$$e_{gk} = e_i - e_k, \tag{8b}$$

where e_{gk} = a-c grid-to-cathode voltage,
e_i = input signal voltage;

$$e_k = \beta e_0 = \beta R_L i_p \mathcal{G}_b, \tag{8c}$$

where e_0 = output signal voltage,
β = feedback ratio,
R_L = first-stage load resistance.

Combining Eqs. (8) with Eq. (7),

$$e_i = i_p\left[\frac{1}{g_m} + \frac{R_L}{\mu} + \beta R_L \mathcal{G}_b\left(1 + \frac{1}{\mu}\right)\right].$$

But the over-all gain is given by

$$\mathcal{G} = \frac{e_0}{e_i} = \frac{R_L i_p \mathcal{G}_b}{e_i},$$

and therefore,

$$\frac{1}{\mathcal{G}} = \frac{e_i}{R_L i_p \mathcal{G}_b} = \frac{1}{g_m R_2 \mathcal{G}_o} + \frac{1}{\mu \mathcal{G}_b} + \beta\left(1 + \frac{1}{\mu}\right). \tag{9}$$

Now $\mathcal{G}_b$ will ordinarily be made very large in order to render the effect of component variations on $\mathcal{G}$ negligible. In this case Eq. (9) may be written as

$$\frac{1}{\mathcal{G}} = +\beta\left(1 + \frac{1}{\mu}\right) \tag{10}$$

Inverting and differentiating, it is found that $d\mathcal{G}/d\mu = 1/\beta(1 + \mu)^2$; hence

$$\frac{d \ln \mathcal{G}}{d \ln \mu} = \frac{\mu}{\mathcal{G}}\frac{d\mathcal{G}}{d\mu} = \frac{\mu}{\beta\mathcal{G}(1 + \mu)^2}. \tag{11}$$

It is evident that this expression becomes smaller as μ becomes larger; now if μ is large, $\mu \approx \mu + 1$. Then from Eq. (10) $\mathcal{G} \approx 1/\beta$, where $\mathcal{G}$ is the over-all gain. Substituting these approximations in Eq. (11) and noting the conditions under which they are made,

$$\frac{d \ln \mathcal{G}}{d \ln \mu} \geqq \frac{1}{\mu}. \tag{12}$$

Therefore, in order that the gain may be protected against variations of the amplification factor of the first stage, the latter must be as large as possible.

The input impedance of a cathode-feedback amplifier can be calculated with the aid of the preceding analysis. The predominant contribution to the input impedance is that resulting from capacitive coupling of the grid to the plate and cathode. The input impedance is defined as the ratio of grid voltage to total current flowing to the grid node. The total current is the sum of the currents in the capacitances C_{gp} and C_{gk}. These currents are determined by the alternating voltages at the plate and cathode as well as by the input voltage e_i. The voltage differences e_{gp} and e_{gk} have the effect of changing the apparent input capacitance; since the currents in the two branches are in parallel, it is possible to write

$$C_{in} = C_{gp}\frac{e_{gp}}{e_i} + C_{gk}\frac{e_{gk}}{e_i}. \tag{13}$$

Now

$$e_{gp} = e_g - e_p = e_i - e_p,$$

since $e_i = e_g$ by definition. Then

$$\frac{e_{gp}}{e_i} = 1 - \frac{e_p}{e_i}.$$

But

$$e_0 = e_i\mathcal{G} = -e_p\mathcal{G}_b,$$

whence

$$\frac{e_{gp}}{e_i} = 1 + \frac{\mathcal{G}}{\mathcal{G}_b},$$

where $\mathcal{G}$ and $\mathcal{G}_b$ are related by Eq. (9). Similarly

$$e_{gk} = e_g - e_k = e_i - e_k,$$

and

$$\frac{e_{gk}}{e_i} = 1 - \frac{e_k}{e_i} = 1 - \beta\mathcal{G},$$

since $e_k = \beta\mathcal{G}e_i$. Therefore,

$$C_{in} = C_{gp}\left(1 + \frac{\mathcal{G}}{\mathcal{G}_b}\right) + C_{gk}(1 - \beta\mathcal{G}). \tag{14}$$

In deriving Eq. (12) it was assumed that $\mathcal{G}_b \gg 1$, from which it followed that $\beta\mathcal{G} \approx 1$. Because this is an inverse-feedback amplifier, $\mathcal{G}_b > \mathcal{G}$. Moreover, if $\mathcal{G}_b \gg \mathcal{G}$, then

$$C_{in} = C_{gp}. \tag{15}$$

Comparison of Grid and Cathode Feedback.—Certain distinctions may be made between grid and cathode feedback. If the load is resistive, the method shown in Fig. 9·1*a* of resistive mixing at the grid has the advantage of light weight, for it requires no additional iron-core parts. The input impedance is nearly equal to R_1 because the high gain of the amplifier requires that the alternating voltage applied to the first grid remain small. On the other hand, the input impedance of the circuit in Fig. 9·1*b* will be approximately equal to the impedance of the inter-winding capacitance of the transformer. The input capacitances of the circuits in Figs. 9·1*c* and 9·1*d* are low, approximately equal to C_{gp}. The output impedance of each of these circuits is roughly equal to the output impedance of the output stage divided by the loop gain.

If the load is an inductance, Method *c* of Fig. 9·1 is probably preferable to Method *a* because precision resistors are not required. Circuits *b* and *d* have an advantage from the standpoint of low power drain on the output stage, because the use of a transformer makes possible push-pull operation, with a corresponding increase in efficiency.

9·3. The Stability Problem.—Certain phase and amplitude requirements must be satisfied by a feedback amplifier in order that it shall not oscillate. These requirements give rise to the problem of synthesizing networks that possess special characteristics, subject to practical limitations imposed by the resistances, condensers, tubes, and wiring. At sufficiently low frequencies a 90° phase lead is introduced by each coupling capacitor and the associated grid resistor; at high frequencies a 90° lag is associated with each stage, determined by its input capacitance and the output resistance of the preceding stage. The design objective is to cause the loop gain $\alpha\beta$ to decrease to less than unity at frequencies between which the phase shift does not exceed 180°. For a one-stage amplifier the problem is not difficult unless there are elements in the circuit producing a phase shift of 180° or more (such as a transformer plus a coupling capacitor). The two-stage amplifiers that can be made from the feedback circuits of Figs. 9·1*b* and 9·1*d* involve transformers that may introduce 180° phase shift at high frequencies; if the circuit of Fig. 9·1*c* is used, there are also two coupling networks affecting the low-frequency response. Three-stage *RC*-coupled amplifiers involve at least three coupling networks, each of which will give 90° phase shift at low frequencies, as well as three networks having an analogous effect at high frequencies (the output resistances and the shunt capacitance of following stages). The limiting transfer characteristic (in both phase and amplitude) determined by these networks is known as the asymptotic characteristic.

The easiest way to satisfy the stability condition at the low-frequency side of the pass band, for a two-stage or three-stage amplifier, is to let one or two coupling networks attenuate at 6 db/octave down to the frequency at which the loop gain is unity or less than unity by the desired amplitude margin.[1] If it is possible to use sufficiently large resistances and capacitances, the other coupling networks may be made to introduce very little phase shift above this frequency and to have almost all their phase-shifting effect at frequencies where the loop gain is less than unity. The analogous procedure for the high-frequency

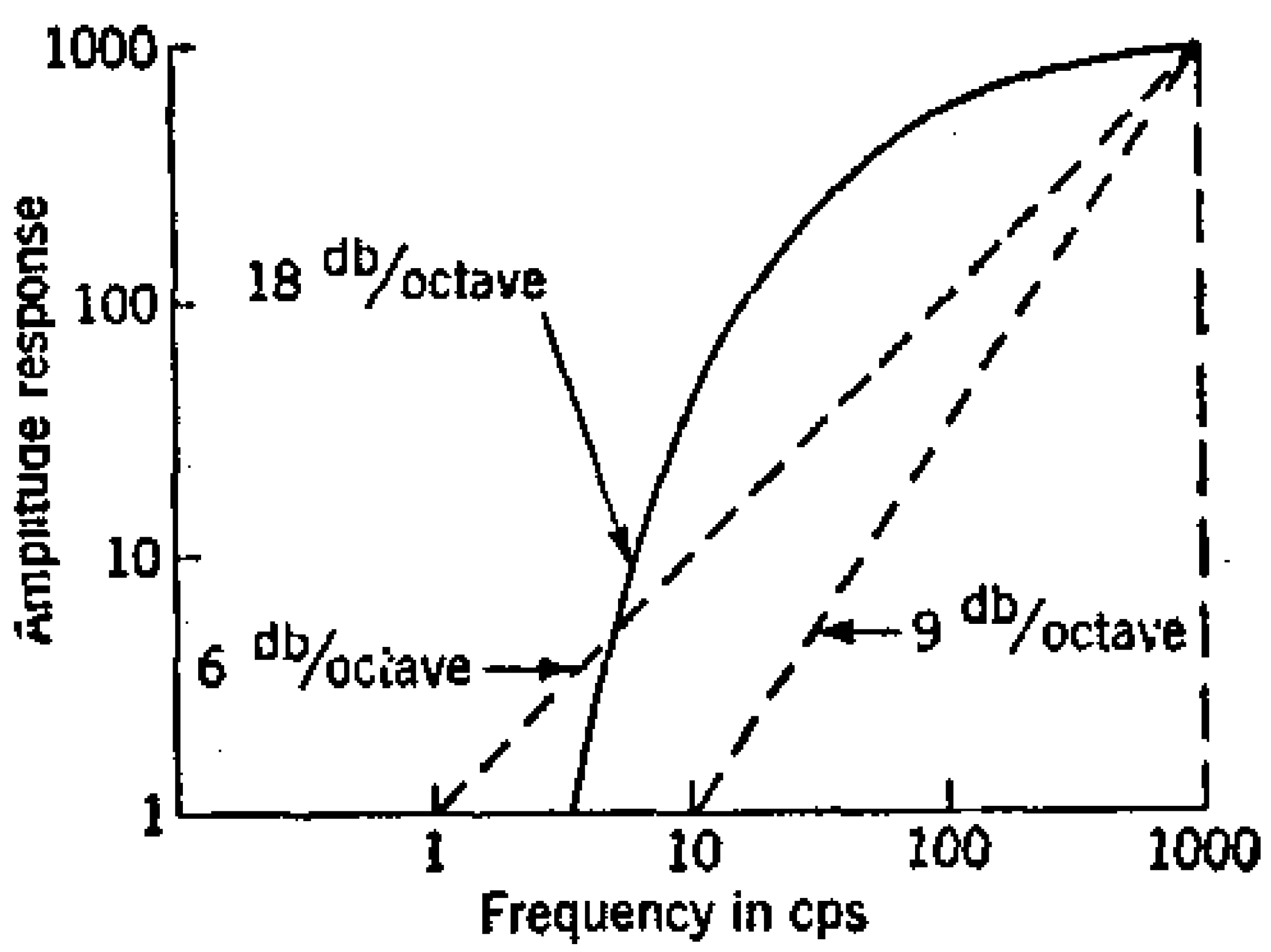

FIG. 9·3.—Low-frequency asymptotic characteristics. Solid line represents possible asymptotic characteristic for a three-stage amplifier.

response is again to make one stage attenuate so that unity gain is reached before the other stages have any effect. This might be achieved, for instance, by putting an additional capacitance in parallel with one of the tube input capacitances. This method cannot be used, however, if the necessary loop gain is too high relative to the ratio of the frequency at which the amplifier is designed to operate and the frequency at which the asymptotic characteristic has unity gain (see Fig. 9·3). In the example shown in Fig. 9·3 the computing frequency is 1000 cps, and the gain at this frequency is 1000 (60 db). If the designer tried to make the amplifier attenuate at 6 db/octave, the effect of the asymptotic characteristic as determined by the inherent properties of the amplifier components would predominate before unity gain was reached and oscillation would probably result. If he could produce a slope of 9 db/octave, however, it might be possible to reach unity gain without having 180° phase shift. Roughly, 6 db/octave corresponds to 90°, 12 db/octave to 180°, etc.; in order to afford a margin of safety, therefore, the slope of the attenuation curve must be somewhat less than 12 db/octave. In order to obtain slopes between 6 and 12 db/octave, networks more elaborate than single *RC*-coupling networks can be used.

The characteristics attainable are sharply limited if light weight is required, for this means that neither condensers larger than some physically small size such as 0.1 μf nor heavy choke coils are permissible in the low-frequency networks.

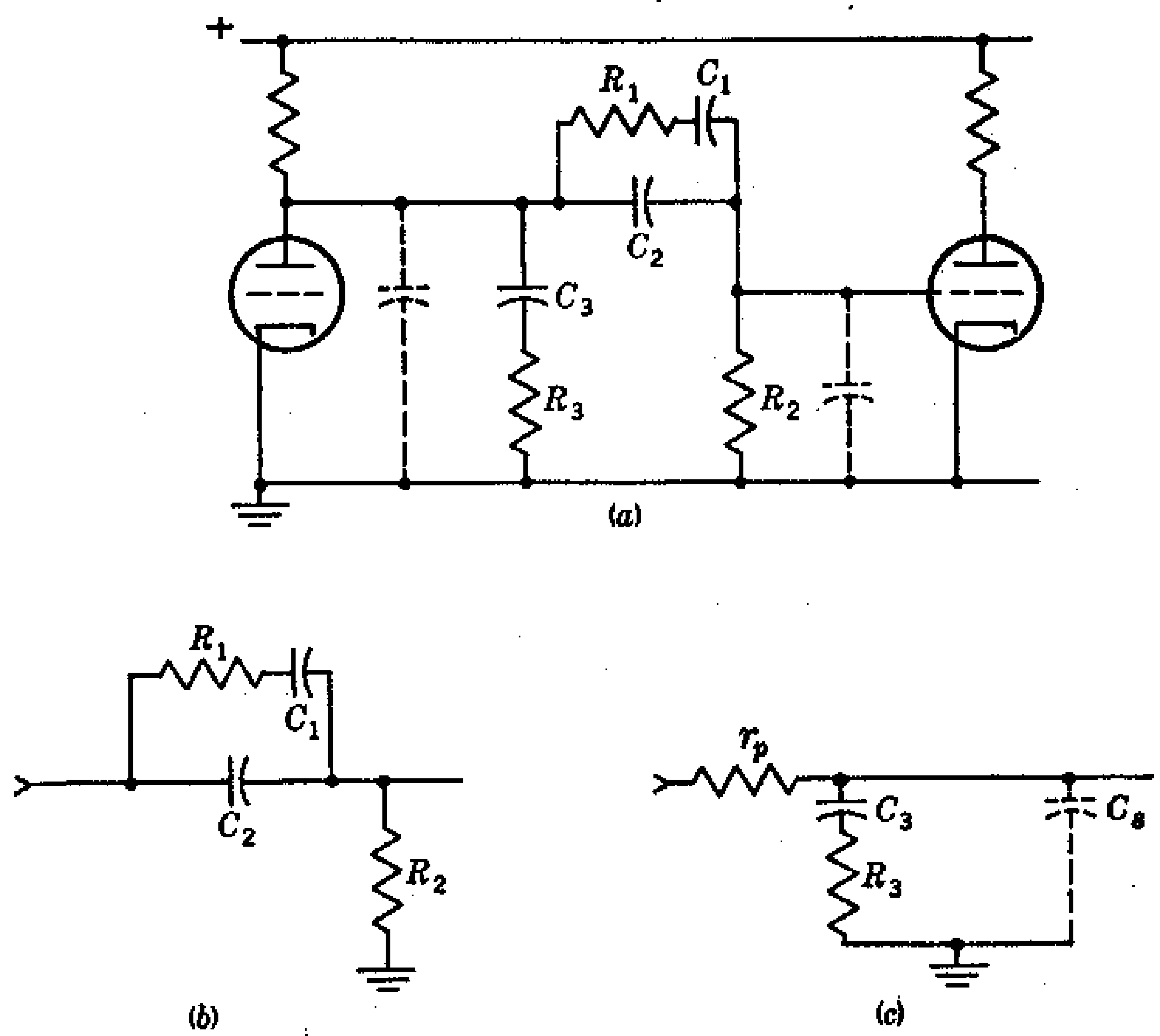

FIG. 9·4.—Typical coupling network. (*a*) Coupling network; (*b*) low-frequency equivalent circuit; (*c*) high-frequency equivalent circuit.

The principal topic to be developed here is the stabilization of three-stage amplifiers by the use of coupling networks similar to those shown in Fig. 9·4. A good example of this is given by Bode.[1] The method used in this example emphasizes the amplitude response, an easily measurable function, and the calculation of the phase response from it. An alternative method, which has advantages in certain special cases, employs the direct calculation of phase response as a function of frequency, using the amplitude response at only a few points. The calculation of the phase response of resistance-capacitance networks is considerably easier than the calculation of the amplitude response. It is particularly helpful at low frequencies, where the values of the parameters involved are fairly well determined; at high frequencies the values of stray and input capacitances are less well known before the layout is made, and more experimental work has to be done to complete a design.

The equivalent high-frequency and low-frequency stabilizing networks used (Fig. 9·4) may be considered together. The property of these networks that makes them useful is that each may have a "plateau" in the curve of phase shift vs. frequency. There are other *RC*-networks having this property, but all those using only two "independent" condensers[1] may be treated mathematically in the same way. If it is assumed that these networks include the effect of the output impedance of the preceding stage and the input impedance of the next stage, each network may be analyzed as a three-terminal network containing *R*'s and *C*'s and operating from zero impedance into infinite impedance. By means of the loop analysis, the ratio e_0/e_i may be expressed as a quotient of determinants. The denominator is a polynomial of the second order in $1/p$; the numerator cannot be of order higher than the second. Thus, the most general representation of e_0/e_i is

$$\frac{e_0}{e_i} = A\,\frac{p^2 + a_1 p + b_1}{p^2 + a_2 p + b_2} = A\,\frac{(p - p_1)(p - p_2)}{(p - p_3)(p - p_4)}, \qquad (16)$$

where the roots $p_4 \ldots p_4$ are real quantities of dimension T^{-1} because it has been assumed that the networks contain only resistances and capacitors.

The physical significance of this relationship is that for certain real values of p (corresponding to exponentially varying voltages and currents) the ratio e_0/e_i can be either zero or infinite.[2] However, only the pure imaginary values of p are considered in finding the phase response of the network as a function of frequency. As a further simplification, it may be noted that the equivalent low-frequency network has zero response at zero frequency and unity response at infinite frequency; the equivalent high-frequency network behaves in exactly the opposite way, having zero response at infinite frequency and unity response at zero frequency. Thus, for the low-frequency network,

$$\frac{e_0}{e_i} = \frac{p(p - p_2)}{(p - p_3)(p - p_4)}, \qquad (17a)$$

[1] Two condensers are "independent" if current loops can be so drawn that only one passes through each of the condensers. This ensures that the determinant of coefficients in the loop equations is a polynomial of the second order in $1/p$, since $1/p$ occurs twice on the principal diagonal.

and for the high-frequency network,

$$\frac{e_0}{e_i} = \frac{-p_3 p_4}{p_2}\,\frac{(p - p_2)}{(p - p_3)(p - p_4)}. \qquad (17b)$$

Finally, setting $p = j\omega$ and making use of the fact that the phase angle of a product of complex factors is the algebraic sum of their separate phase angles, it is found that for the low-frequency network

$$\phi\left(\frac{e_0}{e_i}\right) = +\frac{\pi}{2} + \tan^{-1}\frac{\omega}{-p_2} - \tan^{-1}\frac{\omega}{-p_3} - \tan^{-1}\frac{\omega}{-p_4}, \qquad (18a)$$

and for the high-frequency network

$$\phi\left(\frac{e_0}{e_i}\right) = \tan^{-1}\frac{\omega}{-p_2} - \tan^{-1}\frac{\omega}{-p_3} - \tan^{-1}\frac{\omega}{-p_4}. \qquad (18b)$$

In computing the phase response of such a network, it is necessary to find the roots that characterize it and to use them in connection with a single inverse-tangent curve (Fig. 9·5). This curve gives directly the phase shift of a single *RC* coupling network. The over-all phase response of the network or of several such networks is the algebraic sum of these inverse-tangent curves. Changing the value of p_i is equivalent to adding a constant to $\log_{10}\omega$ and has the effect of moving the curve bodily along the $\log_{10}\omega$ axis without changing its shape. Any particular curve may be located by observing that at $\omega = p_i$, $\phi = 45°$. The corresponding frequency, at which the capacitive reactance of a single network is equal to its resistance, will be called the central frequency. The design objective is now to produce a desired total phase response; this is done by successive trials, as will be illustrated in Sec. 9·7.

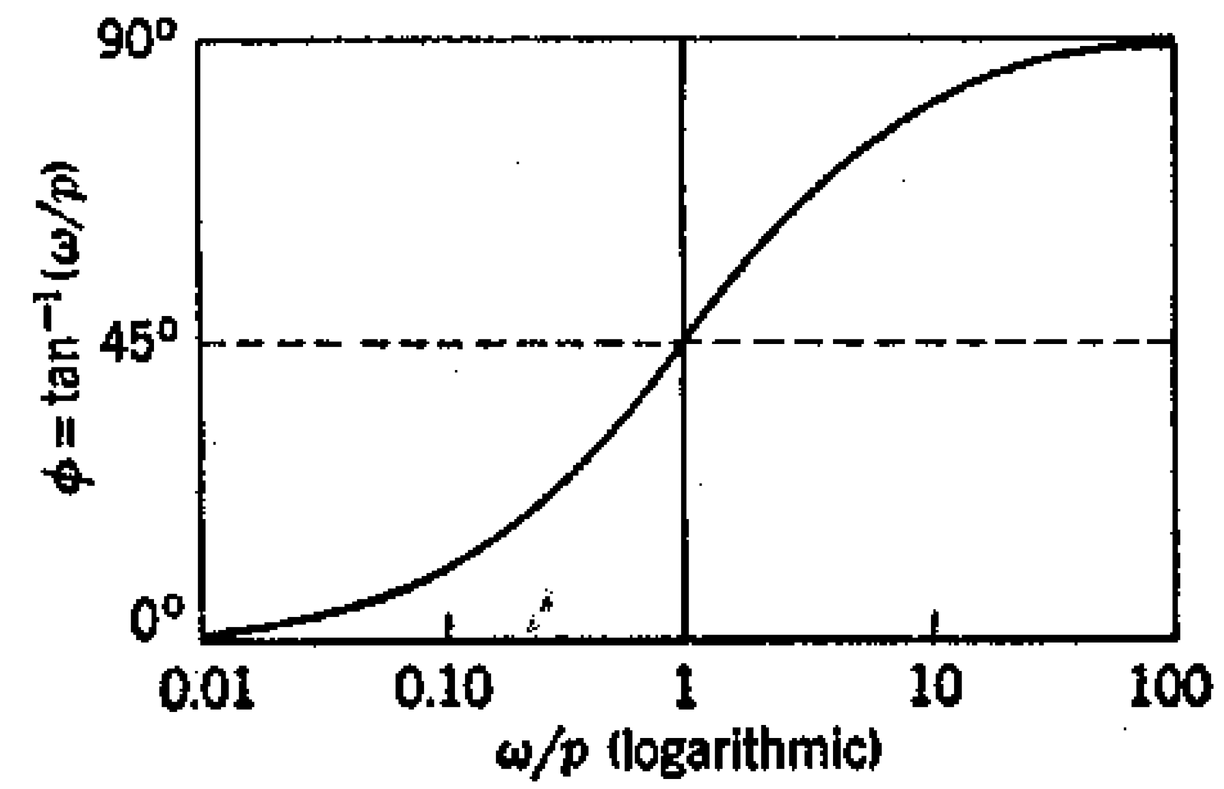

Fig. 9·5.—Inverse-tangent curve.

Consider first the "phase-advance" network, so-called from its use in servomechanisms (see Fig. 9·6). For this circuit,

$$\frac{e_0}{e_i} = \frac{R_2}{\dfrac{1}{(1/R_1) + pC} + R_2} = \frac{p + \dfrac{1}{CR_1}}{p + \dfrac{R_1 + R_2}{R_1 R_2 C}}. \qquad (19)$$

Then the phase response of the circuit will be given by

$$\phi = \tan^{-1}(\omega R_1 C) - \tan^{-1}\left(\frac{\omega R_1 R_2 C}{R_1 + R_2}\right). \qquad (20)$$

This expression as plotted in Fig. 9·6*b* has a maximum value at the logarithmic mean of the two roots $-p_1 = +1/CR_1$ and

$$-p_2 = +\frac{(R_1 + R_2)}{R_1 R_2 C}.$$

It may also be seen from Fig. 9·6*b* that the value of maximum phase shift is

$$2\left[\left(\tan^{-1}\sqrt{\frac{p_2}{p_1}}\right) - 45°\right] = 2\left[\left(\tan^{-1}\sqrt{1 + \frac{R_1}{R_2}}\right) - 45°\right]. \qquad (21)$$

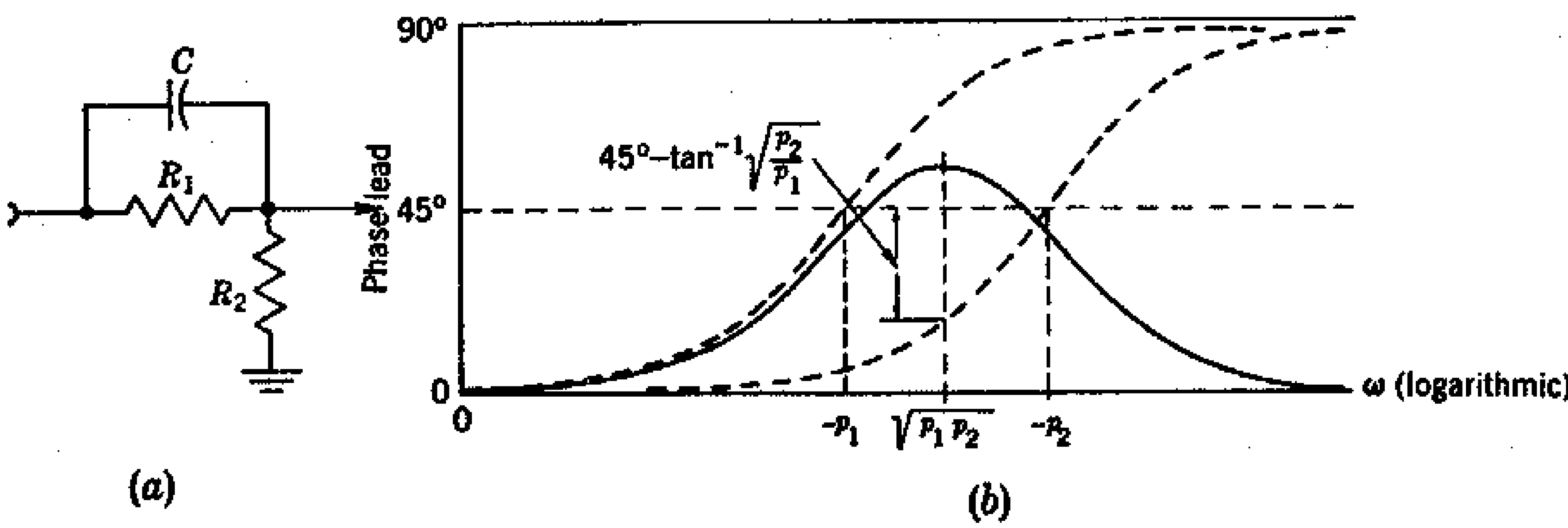

FIG. 9·6.—"Phase-advance" network. (*a*) Network; (*b*) phase response as a function of frequency, $\frac{p_2}{p_1} = 10$; $-p_1 = \frac{1}{CR_1}$; $-p_2 = \frac{(R_1 + R_2)}{R_1 R_2 C}$; $\sqrt{p_1 p_2} = \frac{1}{CR_1}\sqrt{1 + \left(\frac{R_1}{R_2}\right)}$.

The maximum value of phase shift is equal to the difference of the two dotted curves at the center of the horizontal axis and is equal to twice the difference of either dotted curve from 45°. This result is generally useful in connection with linear *RC*-networks containing only one condenser. It may be noted that

$$\frac{p_2}{p_1} = \frac{\left(\frac{e_0}{e_i}\right)_{f=\infty}}{\left(\frac{e_0}{e_i}\right)_{f=0}}. \qquad (22)$$

This equation may sometimes be used as a convenient way of determining p_2/p_1 in order to find the maximum phase shift; the right-hand side of the equation may be found from experimental gain measurements with and without the condenser (see Sec. 9·13).

A typical low-frequency stabilization network is shown in Fig. 9·7*a*. The frequency characteristic of this network can be explained qualitatively by considering the effects that occur as the impedance of one capacitance or the other becomes large with decreasing frequency. The usual design procedure is to let R_1 and C_1 be larger than R_2 and C_2 respectively. At the high-frequency end of the characteristic, R_1 has a considerably higher impedance than C_2, and the characteristic, determined largely by R_2 and C_2, starts as an inverse-tangent curve. As the frequency is decreased, the impedance of C_2 increases to the same order of magnitude as that of R_1. To the extent that the impedance of the section consisting of R_1, C_1, and C_2 approaches a real quantity in this region, there is a tendency for the phase shift to return to zero. Finally, as the impedance of C_1 rises to the order of magnitude of R_1, the response of the network approaches that of the part consisting of R_1, C_1, and R_2, this response being another inverse-tangent curve.

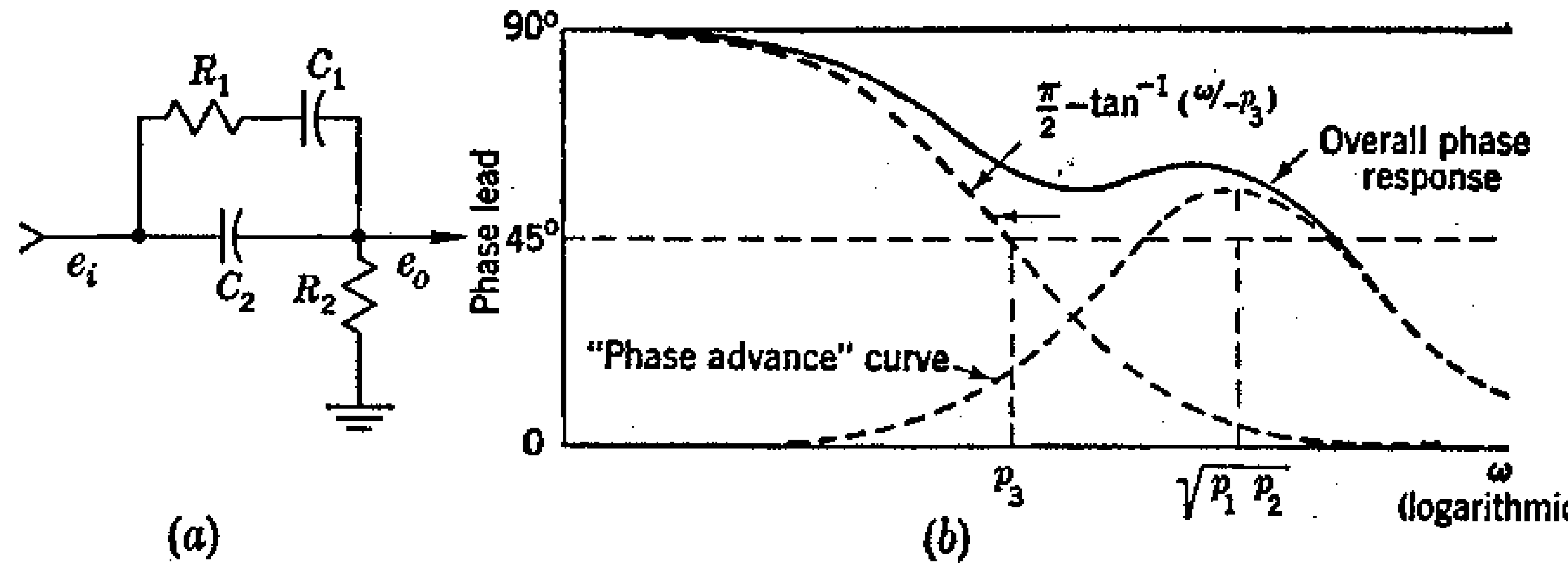

FIG. 9·7.—Low-frequency stabilization network. (*a*) Network; (*b*) phase response. $\frac{p_2}{p_1} = 10$, $\sqrt{\frac{p_1 p_2}{p_3}} = 10$.

The equations for this network can be written

$$\frac{e_0}{e_i} = \frac{R_2}{R_2 + \cfrac{1}{\cfrac{1}{R_1 + (1/pC_1)} + pC_2}}$$

$$= \frac{p\left(p + \frac{1}{R_1 C_1} + \frac{1}{R_1 C_2}\right)}{p^2 + p\left(\frac{1}{R_1 C_1} + \frac{1}{R_2 C_2} + \frac{1}{R_1 C_2}\right) + \frac{1}{R_1 R_2 C_1 C_2}} \qquad (23)$$

The roots are, for the numerator,

$$p_1 = 0, \qquad p_2 = -\left(\frac{1}{R_1 C_1} + \frac{1}{R_1 C_2}\right) \qquad (24a)$$

and, for the denominator,

$$p_{3,4} = -\frac{\left(\frac{1}{R_1 C_1} + \frac{1}{R_2 C_2} + \frac{1}{R_1 C_2}\right)}{2} \pm \sqrt{\frac{\left(\frac{1}{R_1 C_1} + \frac{1}{R_2 C_2} + \frac{1}{R_1 C_2}\right)^2}{4} - \frac{1}{R_1 R_2 C_1 C_2}}. \qquad (24b)$$

If, in these expressions, the assumptions are made that $C_1 \gg C_2$ and $R_1 \gg R_2$, the following approximate formulas are obtained:

$$p_2 = -\frac{1}{R_1C_2}; \qquad p_3 = -\frac{1}{R_2C_2}; \qquad p_4 = -\frac{1}{R_1C_1}. \tag{24c}$$

Here p_2 and p_3 may be said to correspond to a phase-advance network, and p_4 corresponds to the low-frequency limiting response. The phase response is then given by Eq. (18a). The phase-shift characteristic can thus be represented as an algebraic sum of three inverse-tangent curves or as the sum of a curve like that of the phase-advance network and an additional inverse-tangent curve (Fig. 9·7b). In the central region of the characteristic the phase is relatively constant with respect to frequency. In the design of a three-stage amplifier the average

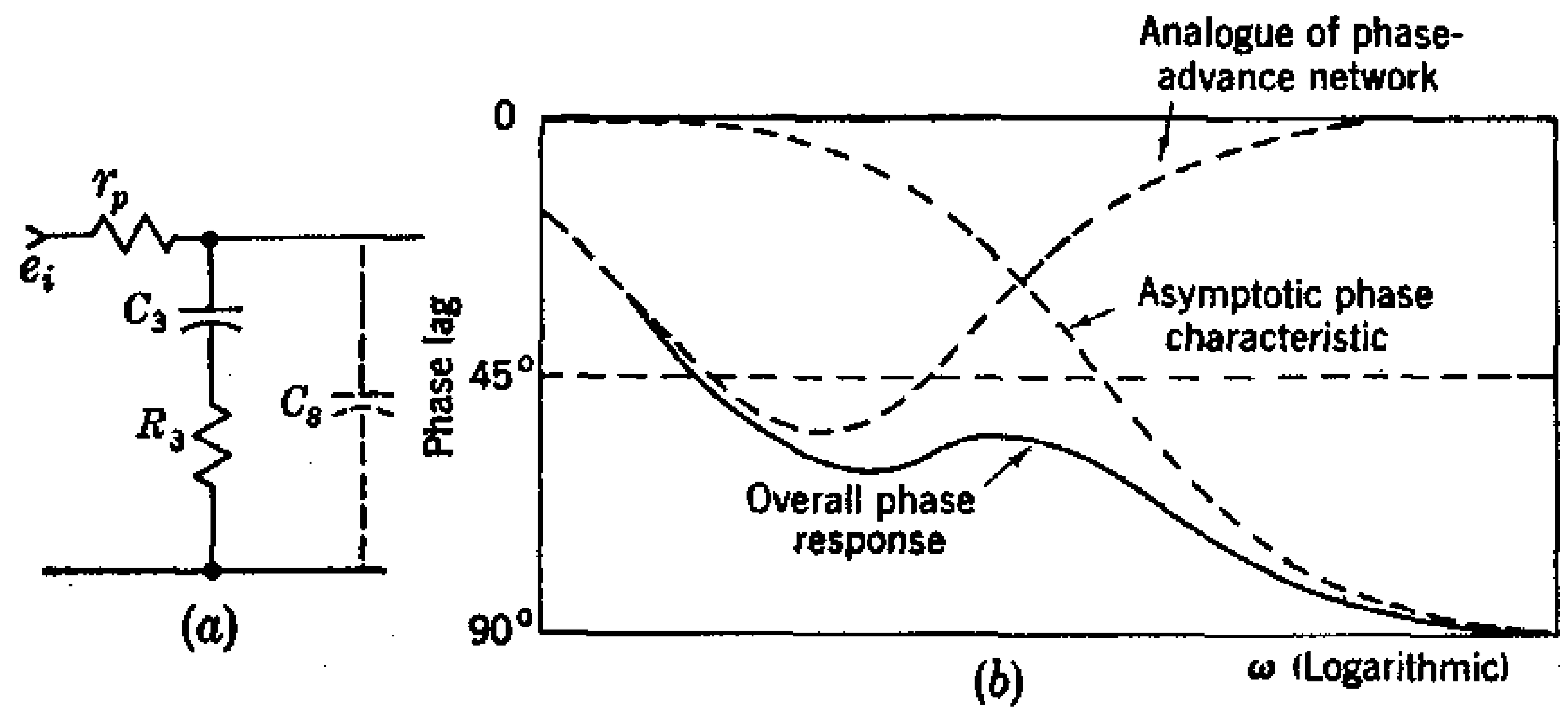

FIG. 9·8.—High-frequency stabilization network. (a) Network; (b) phase response.

phase shift in this region should be kept somewhat less than 60° in order that the response for three such networks will be less than 180°.

Similarly, the network, equivalent at high frequencies to that shown in Fig. 9·4a can be considered to be mathematically equivalent to the series-shunt circuit (r_pC_s) plus a circuit analogous to the phase-advance network, which may be called a phase-retard network. This equivalent circuit is shown in Fig. (9·8a). In calculating the response of the equivalent high-frequency network, a similarity to the low-frequency network may be noted. If the components in Fig. 9·7a are renamed by substituting r_p for R_2, C_s for C_2, R_3 for R_1, and C_3 for C_1, the result is found to be the same as for the equivalent high-frequency network, except that the input and ground terminals are interchanged. From this it can immediately be seen that the sum of the responses of the high-frequency network and the renamed low-frequency network is unity; for if at any frequency the response of the high-frequency network is $Z_2/(Z_1 + Z_2)$ (where $Z_1 = r_p$ and Z_2 is the impedance of the network C_s, R_3, C_3), the response of the renamed low-frequency network is $Z_1/(Z_1 + Z_2)$. Therefore

$$\frac{e_0}{e_i} = 1 - \frac{p(p - p_2)}{(p - p_3)(p - p_4)}$$

where the p_i's may be found from Eq. (24) by renaming the terms. In particular, from Eq. (23),

$$\frac{e_0}{e_i} = 1 - \frac{p\left(p + \frac{1}{R_3C_3} + \frac{1}{R_3C_s}\right)}{p^2 + p\left(\frac{1}{R_3C_3} + \frac{1}{r_pC_s} + \frac{1}{R_3C_s}\right) + \frac{1}{R_3C_3r_pC_s}} \tag{25a}$$

$$= \frac{1}{r_pC_s}\,\frac{p + \frac{1}{R_3C_3}}{(p - p_3)(p - p_4)}.$$

Subject to the approximations $R_3 \ll r_p$, $C_s \ll C_3$, the roots are approximately

$$\left.\begin{aligned} p_2 &= -\frac{1}{R_3C_3}, \\ p_3 &= -\frac{1}{R_3C_s}, \\ p_4 &= -\frac{1}{r_pC_3}. \end{aligned}\right\} \tag{25b}$$

SAMPLE DESIGNS OF COMPUTER AMPLIFIERS

Three computer amplifiers that have been designed for inductive loads and one for a resistive load will be discussed here. The reason for the emphasis on inductive loads is that several types of computer use angle resolvers[1] whose input impedances are chiefly inductive.

TABLE 9·1.—DATA ON RESOLVERS

Manufacturer	Arma Corp.	Bendix Pioneer
Serial No	Dwg. No. 213044	XD-759542
Weight, lb	5	1
Stator reactance (400 cps), ohms	j5000	j3000*
Stator-to-rotor voltage ratio (rotor open-circuited)	1.0	0.9
Maximum voltage on stator (400 cps), rms	≈ 100 volts	≈ 60 volts
Corresponding "saturation current," ma	$20\sqrt{2}$	$20\sqrt{2}$
Peak deviation from linearity of rotor voltage with respect to stator voltage (as fraction of max. output), %.	Approximately† 0.15	Approximately† 0.15

* Effective series resistance = 600 ohms.
† These figures are subject to variation, dependent upon the method of measurement. The values given are conservative.

Pertinent data on two types of resolver are given in Table 11·1. It was arbitrarily decided to let the resolver stator be the primary winding and its rotor be the secondary or output winding. It can be seen (Table 9·1) that within the specified region of operation, the magnitude of rotor output voltage varies almost linearly with the magnitude of stator input voltage.

In the design of these circuits, electrolytic condensers are used to bypass cathode and screen impedances but are not used for interstage coupling because of the effect that d-c leakage through the condenser might have on the grid bias. The maximum value of coupling capacitance used is limited to 0.1 μf because of the physical size of paper-dielectric capacitors of this value. In a great deal of aircraft equipment, electrolytic capacitors can not be used at all because they do not meet specifications for high-altitude operation.

9·4. Single-stage Drivers. *The Cathode Follower.*—This simplest one-stage feedback amplifier has been used extensively as an impedance-changing device, but the employment of reactive loads requires special designs. A typical a-c cathode-follower circuit is shown in Fig. 9·9.

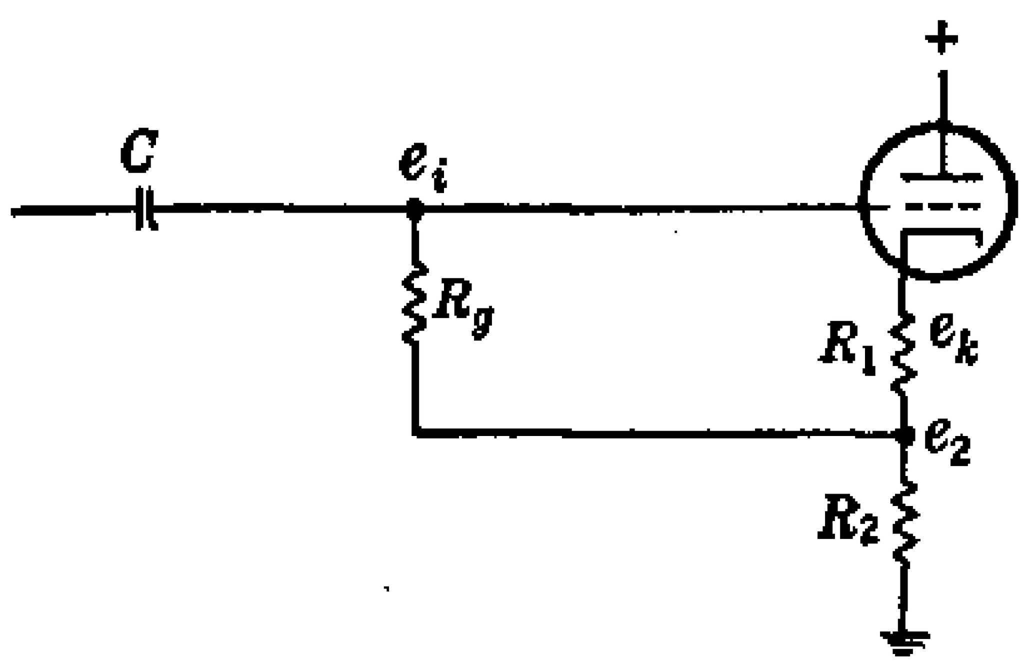

FIG. 9·9.—A-c cathode follower.

The input impedance can be calculated by methods similar to those of Sec. 9·1. The input capacitance is equal to $C_{gp} + [(e_i - e_k)/e_i]C_{gk}$ and is approximately equal to C_{gp}. The resistive component of input impedance (in parallel with this capacitance) is $R_g[e_i/(e_i - e_2)]$. If the current in R_g is neglected relative to the cathode current in computing e_2, the quantity $[e_i/(e_i - e_2)]$ can be easily calculated. The gain of the cathode follower is

$$\frac{e_k}{e_i} = \frac{1}{1 + \frac{1}{\mu} + \frac{1}{g_m(R_1 + R_2)}}$$

and

$$\frac{e_2}{e_k} = \frac{R_2}{R_1 + R_2}.$$

Therefore,

$$\frac{e_i}{e_i - e_2} = \frac{1}{1 - \frac{e_2}{e_i}} = \frac{1}{1 - \frac{R_2}{(R_1 + R_2)\left[1 + \frac{1}{\mu} + \frac{1}{g_m(R_1 + R_2)}\right]}}, \quad (26)$$

and the input resistance is approximately

$$R_g\left(\frac{R_1 + R_2}{R_1}\right)$$

if $\mu \gg 1$, and $g_m(R_1 + R_2) \gg 1$. A nonresistive cathode impedance Z_k could be substituted for $R_1 + R_2$ without invalidating the derivation of e_k/e_i provided that the d-c levels are properly maintained. In this case

$$\frac{e_k}{e_i} = \frac{1}{1 + \frac{1}{\mu} + \frac{1}{g_m Z_k}},$$

and

$$\frac{e_i - e_k}{e_k} = \frac{1}{\mu} + \frac{1}{g_m Z_k}. \quad (27)$$

The limits of linear operation of a cathode follower are determined by the grid current and cutoff characteristics of the tube. These limits can be calculated by the use of the preceding equations. If it is assumed that the voltage $e_{gk} = e_i - e_k$ has the limits 0 (corresponding to grid current) and e_{co} (at cutoff), and if the region of a-c operation is chosen so that these limits are reached together by the positive and negative peaks of the grid-cathode waveform, then the maximum output is given by

$$\frac{(e_k)_{max}}{(e_{gk})_{max}} = \frac{1}{\frac{1}{\mu} + \frac{1}{g_m Z_k}}. \quad (28)$$

Since the rms value of

$$(e_{gk})_{max} = \frac{e_{co} - 0}{2\sqrt{2}},$$

and[1]

$$e_{co} \approx \frac{e_p}{\mu},$$

then, finally, the maximum rms output is given by

$$|(e_k)_{max}| = \frac{e_{co}}{2\sqrt{2}\left|\frac{1}{\mu} + \frac{1}{g_m Z_k}\right|} = \frac{e_p}{2\sqrt{2}\left|1 + \frac{r_p}{Z_k}\right|}. \quad (29)$$

The value of e_p used for a reactive load will be different from that for a resistive load, for in the former case the load line is an ellipse and the nearest approach to cutoff will be at a value of e_p less than the plate supply voltage.

It is often undesirable to use an ordinary cathode follower for driving an inductive resolver because the linearity of the stator-to-rotor transfer characteristic is affected by magnetic saturation; moreover, unless resonant tuning is used, the tube must supply a direct current at least as great as the peak alternating current in the inductive load. For cases where the desired range of operating frequencies is too great to permit such tuning, the circuit of Fig. 9·10 which was designed for use with the Arma resolver (Table 9·1), can be used. To make use of the tetrode characteristics of a tube such as the 6V6, it is necessary to bias the screen from a relatively high-impedance source and condenser-couple it to the cathode. The circuit shown in Fig. 9·10 satisfies these conditions because the inductive load itself has the high a-c and low d-c impedance necessary for screen bias. The d-c screen current flowing through the load is less than 5 ma and does not produce serious saturation.

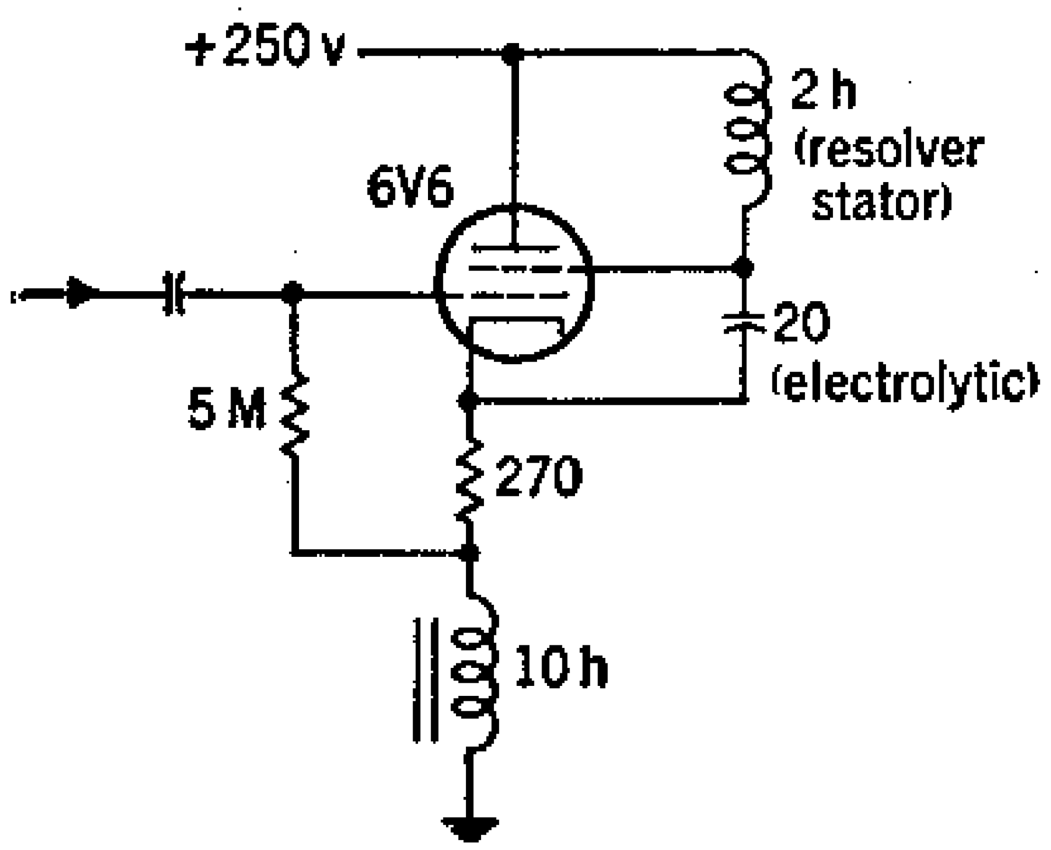

FIG. 9·10.—Single-stage driver.

For this circuit the maximum deviation from linearity of peak a-c voltage across the load with respect to peak a-c input voltage was measured as 0.08 per cent of maximum output up to an output voltage of 60 volts rms. However, changing tubes, especially changing from one make of 6V6 to another, changed the gain by ±0.25 per cent.

A single stage with plate-to-grid feedback can also be used to drive an inductive load as is shown in Fig. 9·11. In this circuit the plate current flows through the inductor; and because it may saturate the core, the maximum output voltage is correspondingly limited. The analysis of resistive-mixing feedback in Sec. 9·2 is applicable to this circuit. Compared with the modified cathode follower shown in the previous figure, it has the disadvantages of lower input impedance and increased sensitivity to tube-parameter variability.

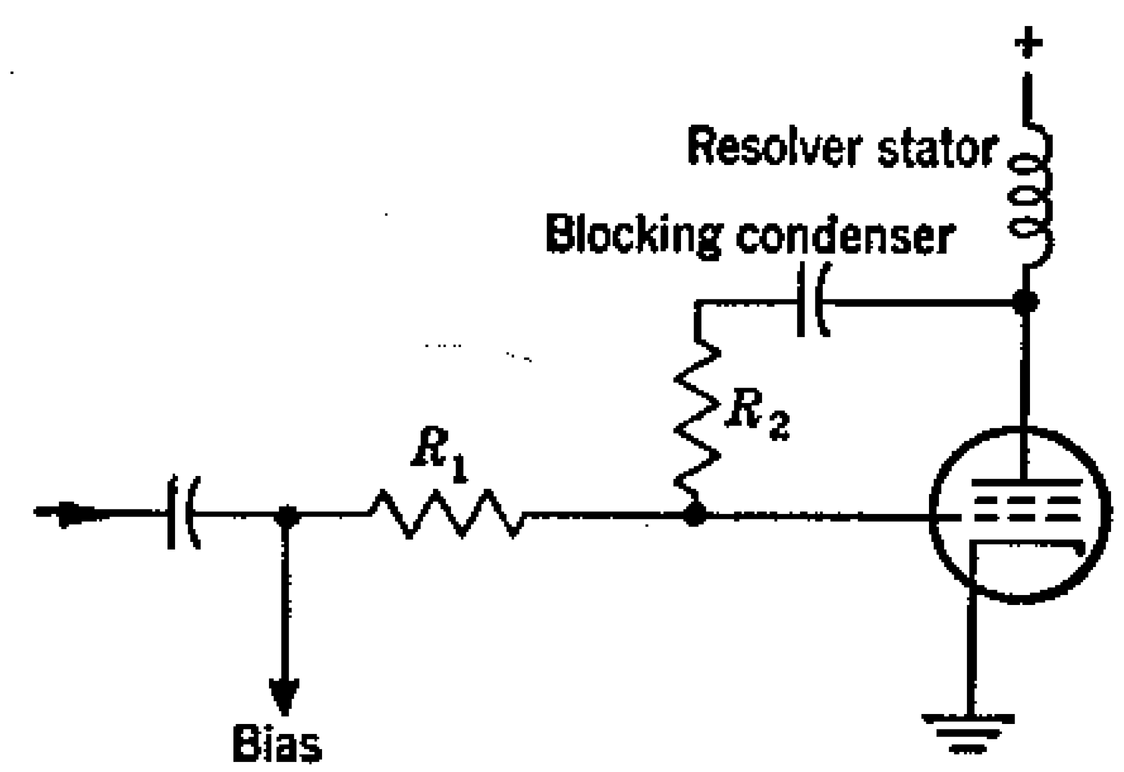

FIG. 9·11.—Single-stage driver with plate-to-grid feedback.

9·5. Driver with Push-pull Output Stage and Regeneration within the Loop.—The circuit in Fig. 9·12 was designed to drive the stator of an Arma resolver (Table 9·1). Cathode feedback was employed, and a pentode was therefore used in the first stage to secure a high amplification factor. The design procedure for this amplifier was largely experimental, both with regard to antioscillation measures and with respect to maintaining constancy of gain with tube change. The 0.001-μf condenser across the output transformer was used to suppress oscillations; it prevented the high-frequency response from falling off too rapidly with increasing frequency. The 2.2-kilohm resistor and the 0.05-μf condenser provide a low-Q tuning for the load. The feedback from the transformer secondary to the right-hand grid of the output stage is regenerative. The bleeder determining how much signal is fed back was adjusted so that the output stage, disconnected from the pentode, was just on the threshold of oscillation, thus providing an over-all gain very near to unity. The decrease in the linearity of the regenerative stage of the amplifier was offset by the increase of gain; thus the linearity

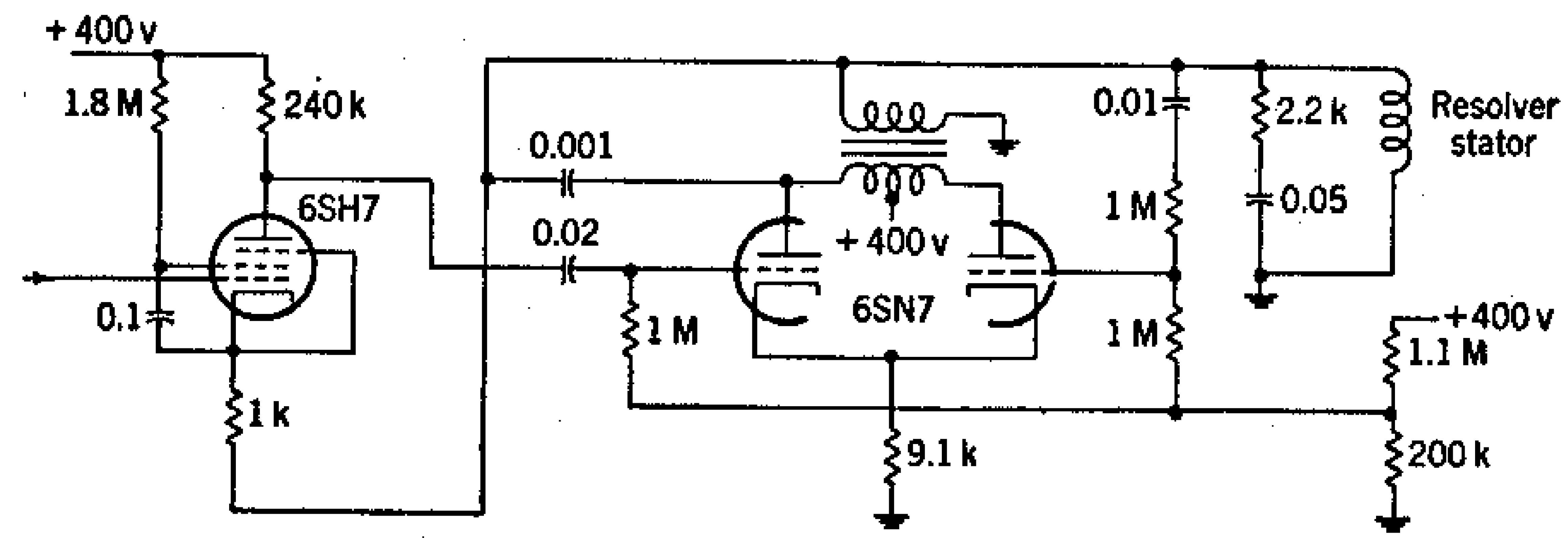

FIG. 9·12.—Driver circuit with push-pull output stage and regeneration.

(and constancy of gain with respect to tube changes, etc.) with the over-all negative feedback was not impaired (see Chap. 10). Since the over-all feedback factor was unity, infinite gain without negative feedback would be needed for unity gain with the negative feedback. If exactly unity gain is not an important consideration, more symmetrical push-pull action can be obtained by reducing the regeneration; this can be done without appreciably sacrificing constancy of over-all gain.

The observed performance of the circuit was as follows: The difference between output and input voltages was less than 0.03 volt up to an output voltage of 70 volts rms. This figure includes the effects due to substituting tubes whose parameters vary over the entire range permitted by the manufacturing tolerances.

TWO-STAGE DRIVER FOR INDUCTIVE LOAD WITHOUT TRANSFORMER OUTPUT

9·6. General Considerations.—The object of designing this circuit was to reduce the weight in comparison with the amplifier shown in

Sec. 9·5 and to analyze more thoroughly the conditions for preventing oscillations. In order to save weight, miniature tubes were used, and the load, a Bendix resolver (Table 9·1) especially designed for light-weight applications, was condenser-coupled rather than transformer-coupled.

The circuit type of Fig. 9·1c was chosen, and the accuracy requirement set at ±0.1 per cent probable variation in over-all gain (and ±0.001 radian in phase) with respect to replacement of all components. This requirement seemed realizable because a loop gain $\mathcal{A}\beta$ of 300 to 500 can be obtained with two stages if $\beta = 1$; the approximate variation of g_m (the largest source of error) is ±30 per cent, and feedback could reduce the effect of this by a factor of approximately $1/\beta\mathcal{A}$.

The circuit was designed to give a maximum output voltage of between 10 and 40 volts rms. The supply voltage, tube type, and load determine this, and the voltage scale of the computer was to be chosen accordingly. It was assumed that the first stage would employ a type 6AK5 and the output stage a type 6C4. The plate supply voltage was to be 250 volts, and the operating frequency was to be 500 cps ± 2 per cent. The tube-parameter tolerances, as given in the JAN specifications, are shown in Table 9·2. In many cases it would be desirable to supplement these with additional tube data relating more directly to circuit design.[1]

Table 9·2.—Excerpts from JAN Specifications* for Types 6AK5 and 6C4 Tubes

Characteristic	6AK5 under operating conditions of e_p† = 120v, e_{g_1} = −2v, and e_{g_2} = 120v		6C4‡ under operating conditions of e_p = 250v, and e_g = −8.5v	
	Min.	Max.	Min.	Max.
i_g	0	−0.10 μa	0	−1.5 μa
i_p	3.0 ma	12.0 ma	6.5 ma	14.5 ma
i_{g_2}	0.8 ma	4.0 ma	....	....
g_m	3500 μmhos§	6500 μmhos	1750 μmhos	2650 μmhos

* Issued November–December 1944.
† Maximum allowable value of e_p (according to supplement of Mar. 30, 1945): 180v, design-center value.
‡ The maximum recommended value of grid-leak resistor is 0.25M with fixed bias, 1.0M with cathode bias.
§ Reduction of heater voltage to 5.7 volts causes a reduction of g_m of 15 per cent.

9·7. Design of the Output Stage.—A schematic diagram of the output stage is shown in Fig. 9·13. It incorporates cathode bias, condenser-coupling to the load, and an additional condenser C_4 to increase the apparent load impedance by parallel-resonant tuning. Cathode bias was used because it permits a large grid-leak resistor (Table 9·2) and because it stabilizes tube parameters with respect to tube replacement and heater-voltage variation. In the complete amplifier the tuning condenser C_4 does not appreciably affect the current through the resolver stator for a given input voltage, since the voltage feedback makes the voltage across the load nearly equal to the input voltage throughout the operating range of the circuit. This condenser extends the operating range of the amplifier. Parallel-resonant tuning has the disadvantage of increasing the variation in phase shift that is produced by variation in the values of capacitance or of stator impedance, but it will be seen that this is not a serious difficulty.

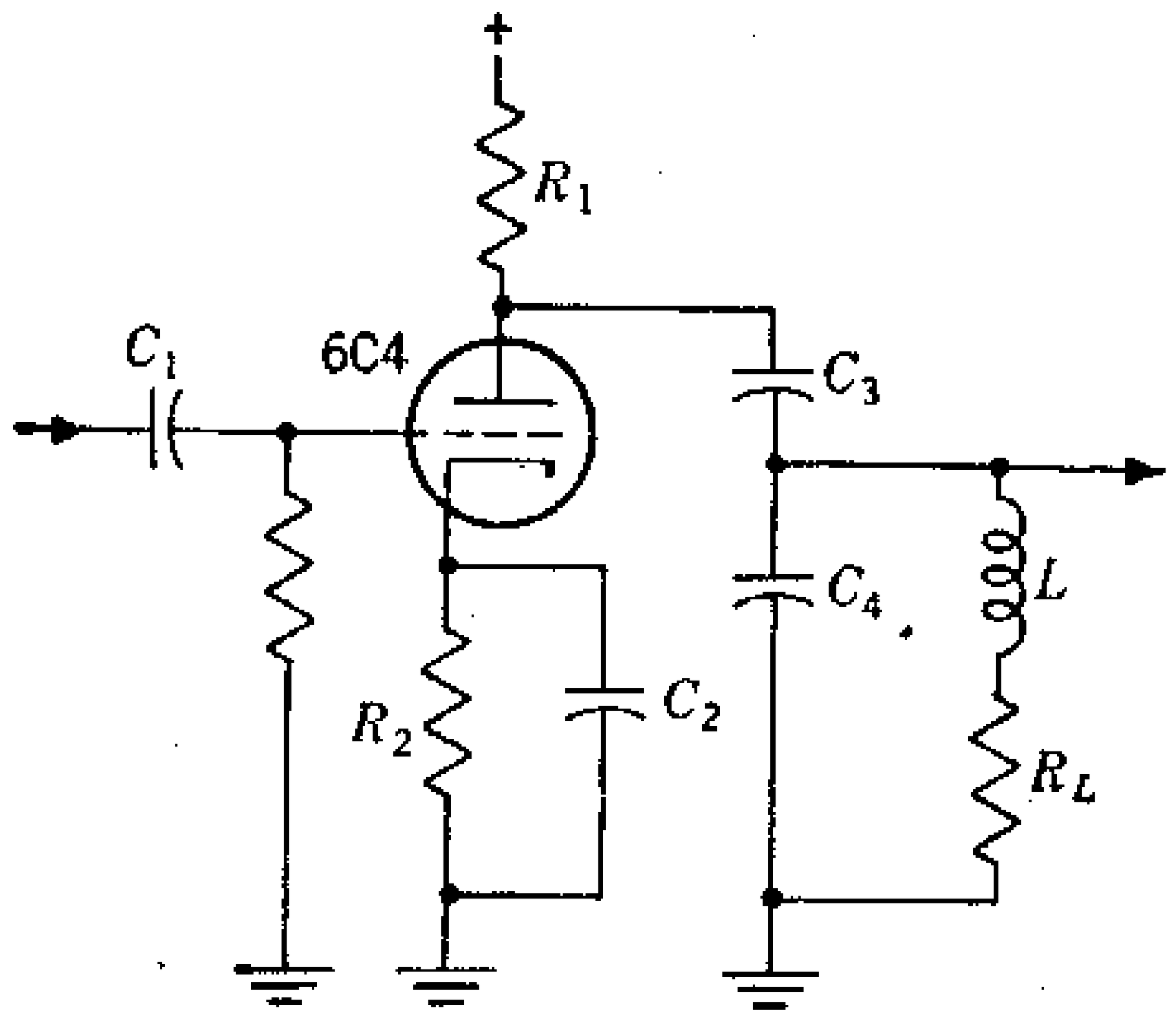

Fig. 9·13.—Output stage of driver.

In order to find the variations in load impedance and in phase shift that might occur, the variations in the load circuit parameters were calculated. Measurements of a typical resolver-stator impedance showed a variation of 15 per cent over the temperature range −50° to +80°. The values of the stator impedances at room temperature for all the units measured varied as much as ±12 per cent from their mean; but if condensers were individually selected to tune each resolver, this effect could be almost nullified. The average value of stator impedance at 500 cps was $600 + j3500$ ohms. The maximum variation in capacity of condensers of the sort to be used was ±10 per cent apart from temperature-dependent changes. As a working assumption, the variation to be expected in the LC product will be taken to be ±15 per cent.

It must be determined whether this range of variation of the LC product can lead to an undesirable phase shift through the amplifier or can make the maximum output voltage too small because of the reduced load impedance. The impedance of a parallel-resonant circuit

[1] See Chap. 11.

in which the resistance R is in series with the inductance is given by

$$|Z| = \sqrt{\frac{R^2 + \omega^2 L^2}{(\omega RC)^2 + (\omega^2 LC - 1)^2}}; \qquad \phi = \tan^{-1}\frac{\omega L}{R} - \tan^{-1}\frac{\omega RC}{1 - \omega^2 LC}.$$

Sample values of $|Z|$ and ϕ can be calculated to show the effect of component variations. Suppose that

$\omega = 3140$ radians/sec ($f = 500$ cps),
$R = 600$ ohms,
$L = 1.1$ henrys,
$C = 0.092$ μf (selected so that $\omega^2 LC = 1$).

For the expected variations of L and C the corresponding values of $|Z|$ and ϕ are as follows:

	$L = 1.1\ h$ $C = 0.092$	L and C each increased by 7%	L and C each decreased by 7%
$\|Z\|$ ϕ	20,300 ohms $-10°$	15,700 ohms $-48°$	15,700 ohms $-28°$

Even though the phase angle ϕ corresponding to an increase of 7 per cent in both L and C is 48°, the phase shift from the grid to the output terminal under this condition will be considerably less than 48° because

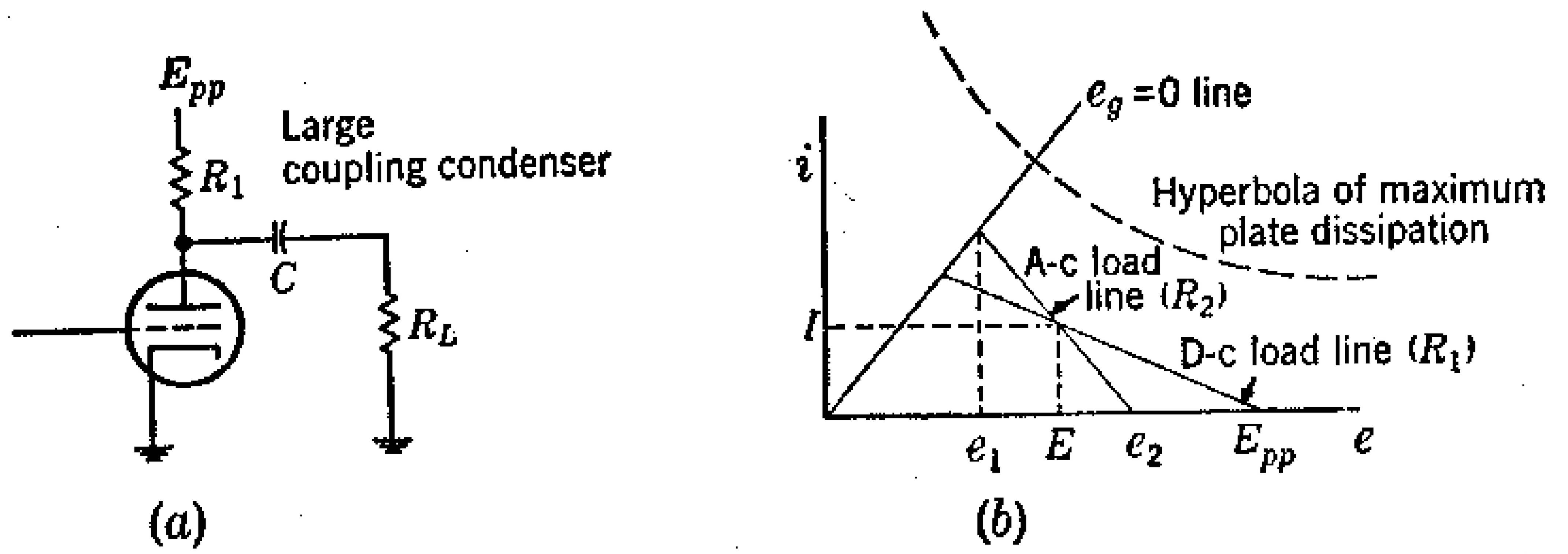

FIG. 9·14.—Triode circuit with condenser coupling to resistive load. (a) Circuit; (b) operating lines.

the output impedance of the tube (nearly equal to r_p if R_k is sufficiently well bypassed) is smaller than the load impedance. Since feedback can reduce the phase shift by a factor of approximately $1/\beta\mathfrak{A}$, a loop gain $\beta\mathfrak{A}$ of 500 will suffice to keep the phase shift with feedback below 0.1°.

It is necessary to choose the best value of d-c plate-load resistance; for this purpose the following derivation is helpful. For a triode amplifier whose plate is condenser-coupled to a resistive load of resistance large enough so that the output voltage is not limited by plate dissipation (Fig. 9·14), there is a value of the d-c plate load resistance R_1 for which maximum output voltage can be obtained without exceeding a given distortion. This value and the corresponding output voltage can be calculated roughly by means of an analysis based on idealized tube characteristics. The procedure will be to state mathematically that the positive and negative voltage swings at the plate, measured from the quiescent voltage, are equal and are limited by cutoff and grid current respectively (Fig. 9·14b). This condition, together with the tube characteristics and component values, determines the operating line and the output voltage for the tube. Maximizing the output voltage with respect to R_1 gives the desired value of R_1.

Let V = d-c plate supply voltage,
E = d-c plate voltage,
I = d-c plate current,
e = instantaneous plate voltage,
e_1 = plate voltage at $e_g = 0$,
e_2 = plate voltage at cutoff,
i = instantaneous plate current,
R_L = load resistance,
$R_2 = \dfrac{R_1 R_L}{(R_1 + R_L)}$.

The value of e at cutoff is

$$e_2 = E + IR_2. \tag{30}$$

The value of e at $e_g = 0$ (assumed to be the grid-current point) is given by the tube characteristic

$$i = \frac{e_1}{r_p} \tag{31}$$

and the equation of the a-c load line

$$e - E = (i - I)(-R_2). \tag{32}$$

Solving for e_1,

$$e_1 = \frac{E + IR_2}{1 + \dfrac{R_2}{r_p}}. \tag{33}$$

If the positive and negative voltage swings from E are equal,

$$e_1 = E - IR_2. \tag{34}$$

By eliminating e_1 from Eqs. (33) and (34), a relation between E and I can be obtained. Combining this with the d-c relation

$$E = E_{pp} - IR_1, \tag{35}$$

it is possible to solve for I and to compute the peak output swing

$$e_{\text{peak}} = IR_2.$$

The rms output is then $e_{\text{peak}}/\sqrt{2}$, or

$$e_{\text{rms}} = \frac{\dfrac{E_{pp}}{\sqrt{2}}}{1 + \dfrac{R_1}{R_2} + \dfrac{2r_p}{R_2}} = \frac{\dfrac{E_{pp}}{2\sqrt{2}}}{1 + \dfrac{r_p}{R_L} + \dfrac{r_p}{R_1} + \dfrac{R_1}{2R_L}}. \tag{36}$$

Maximizing the rms output with respect to R_1 gives

$$R_1 = \sqrt{2r_pR_L} \tag{37}$$

and

$$(e_{\text{rms}})_{\max} = \frac{\dfrac{V}{2\sqrt{2}}}{1 + \dfrac{r_p}{R_L} + \sqrt{\dfrac{2r_p}{R_L}}}. \tag{38}$$

This derivation may be generalized to take into account nonlinear characteristics: If the negative plate swing is a times as great as the positive swing, the equations become

$$R_1 = \sqrt{(1+a)r_pR_L} \tag{39}$$

and

$$(e_{\text{rms}})_{\max} = \frac{\dfrac{V}{2\sqrt{2}}}{1 + \dfrac{r_p}{R_L} + 2\sqrt{\dfrac{r_p}{(1+a)R_L}}}. \tag{40}$$

To estimate the maximum output voltage, 18,000 ohms can be used as the average value of $|Z|$, and r_p set equal to 10,000 ohms. According to the treatment for a triode, if the departure of Z from a pure resistance is neglected, R_1 can be selected equal to

$$\sqrt{2 \times 18K \times 10K} = 19K \approx 20{,}000 \text{ ohms.}$$

The output voltage to be expected can be found approximately from Eq. (38): if $B^+ = 250$ volts,

$$(e_{\text{out}})_{\text{rms}} = \frac{\dfrac{250 \text{ volts}}{2\sqrt{2}}}{1 + \dfrac{r_p}{R_1} + \sqrt{2\dfrac{r_p}{R_1}}} = \frac{88 \text{ volts}}{1 + 0.56 + 1.05} = 35 \text{ volts rms.}$$

In Fig. 9·24 this value is compared with experiment.

The d-c and a-c load lines for a 6C4 are shown in Fig. 9·15a. The approximate optimum bias is found to be -7 volts; the corresponding d-c plate voltage is $+170$ volts; and the plate current, 5 ma; hence the cathode resistor should be 1500 ohms. The plate dissipation is 0.85 watts (see Fig. 9·15). A 5.0-μf electrolytic condenser, for which

$$\frac{1}{\omega C} = 64 \text{ ohms at 500 cps,}$$

may be used to bypass the cathode. The preliminary design of the output stage is shown in Fig. 9·15b.[1]

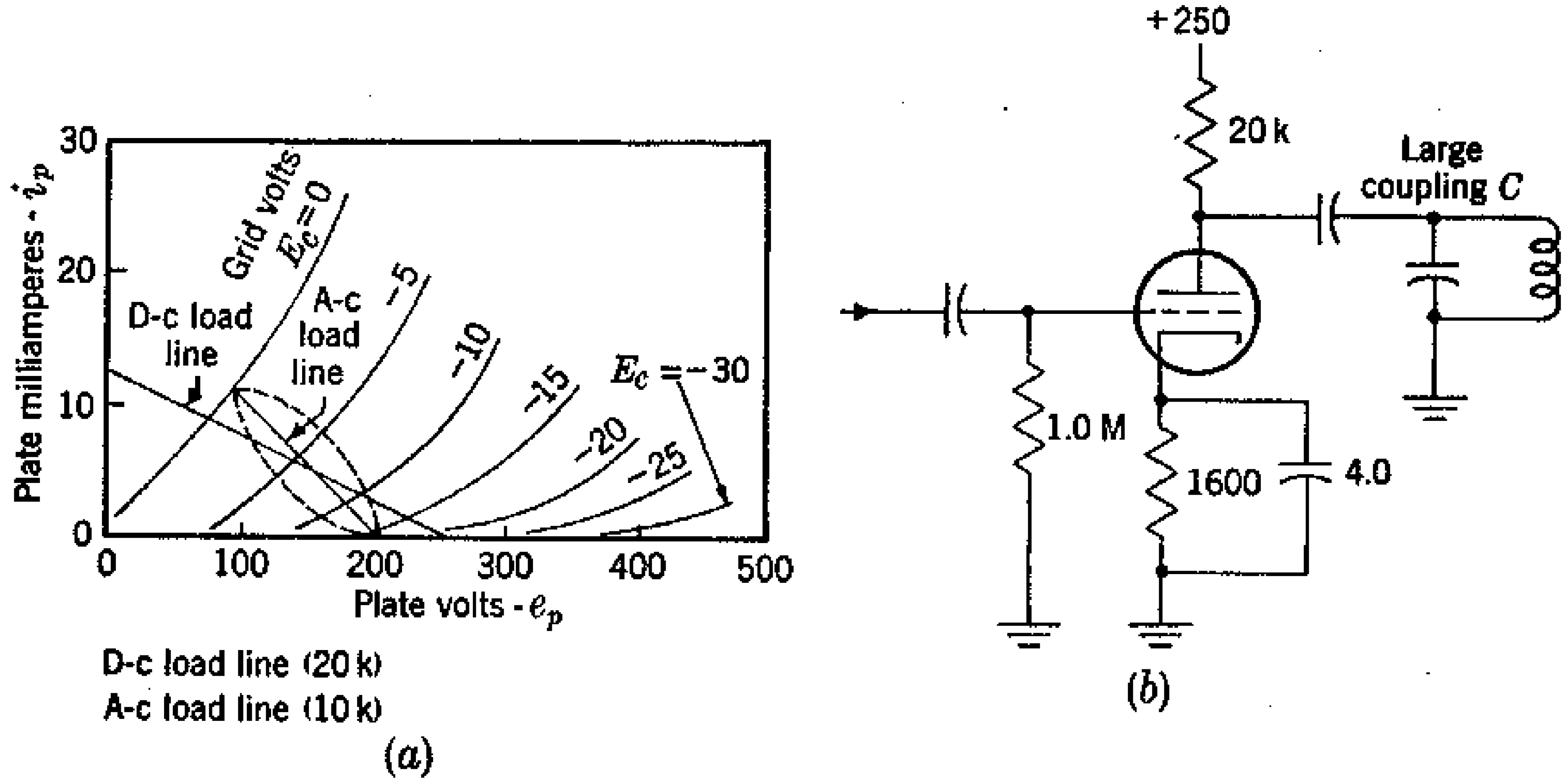

FIG. 9·15.—Operation of 6C4 output stage.

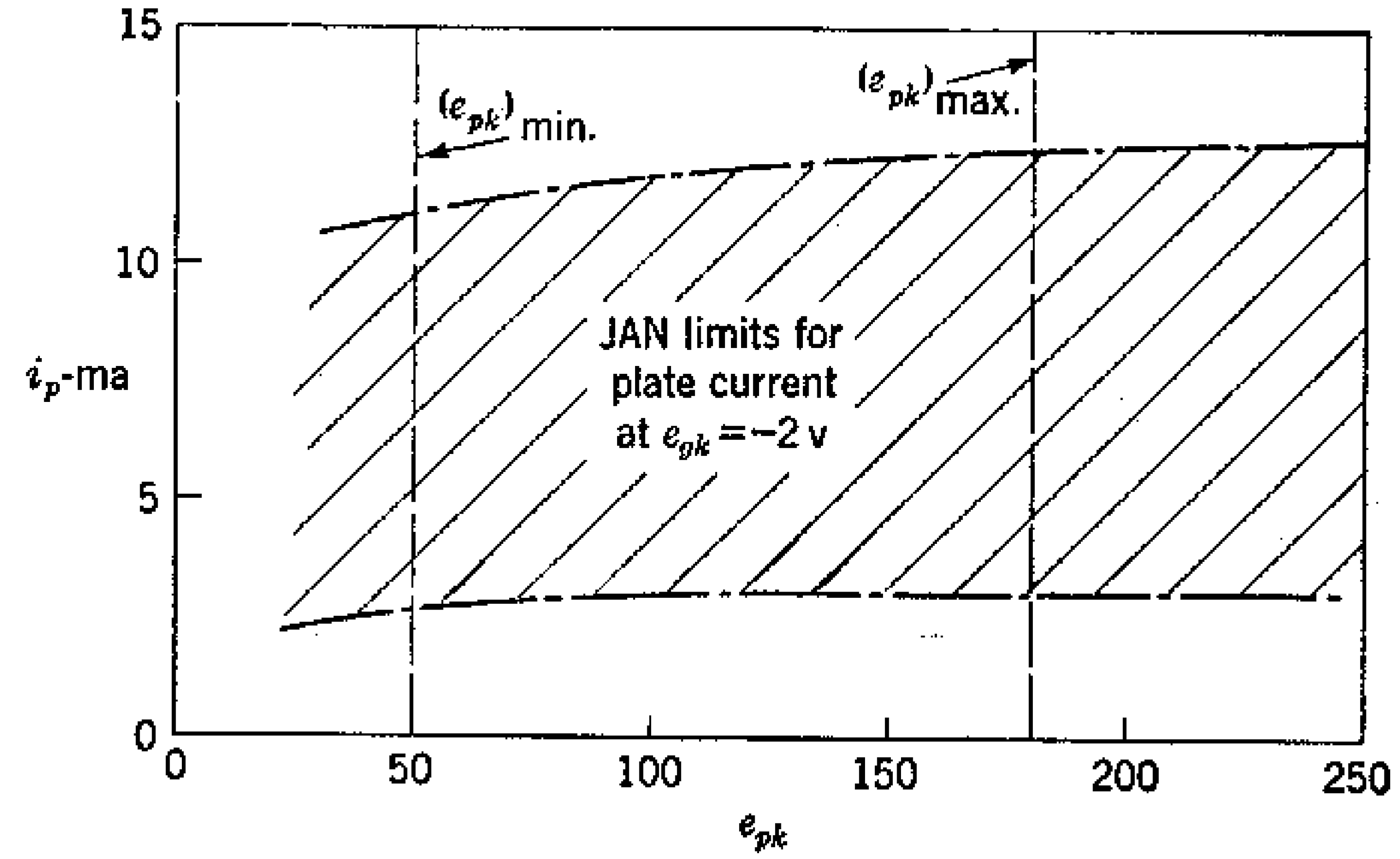

FIG. 9·16.—Type 6AK5 characteristic with tolerances.

9·8. Design of Pentode Stage.—Table 9·2 shows that the expected variations among 6AK5's are somewhat greater than among 6C4's. Moreover, a maximum plate voltage is specified for the 6AK5. In selecting electrode voltages it is helpful to use characteristic curves that indicate the tolerances of tube performance (Fig. 9·16). From the plate-current and screen-current specifications on the 6AK5, it can

[1] See Appendix B.

be concluded that the spread of the tube characteristics is roughly equivalent to a change in grid bias of ± 1 volt. This restricts possible designs that use fixed bias, as can be seen from Fig. 9·17*a*. This graph shows that a plate-load line drawn from a sufficiently large supply voltage will include undesirable operating regions for some tubes if the bias is -2 volts. For example, either the operating point will be near the "knee" of the pentode curves in the case of high-current tubes, or the plate voltage will exceed the absolute maximum rated value in the case of low-current tubes. (The value of 180 volts shown in Fig. 9·17 is actually a design-center value, but it serves to illustrate the point.) Thus, there is a maximum plate-supply voltage at which a particular

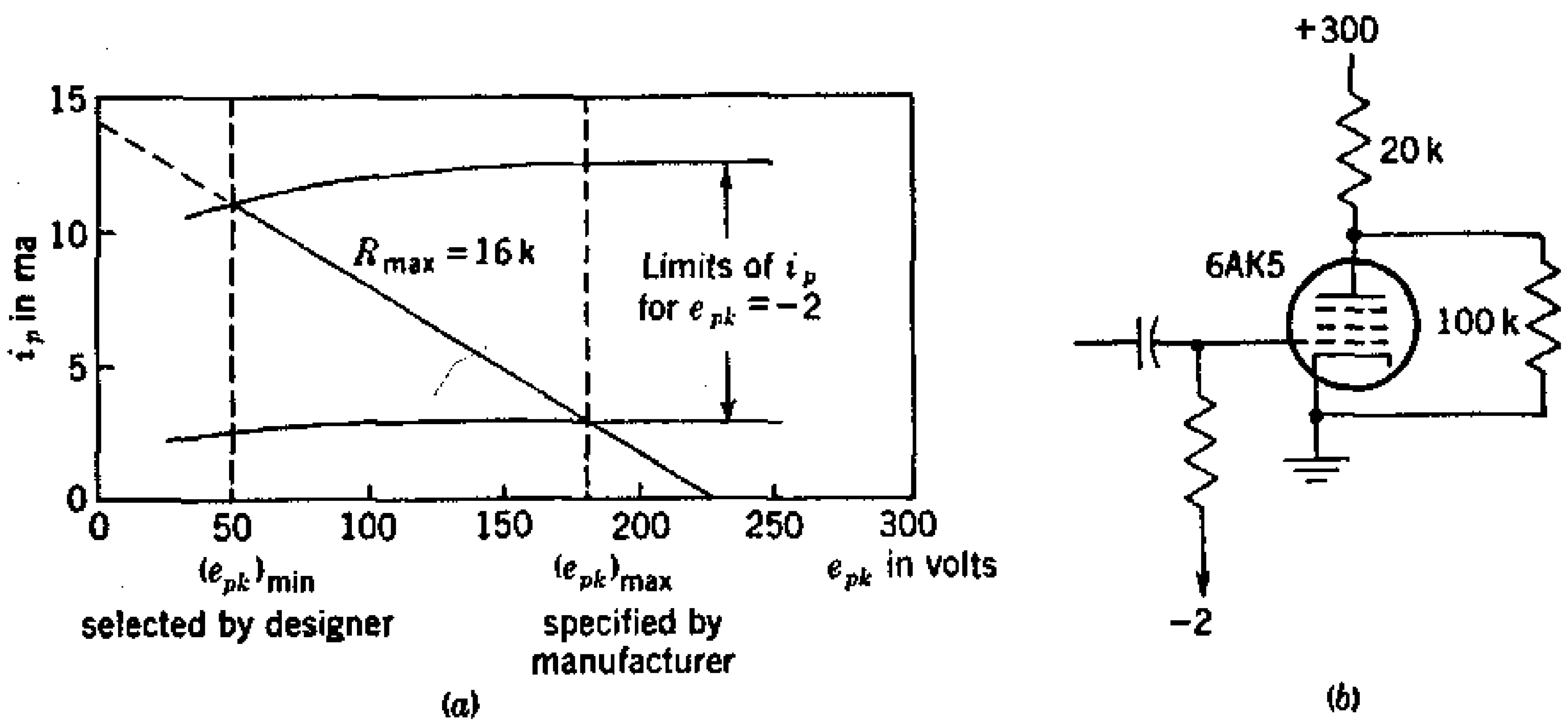

FIG. 9·17.—Tolerances and selection of plate load. (*a*) Type 6AK5 characteristic; (*b*) amplifier with bleeder resistor.

fixed bias can be used. If it is desired to operate the tube at fixed bias and to use a higher-voltage plate supply than this, the plate resistor can be replaced by a bleeder from B^+ to ground (Fig. 9·17*b*).

In the design to be described in this section a cathode resistor will be used to stabilize the tube characteristics. For the stabilization of i_p it is convenient to use the $i_p - e_g$ diagram together with the relation $e_g = -i_pR_k$ graphically expressed as a "load line" (Fig. 9·18*a*). It is seen that the spread of i_p for different tubes is considerably reduced from the spread at fixed bias by the use of a cathode resistor of the proper value. The optimum value is determined by a compromise between the fact that the plate-current stabilization is greatest for high R_k and the fact that the correlation between a fractional change in i_p and a given fractional change in g_m becomes less at low values of plate current. If linear characteristics are assumed (Fig. 9·18*b*), the "stabilization factor," the ratio by which the i_p spread is reduced, can be derived. From the geometry, $(A - B)/B = (A/B) - 1 = g_mR_k$. Therefore,

$$\frac{B}{A} = \frac{\Delta i_{p\ \text{cathode bias}}}{\Delta i_{p\ \text{fixed bias}}} = \frac{1}{1 + g_mR_k}. \tag{41}$$

This is an approximate measure of the reduction of the effect of tube replacement. Similar results are obtained when a combination of fixed bias and cathode bias is used. Analogous considerations also apply to variations of heater voltage (Sec. 10·5, Fig. 10·16). The objects of stabilizing i_p are to keep the plate voltage within rated limits and to reduce the variation of g_m and therefore the variation of gain. Complete

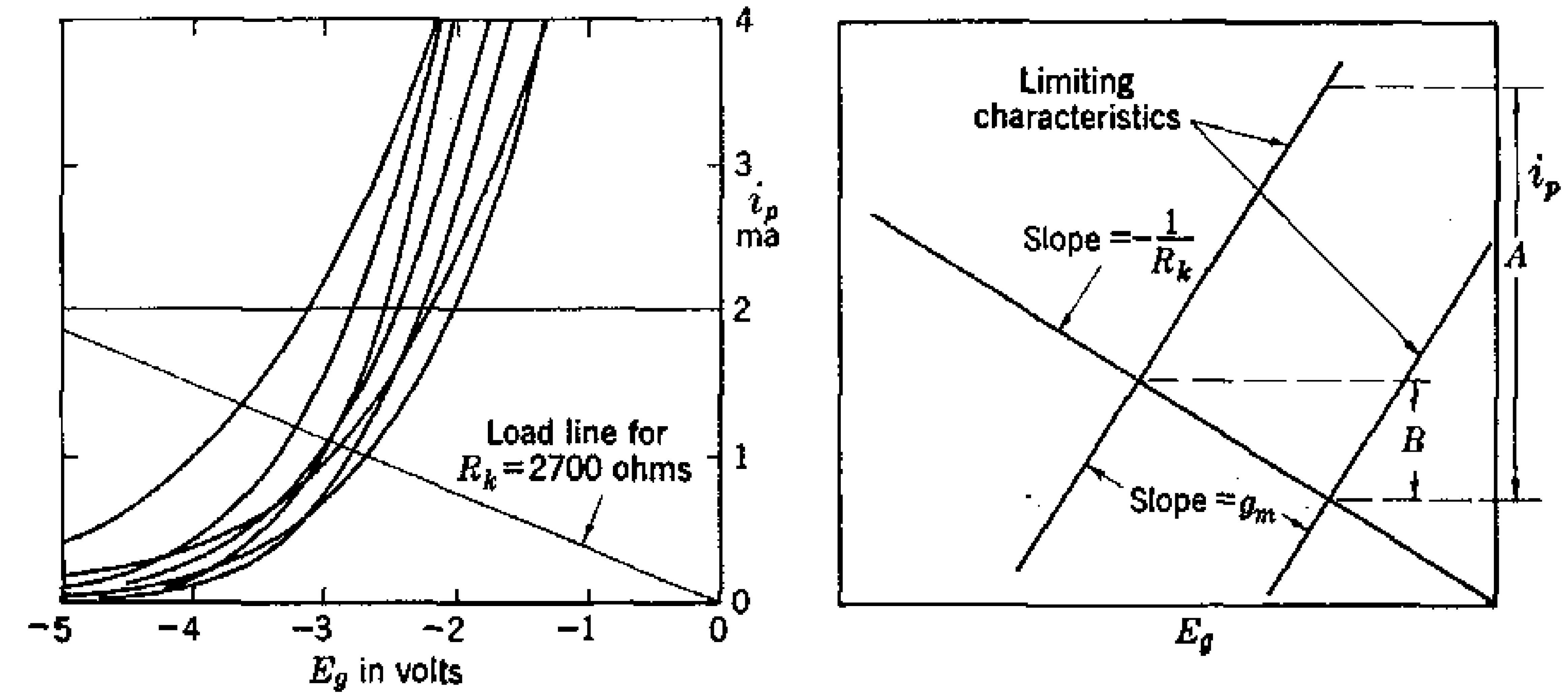

FIG. 9·18.—Stabilization of plate current by cathode resistor. (*a*) Mutual characteristics of several type 6AK5's, $E_p = E_s = 90'$, $E_f = 6.3'$, four different manufacturers; (*b*) idealized characteristics, A = spread of i_p, with fixed bias, B = spread of i_p with cathode bias.

data on the g_m-i_p correlation are not available; the curves of Fig. 9·18*a* indicate the extent of g_m variation. The variation in plate voltage is R_1 times the i_p variation, as is seen from the i_p-e_p diagram.[1]

The screen bias must also be considered. The criteria for the choice of the operating point are the maximization[2] of g_m/i_p and the minimization of plate dissipation. Table 9·3 shows that other things being the same, the smallest values of i_p/g_m (highest gain) are obtained at low screen bias and high (negative) grid bias. It would be desirable to obtain data on 6AK5's beyond the printed characteristics, but in

[1] There is a more elegant over-all geometrical representation of this. If the function $i_p(e_p,e_g)$ for fixed screen voltage is represented as a surface in three dimensions, the Ohm's law relations affecting e_p and e_g may be represented by two *load planes.*

[2] For given values of plate supply voltage and d-c plate voltage, the gain of the stage is proportional to g_m/i_p. The reason for this is that the fixed drop across the d-c plate load is $E_{pp} - E_p = i_pR_L$, and the gain is $g_mR_L = g_m(E_{pp} - E_p)/i_p$. This assumes that R_L is the same for alternating current and for direct current.

their absence E_{g_1} is chosen equal to -3 volts, $E_{g_2} = 90$ volts. Since $i_p = 1.1$ ma, the cathode resistor will be 2700 ohms. The average screen current is 0.45 ma; the extent to which it will be stabilized with respect to tube variation by cathode bias is not known; the screen is

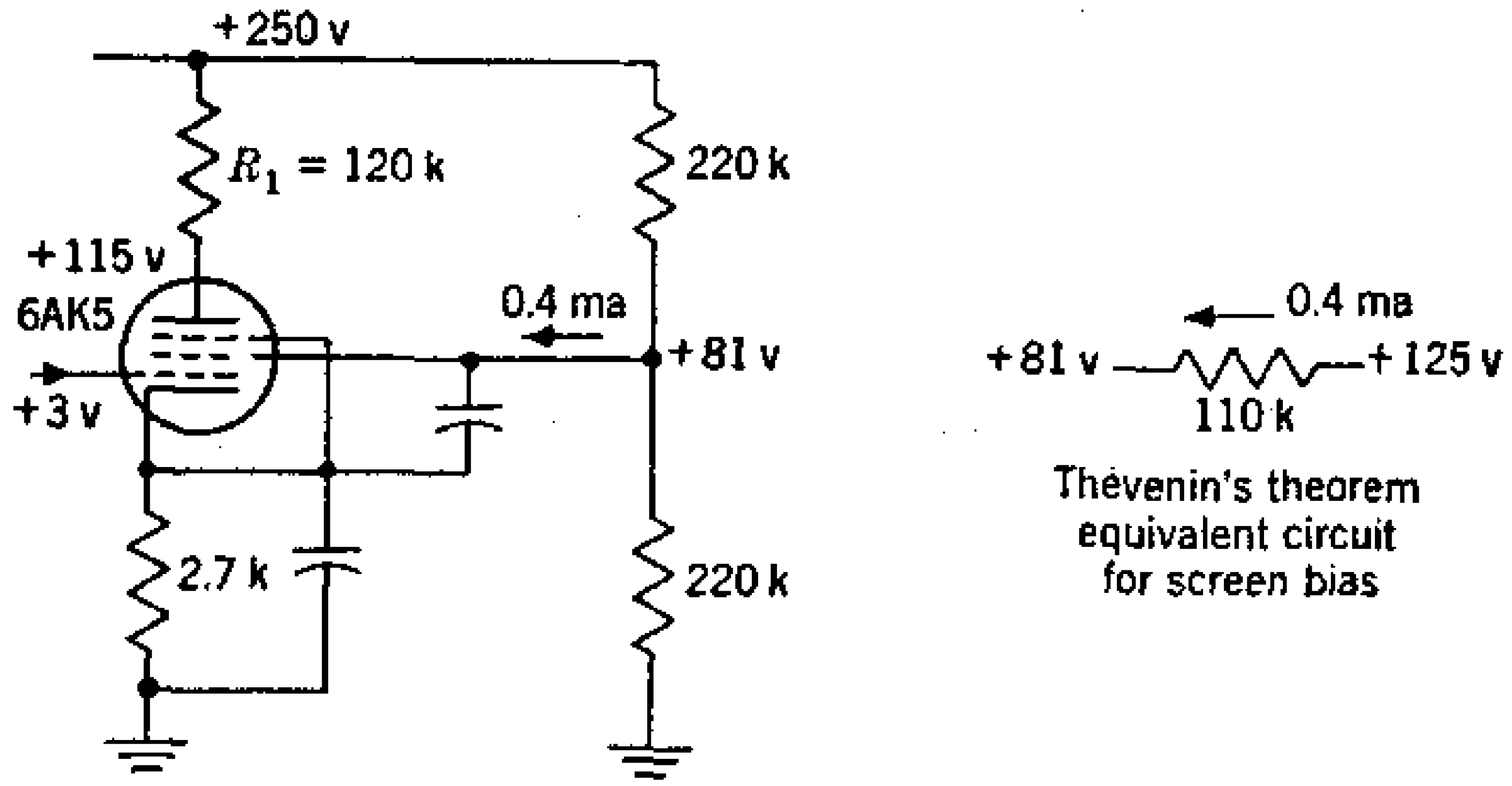

FIG. 9·19.—Preliminary design of pentode stage.

biased from an 0.6-ma bleeder. If the operating e_p is to be 115 volts (the center of the permissible range) and $B+ = 250$ volts, the load resistor R_1 will be $(250 - 115)$ volts/1.1 ma = 123 kilohms ≈ 120 kilohms. Therefore the circuit assumes the form shown in Fig. 9·19.

TABLE 9·3.—VALUE OF i_p/g_m FOR TYPE 6AK5 AS A FUNCTION OF GRID AND SCREEN VOLTAGES*

e_{c_1}, volts	e_{c_2}, volts	g_m, μmhos	i_p, ma	i_p/g_m, volts
−1	150	9000?	20.00	2.20
−2	150	7000	14.50	2.00
−3	150	5000	8.70	1.70
−4	150	3200	4.70	1.50
−1	120	7200	13.10	1.80
−2	120	4800	7.60	1.60
−3	120	2800	3.70	1.30
−4	120	1400	1.60	1.14
−1	90	4800	7.00	1.46
−2	90	2800	3.00	1.07
−3	90	*1300*	*1.10*	*0.85*
−4	90	400	0.25	0.63
−1	60	2700	2.10	0.78
−2	60	1000	0.40	0.40
−3	60	100?	0	
−4				

* Voltages from data in RCA *Tube Handbook.*

9·9. Constancy of Gain with Respect to Circuit Parameters.—The stabilization factor [Eq. (41)] for i_p and e_p is about 4.5, since

$$g_mR_k = 1300 \times 10^{-6} \times 2700 = 3.5,$$

and the value of 120 kilohms can therefore be used for the load resistor without causing e_p to depart from the desired region.

The sensitivity of over-all gain to component variation will now be calculated. The complete circuit at the present design stage is shown in Fig. 9·20. The d-c resistance of the resolver stator is 170 ohms, which is sufficiently small not to necessitate changing the cathode resistor of the first stage. If perfect bypass at 500 cps is assumed, the gain of the second stage may be expressed as $\mu Z_2/(r_p + Z_2)$ where Z_2 is the effective a-c load.

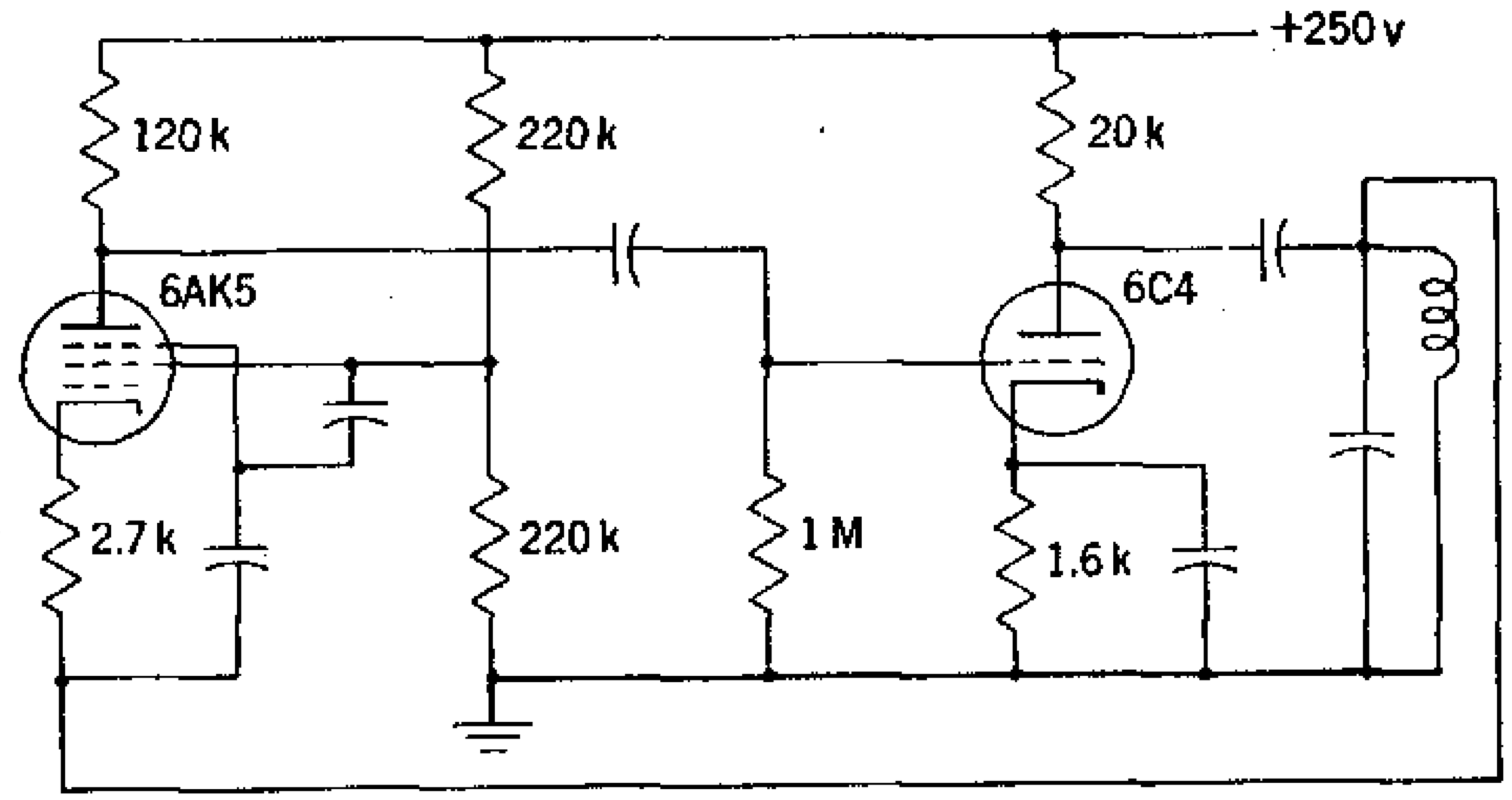

FIG. 9·20.—Driver circuit with tentative resistance values.

The gain of this stage, $\mathcal{G}_b$ in Eq. (9), can be calculated without considering the effect of the pentode stage. If e_i were zero, the cathode input impedance of the pentode would be $1/g_m$; actually the grid is varying more than the cathode, so that when the cathode rises, the current in T_1 *increases* slightly. This corresponds to a negative conductance in parallel with the load. Its effect is small, however, for the conductance is $g_m(e_k - e_i)/e_k \approx -g_m/300$ using an experimental value of $(e_k - e_i)/e_k$. Since $g_m = 1300$ μmhos, this is a negative resistance of $-300/(1300 \times 10^{-6})$ ohm or -230 kilohms in parallel with the 18-kilohm load. Since the 20-kilohm plate resistor is in parallel with this, the a-c load impedance is the parallel combination of all three of these resistances, or 10 kilohms. Using $r_p = 10$ kilohms, the gain of the second stage is

$$\mathcal{G}_b = \frac{\mu Z_2}{r_p + Z_2} \approx \frac{16 \times 10k}{10k + 10k} \approx 8. \tag{42}$$

The expressions developed for cathode feedback in Sec. 9·2 can now be applied. In this circuit $\beta = 1$. Equation (9) then assumes the form

$$\frac{1}{\mathcal{G}} - 1 = \frac{1}{\mu} + \frac{1}{\mathcal{G}_b}\left(\frac{1}{\mu} + \frac{1}{g_m R_L}\right), \tag{43a}$$

where β = feedback ratio
$\mathcal{G}$ = amplifier gain with feedback,
$\mathcal{G}_b$ = gain of second stage,
R_1 = a-c load of first stage,
μ, g_m = variational characteristics of first stage.

There is an additional network not considered in the previous analysis, namely, the screen-biasing circuit coupled to the first cathode. If the first cathode resistor could be considered as completely bypassed, this would merely be a high impedance in parallel with the load and as such

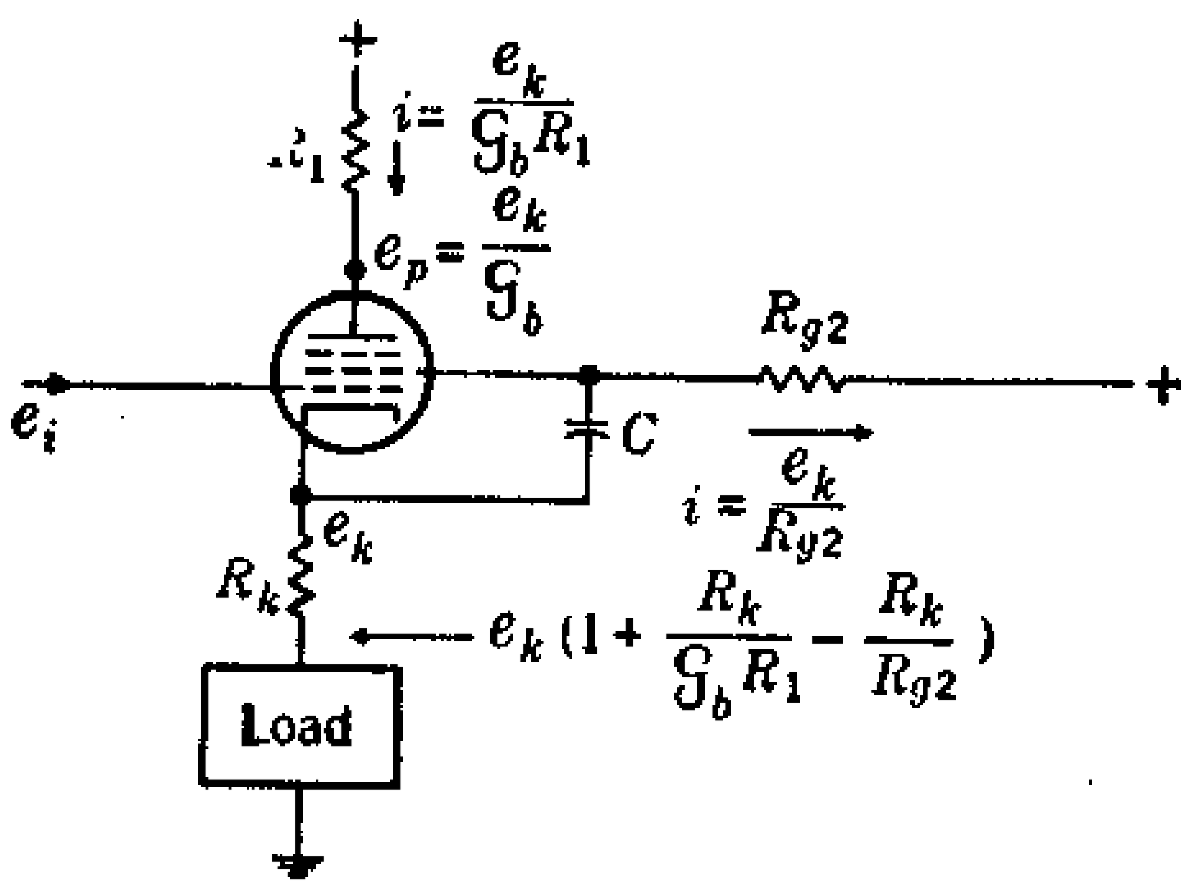

FIG. 9·21.—Pentode stage with unbypassed cathode resistor. Arrows indicate directions of currents in plate and screen circuits assuming e_i and e_k positive.

could be neglected. If the first cathode is not bypassed, additional terms are introduced into Eq. (43a), which then becomes

$$\frac{1}{\mathcal{G}} - 1 \approx \frac{1}{\mu} + \frac{1}{\mathcal{G}_b}\left(\frac{1}{\mu} + \frac{1}{g_m R_1}\right) + \frac{R_k}{\mathcal{G}_b R_1} - \frac{R_k}{R_{g_2}}. \tag{43b}$$

where R_{g_2} is the Thévenin's-theorem equivalent screen-biasing resistance. The origin of the two new terms may be clarified by reference to Fig. 9·21. The feedback holds e_k at nearly its former value, but the plate current and the current through R_{g_2} now flow through R_k, changing the output voltage accordingly. In this case, by choice of R_{g_2} and R_k, the over-all gain can be made to center at unity rather than at some smaller value, although the sensitivity to $\mathcal{G}_b$, g_m, and μ will not be decreased thereby.

Substituting circuit values in Eq. (43a),

$$\frac{1}{\mathcal{G}} - 1 = \frac{1}{1300} + \frac{1}{8}\left(\frac{1}{1300} + \frac{1}{1.3 \times 160}\right).$$

Now, although both the exact tolerances of μ and g_m and the correlation of g_m with i_p are unknown, it can be seen that the term $1/(8 \times 1300)$ is relatively negligible, and the expression may be written as

$$\frac{1}{\mathcal{G}} - 1 \approx \frac{1}{1300} + \frac{1}{1660}.$$

Even if each of these quantities is subject to a 40 per cent variation, the variation in $1/\mathcal{G}$ will not exceed 0.1 per cent. Therefore the loop gain seems sufficient.

9·10. Stability Against Oscillation.—The loop gain that is important for this problem is found by breaking the loop between the first and second stages, and holding the first grid at a-c ground.[1] In this case the second stage is operating into the low input impedance at the cathode of the first stage. This input impedance is affected by the screen circuit as well as by the plate circuit; it is

$$\frac{1}{g_{m_1} + g_{12}} = \frac{1}{1300 + 500} \times 10^6 \text{ ohms} \approx 550 \text{ ohms}.$$

The gain of the second stage therefore may be expressed roughly as $g_{m_2}/(g_{m_1} + g_{12})$,
where g_m = grid-plate transconductance of the first stage,
g_{12} = grid-screen transconductance of first stage,
g_{m_2} = transconductance of second stage.

The loop gain is the product of this quantity and the cathode-to-plate gain of the pentode, the latter being approximately $g_{m_1} R_{L_1}$, where R_{L_1} is the load resistance of first stage. Hence, if both cathodes are bypassed, the loop gain is

$$\mathfrak{A} = \frac{g_{m_2}}{1 + \frac{g_{12}}{g_{m_1}}} R_{L_1}. \tag{44}$$

It is also this factor which determines the reduction of extraneous voltages (B^+ ripple, for example) by the circuit.

Experimentally, the gain from the second grid to the first cathode with the loop open was found to be approximately one, in fair agreement with the predicted value 2000/1800. The loop gain with the loop open (experimentally) was about 100, and the predicted value was

$$\frac{2000}{1800} \times 120 \times 1.3 = 170.$$

The experiments mentioned were done with a 4-μf bypass capacitor in each cathode circuit.

[1] If the driver is used in another loop, however, the potential of the first grid will vary depending on the effect on it of the output through this loop.

Now that the loop gain at 500 cps is known, the next step is to consider shaping the response at higher and lower frequencies. (It is assumed for the present that the observed gain will suffice to reduce the effects of component variations.) Experimental curves of loop gain (amplitude and phase response) are shown in Fig. 9·22. The con-

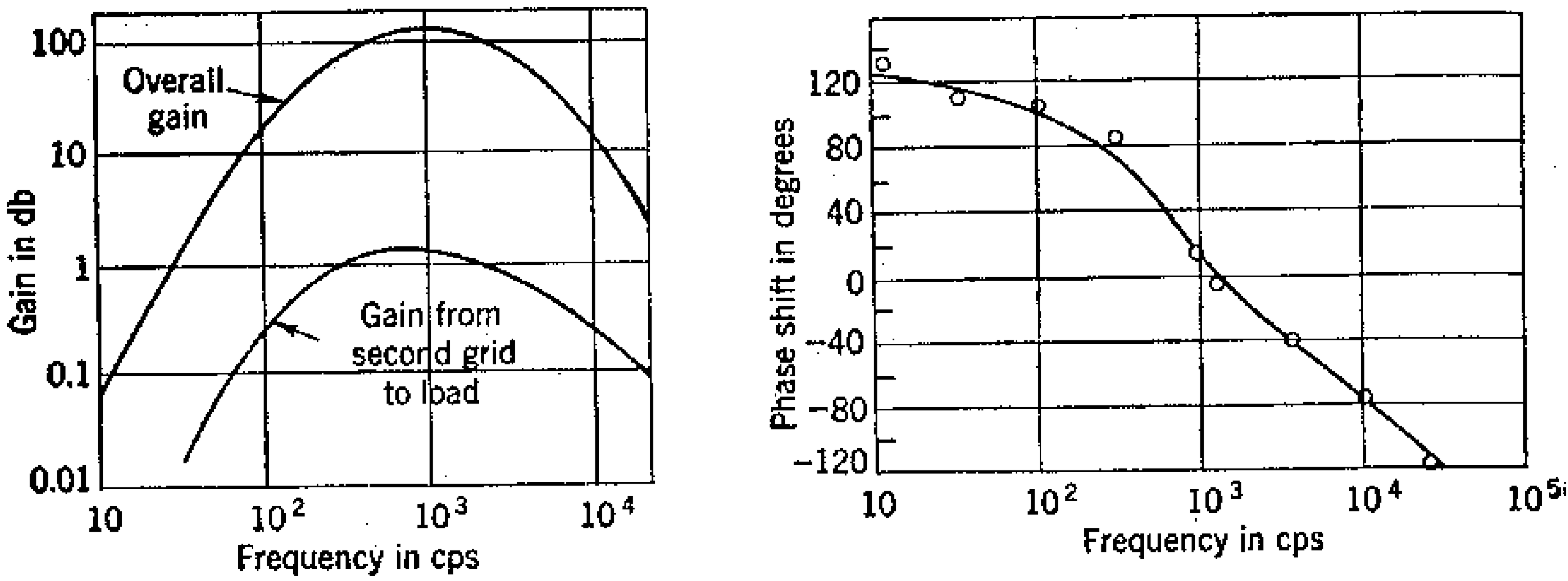

FIG. 9·22.—(a) Amplitude response of resolver driver with loop open; (b) phase response of resolver driver with loop open (experimental points).

denser values used are screen bypass, 4 μf; first-cathode bypass, 0.5 μf; both coupling condensers, 0.1 μf; second-cathode bypass 5.0 μf. It will be shown later that these values are satisfactory. The circuit tested was thus similar to that of Fig. 9·23. At low frequencies the circuit is like an LC-network and at high frequencies like an RC-network (whose phase shift approaches 90°), hence the different slopes at high

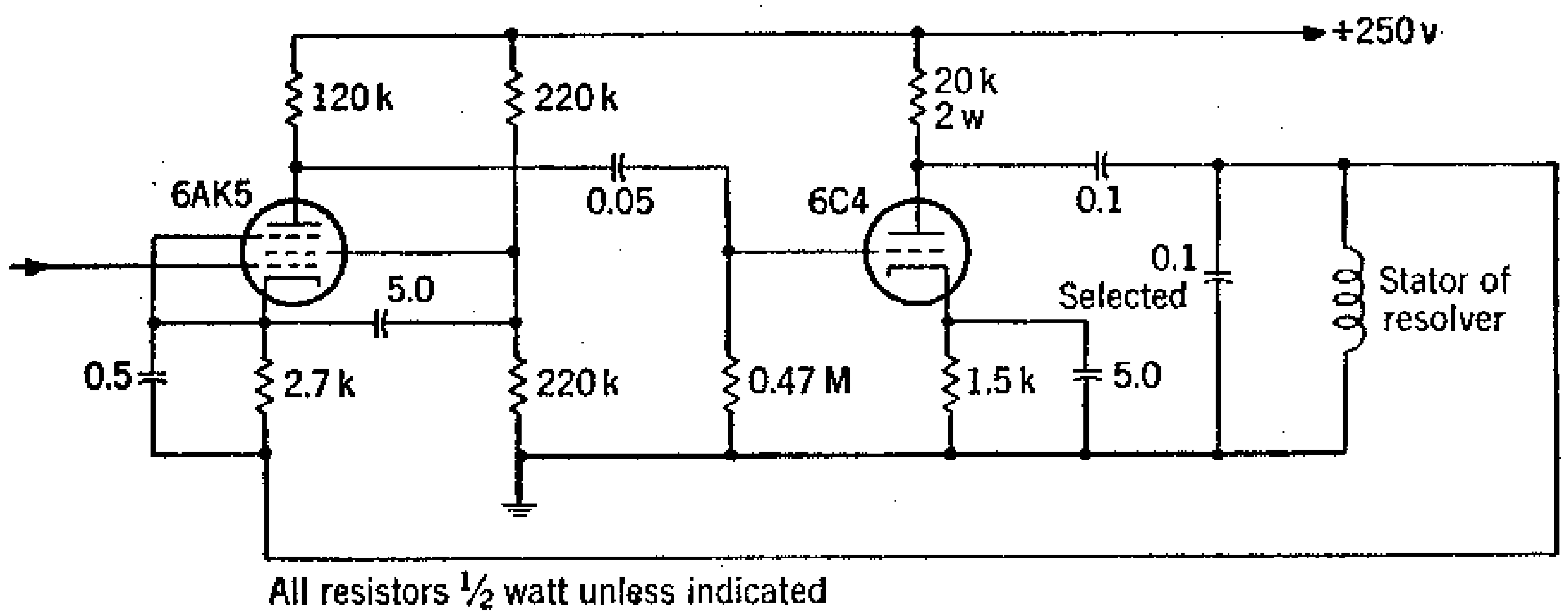

FIG. 9·23.—Final design of resolver-stator driver. All resistors ½ watt unless otherwise indicated.

and low frequencies of the curve in Fig. 9·22. The frequency at which the resolver-stator inductive reactance equals 600 ohms, which is the value of its resistance at 500 cps, is given by $2\pi f = R/L$, $f = 600/7 = 80$ cps. On the low-frequency side, unity gain is reached at about 30 cps (Fig. 9·22a). The frequency at which the RC-coupling network has 45° phase shift is $f = 1/2\pi RC$. If $R = 0.51$ megohm, and $C = 0.05$ μf, $f = 6.4$ cps. Thus the phase shift of the coupling network is effective only at frequencies at which oscillation cannot occur. The rest of the condenser values are also satisfactory in that it appears unlikely that any 180° phase shifts will occur within the region where the loop gain is unity or greater.

A method of determining the approximate values of bypass condensers is to select them so that their maximum phase-shift contributions occur at different frequencies.[1] If a 2.0-μf condenser is used to bypass the screen, the approximate frequency at which this produces maximum phase shift is

$$\frac{1}{2\pi C r_{g_2}} = \frac{1}{2\pi \times 2 \times 10^{-6} \times 30{,}000} \text{ cps} \approx 3 \text{ cps},$$

where it does not particularly influence the possibility of oscillation. (The screen variational resistance is r_{g_2}.[2]) The approximate effect of the cathode RC-circuits may be seen with the aid of a family of curves showing the falling off and phase shift in output voltages at low frequencies in a resistance-coupled amplifier.[3] The maximum phase shift caused by a phase-advance network (to which each of these is equivalent) is $2 \tan^{-1} \sqrt{p_2/p_1} - 90°$ [Eqs. (21) and (22), Fig. 9·6]. It is found experimentally by measuring the gains with the cathode condenser removed that the ratio of $(p_2/p_1) = (e_2/e_1)_\infty/(e_2/e_1)_0 = 4$ for the triode and $\frac{3}{2}$ for the pentode. The corresponding phase shifts are 37° and 12°. The choice of a 5.0-μf condenser to bypass the second cathode resistor puts the maximum phase shift of that network at about

$$\frac{1}{(2\pi \times 1500 \times 5 \times 10^{-6})} \text{ cps} \approx 21 \text{ cps}.$$

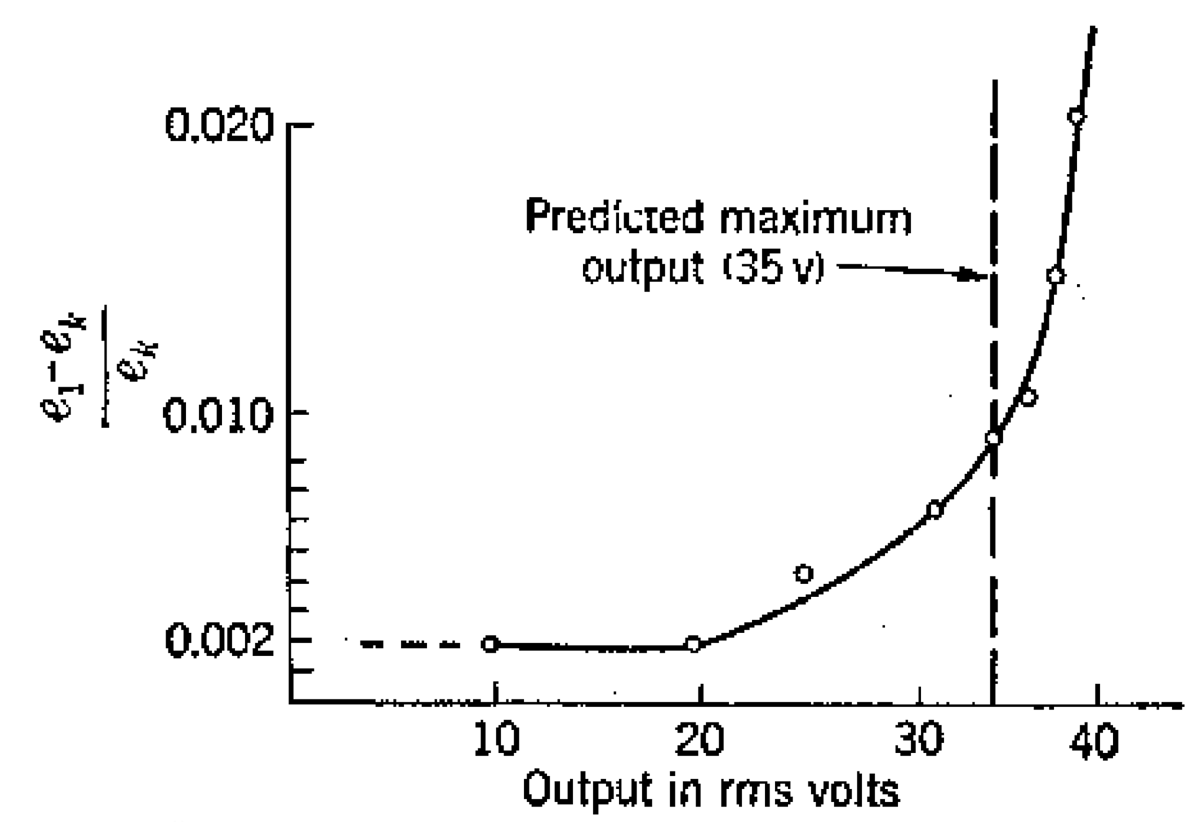

FIG. 9·24.—Fractional error voltage as a function of output voltage of second stage.

The phase-shift effect of the first cathode network may be put at a higher frequency, since the smaller maximum phase shift makes it possible to put the curve nearer to 500 cps without producing much phase shift or attenuation at 500 cps. If, for example, the value of RC is made to correspond to 100 cps,

$$C = \frac{1}{2\pi \times 100 \times 2700} \times 10^6 \ \mu\text{f} \approx 0.6 \ \mu\text{f}.$$

In these calculations, use has been made of the approximation that the maximum phase shift of the equivalent phase-advance network is at a frequency $1/(2\pi R_k C_k)$; actually this is the central frequency of one of the inverse-tangent curves, but for small phase shifts the error is not serious.

The final circuit design then assumes the form shown in Fig. 9·23. The difference between input voltage and output voltage may be measured by means of an oscilloscope, and the ratio of the peak value of this voltage to the peak value of the output voltage is plotted in Fig. 9·24 as a function of output voltage. Most of this difference voltage, in the region above 20 volts output voltage, corresponds to distortion resulting from cutoff of the second stage.

Up to an output voltage of 20 volts rms this amplifier approximately satisfies the original specifications. The fractional difference between output voltage and input voltage is 0.002; for this quantity to vary by 0.001, variations in component values must combine to produce a fractional variation in gain of at least $\frac{1}{3}$. The phase-shift condition is approximately satisfied, for even a loop phase shift of 48° (calculated for values of L and C at the extreme limits of the tolerances prescribed) would produce an over-all phase shift of only 0.002 sin 48° radian, or about 0.08°, as compared with the requirement of 0.06°.

Three-stage Amplifier for Resistive Load

9·11. General Considerations.—In the design of this amplifier it is desired to increase a voltage by a factor that will be adjustable about a mean value of 4.5 and that will remain constant to within ±0.1 per cent with respect to component variations. The input voltage is available from a relatively low-impedance source, and in order to save weight it is desired not to use transformers. A three-stage amplifier with resistive mixing is to be used (Fig. 9·1*a*).[1] The amplifier is to use miniature tubes. It is required to operate linearly to as high an output voltage as is possible with a given plate supply voltage.

Before selecting the tube types to be used, the loop gain necessary for the desired degree of constancy of over-all gain must be considered. For the purpose of calculating the loop gain $\beta\mathfrak{A}$ required, it is assumed that the loop gain will vary by ±40 per cent as a result of all component variations (±12 per cent peak variation for each stage). This assumption means that half the difference between the extreme values of $1/\beta\mathfrak{A}$, corresponding to the ±40 per cent variation of $\mathfrak{A}$ about a value $\mathfrak{A}_0$, must be 0.001 or less. This is expressed mathematically as follows:

$$0.001 \geqq \frac{1}{\beta\mathfrak{A}_0} \times \frac{1}{2}\left(\frac{1}{0.6} - \frac{1}{1.4}\right), \qquad \text{and} \qquad \beta\mathfrak{A}_0 \approx 500. \qquad (45)$$

[1] By variation of the mixing resistances, the circuit may also be used for multiplication or division with low output impedance.

The voltage fed back to the first grid is 1/5.5 times the output voltage of the third stage, this attenuation being characteristic of resistive mixing; for if the ratio $R_B/R_A = 4.5$, the voltage at the first grid will be 4.5/5.5 times the input voltage plus 1/5.5 times the output voltage. Therefore the gain of the amplifier from first grid to third plate must be about $5.5 \times 500 = 2750$. If it is assumed that three similar stages are used, the gain of each would be $\sqrt[3]{2750} \approx 14$. This gain can probably be realized if three 6C4's ($\mu \approx 17$) are used, as shown in Fig. 9·25.[1]

If the load resistances of the three amplifier stages are large compared with r_p, the stage gains will be nearly equal to μ and will depend more

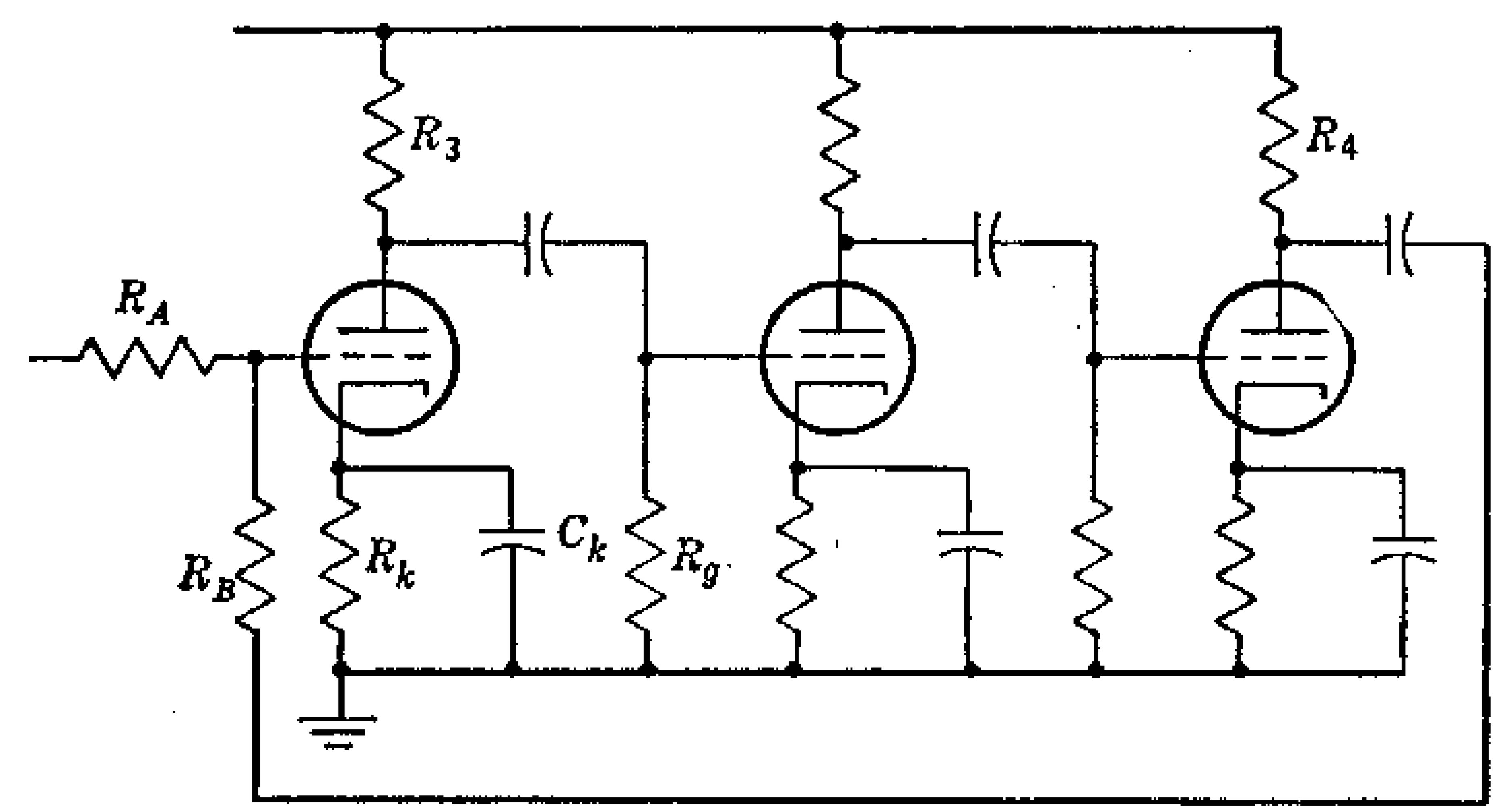

Fig. 9·25.—Schematic circuit of three-stage driver without stabilization networks.

on μ than on other circuit parameters; therefore the variation of μ with tube replacement and aging will be the principal source of error. Data on the variation of μ among 6C4's are given in the JAN specifications: The limits are 15.5 and 18.5 for $E_g = -8.5$ volts and $E_p = +250$ volts. If the equipment is assumed to be calibrated for a mean value of

$$\mu = 17.0 \pm 1.5,$$

the peak variation in μ per stage is then ±9 per cent.

9·12. Design of Individual Stages.—The first two stages can be identical, since they are both to operate at relatively low level. For a given plate current (limited by the permissible power drain from the plate supply) higher gain can be obtained at low plate voltage. Assume $I_p = 1$ ma, $E_p \approx 30$ volts, $E_{pp} = 250$ volts. The circuit constants may then be determined.

$$R_3 = \frac{(250 - 30)\text{ volts}}{1\text{ ma}} = 220{,}000 \qquad \text{ohms, an RMA value.}$$

[1] Alternatively, a pentode output stage might be considered in order to increase the maximum output voltage.

If the bias is -2 volts, then $R_k = 2$ volts/1 ma $= 2$ kilohms. The operating point on the 6C4 characteristics is shown in Fig. 9·26. The size of the cathode bypass condenser must be determined with some care, because it influences the phase shift at low frequencies and hence the possibility of oscillation. The bypass condensers will be given the smallest values that will provide satisfactory gain for each stage; these may be altered later when the question of oscillation is considered. The gain of a single triode stage is given by

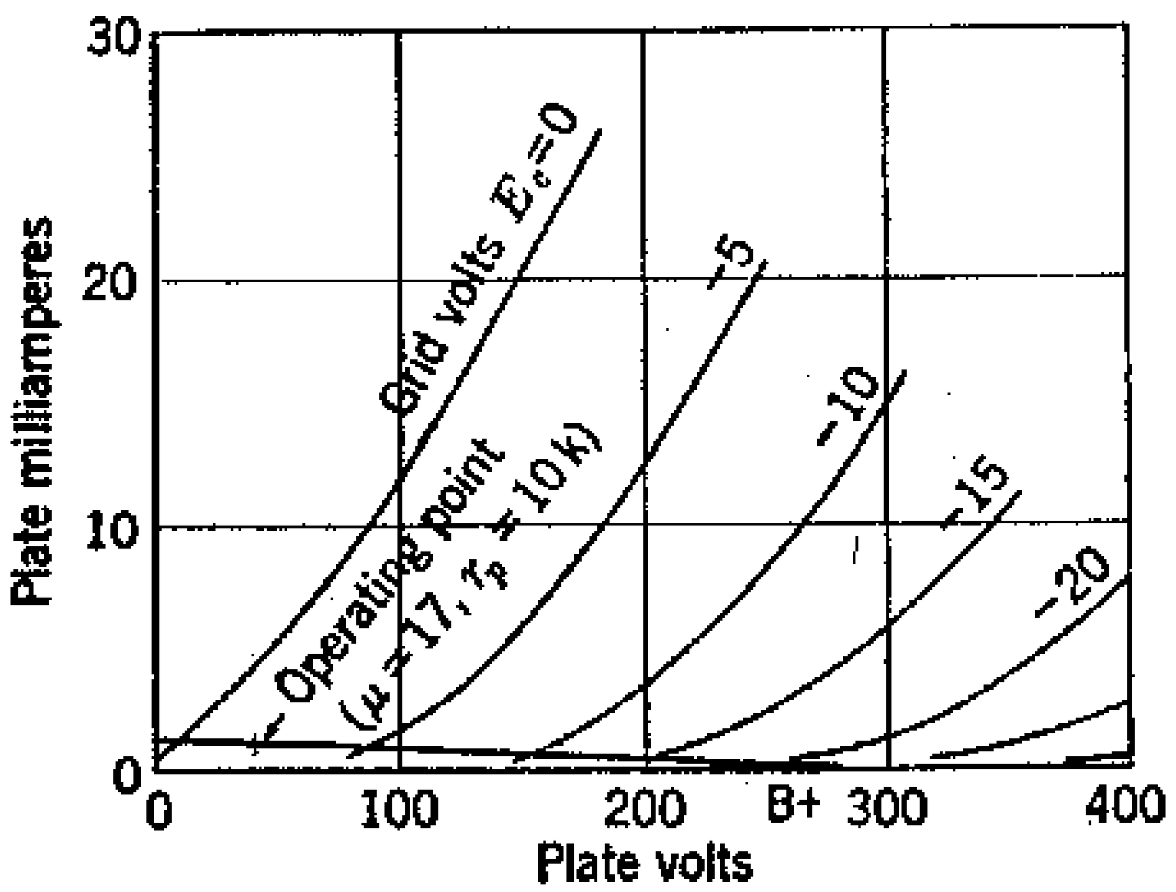

FIG. 9·26.—D-c operation of first and second 6C4 amplifier stages.

$$\mathrm{G}_1 = \frac{\mu}{1 + \dfrac{r_p}{R_L} + \dfrac{(\mu + 1)Z_k}{R_L}}, \qquad (46)$$

where R_L, the a-c load resistance, is the resistance of the parallel combination of R_3 and R_g (Fig. 10·25) and is assumed for the present to be 150 kilohms. The equivalent circuit is shown in Fig. 9·1*a*. The cathode impedance should be sufficiently small not to decrease the gain of a stage more than approximately 5 per cent. The condition that the reactance of $C_k/(\mu + 1)$ be 5 per cent of R_L is satisfied by

$$C_k = \frac{\mu + 1}{\omega R_L \times 0.05} = \frac{18}{2\pi \times 500 \times 150{,}000 \times 0.05} = 0.8 \quad \mu\text{f}. \qquad (47)$$

It may not be necessary to use this value of C_k to achieve the desired gain, because the effect of C_k adds in quadrature rather than directly. The gain of each of these stages, with no cathode degeneration, will be approximately

$$\frac{\mu}{1 + \dfrac{r_p}{R_L}} \approx \frac{17}{1 + \dfrac{10}{150}} \approx 16, \qquad (48a)$$

where the values $\mu = 17$, $r_p = 10$ kilohms are estimated average values at the operating point (Fig. 9·26).

The output of the third stage is condenser-coupled to the precision resistor R_B (Fig. 9·25). Since the circuit operation keeps the first grid near zero a-c potential, the a-c load line for the third stage has a slope corresponding to the parallel resistance of R_B and the d-c plate load R_4. The value of R_4 for maximum voltage output can be found from the expression[1] $R_4 = \sqrt{2r_pR_B}$, where $r_p \approx 10$ kilohms. This value of r_p is the estimated static plate resistance along the zero-bias line, since it is this quantity which enters into the derivation for maximum output. The value of R_B is determined by the availability of high-resistance precision wire-wound resistors. In this design the values $R_A = 100$ kilohms and $R_B = 450$ kilohms were chosen tentatively, although it might be possible to use higher values and thereby increase the output voltage. The value of R_4 is then $\sqrt{2 \times 10k \times 450k} \approx 100$ kilohms. The d-c operating conditions are shown in Fig. 9·28. A bias of about -7 volts (arrived at by drawing approximate load lines on the 6C4 characteristics with the object of maximizing the plate voltage swing) seems desirable. This corresponds to a plate current of about 1.0 ma, and $R_k \approx 6.8$ kilohms. A cathode-bypass condenser of about 1 μf will suffice for the third stage. The circuit then assumes the form shown in Fig. 9·27.

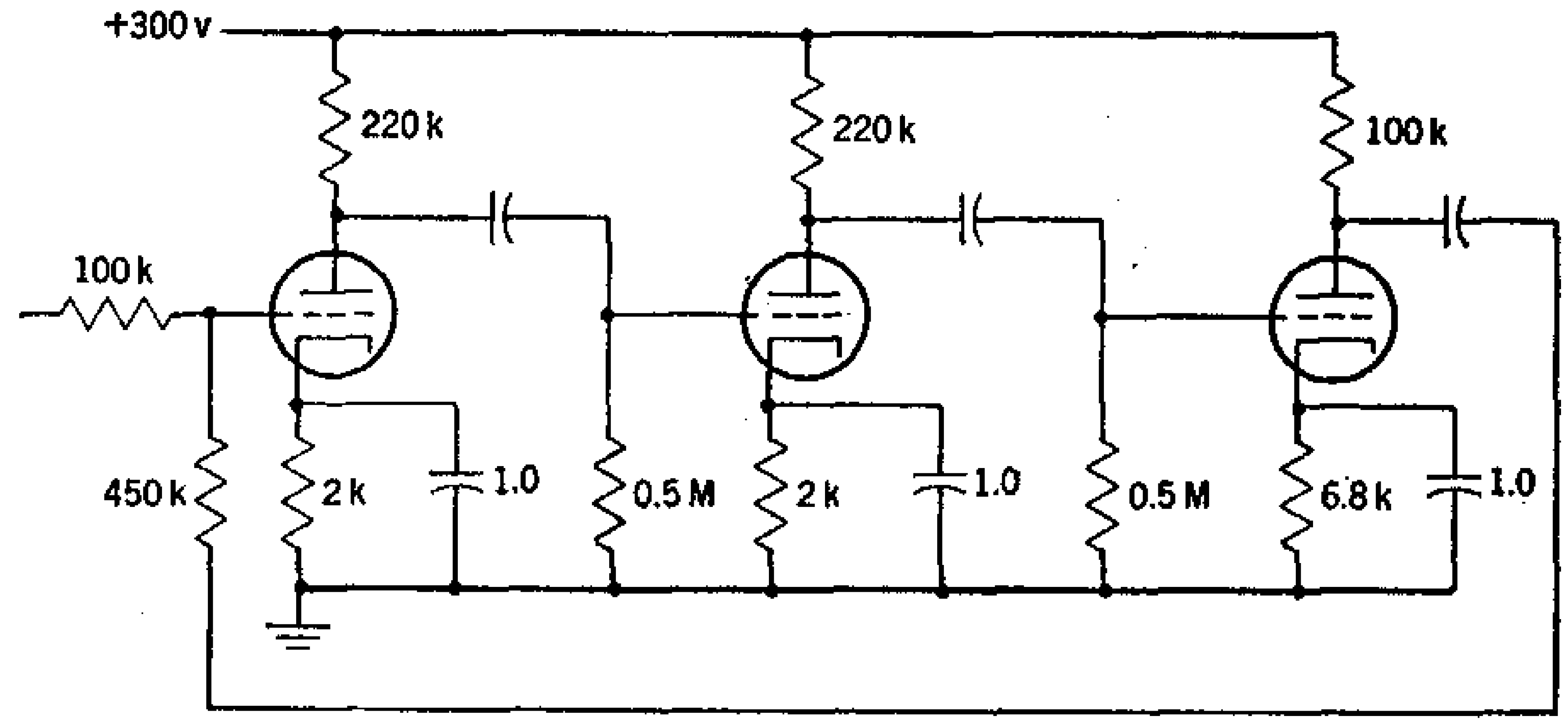

FIG. 9·27.—Preliminary design of three-stage driver exclusive of stabilization networks.

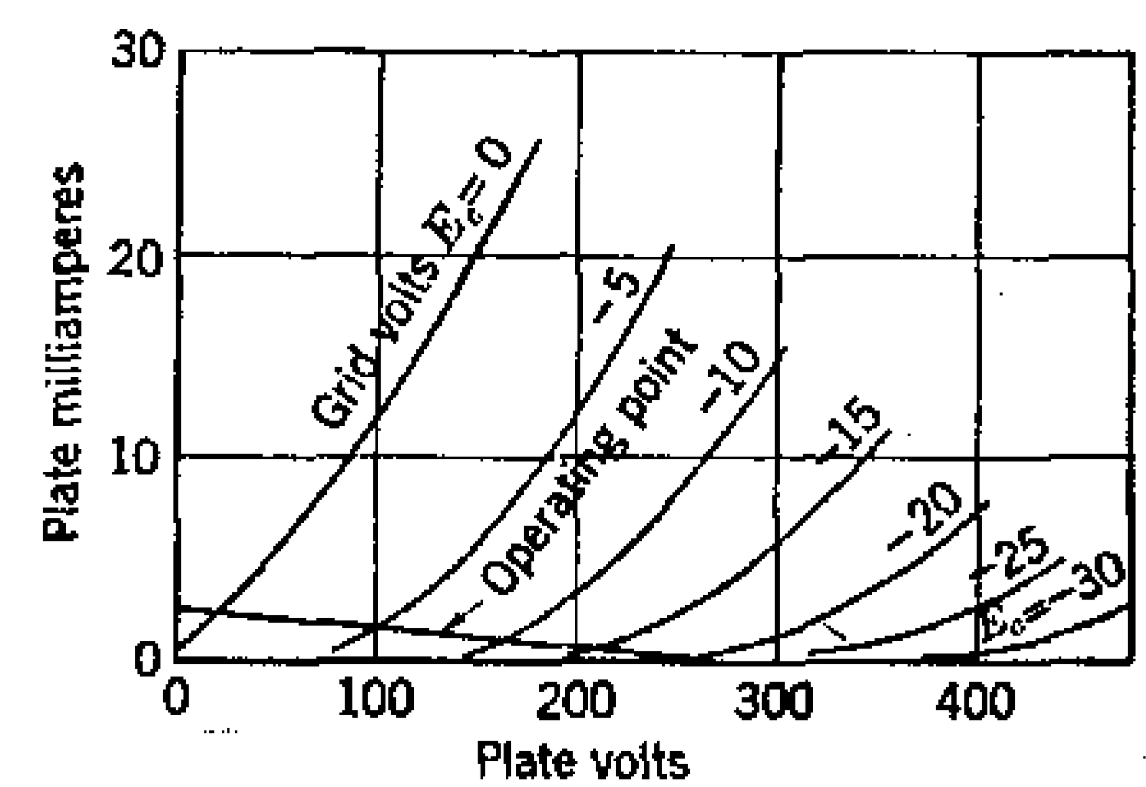

FIG. 9·28.—D-c operation of third amplifier stage.

The values of grid-leak resistors shown are trial values and are likely to be changed subsequently in the design of the stabilization networks. The gain of the third stage will be approximately

$$\frac{\mu}{1 + \dfrac{r_p}{R_L}} \approx \frac{14}{1 + \dfrac{25}{80}} \approx 11, \qquad (48b)$$

the values $\mu = 14$, $r_p \approx 25$ kilohms being estimated from the tube characteristics near the operating point as is shown in Fig. 9·28, and the value

[1] See Sec. 9·7 for derivation.

$R_L = 80$ kilohms being the parallel resistance of the d-c plate load (100 kilohms) and $R_B = (450$ kilohms). Therefore the expected over-all gain is $(16)^2 \times 11 \approx 2800$, and the loop gain $\mathcal{A}$ is about 500 (54 db).

9·13. Stability against Low-frequency Oscillation.—The frequencies at which the cathode-bypass networks produce maximum phase shift can be calculated approximately from the time constants R_kC_k. If the phase shift is small, the frequency of maximum phase shift is approximately that at which one of the RC-networks involved produces 45° phase shift, that is, the frequency at which the reactance of the capacity C_k equals the resistance R_k. For the network R_kC_k, this frequency is given by the equation

$$2\pi f R_k C_k = 1.$$

For the first two stages,

$$f \approx \frac{1}{2\pi R_k C_k} = \frac{1}{6.28 \times 2000 \times 1 \times 10^{-6}} = 80 \qquad \text{cps.}$$

For the third stage, the corresponding frequency is about 25 cps. The ratio of the gain with the bypass condenser to that without the condenser determines the maximum phase shift resulting from each cathode-bypass network; this corresponds to the ratio

$$\frac{\left(\dfrac{e_0}{e_i}\right)_{f=\infty}}{\left(\dfrac{e_0}{e_i}\right)_{f=0}}$$

of Eq. (22).

This gain ratio may be found from Eq. (46) for the gain of a triode amplifier with cathode impedance Z_k:

$$Z_k = R_k \qquad \text{at } f = 0,$$
$$Z_k = 0 \qquad \text{at } f = \infty;$$

therefore,

$$\frac{(\mathcal{G}_1)_{f=\infty}}{(\mathcal{G}_1)_{f=0}} = 1 + \frac{(\mu + 1)R_k}{R_L + r_p}.$$

For the first two stages this has the value

$$1 + \frac{18 \times 2k}{150k + 10k} = 1.22;$$

for the third it is

$$1 + \frac{15 \times 6.8k}{80k + 25k} = 1.97.$$

The corresponding maximum phase shifts, which in Eq. (21) are given by $\phi_m = 2(\tan^{-1}\sqrt{p_1/p_2} - 45°)$, are 5.6° for each of the first two stages and 16° for the third. The reductions in gain make the remaining stabilization problem somewhat easier, however, for they produce an attenuation of $1.97(1.22)^2 = 2.9$ at very low frequencies without producing an appreciable phase shift. Thus it can be considered that the loop gain that must be reduced to unity by the coupling networks at low frequencies is approximately $500/2.9 \approx 170$. At high frequencies the corresponding figure is 500.

In stabilizing the amplifier at low frequencies it should first be determined whether or not the desired response can be obtained with coupling networks, each consisting of a single resistance and capacitance. To save weight no coupling capacitor greater than 0.1 μf will be used. According to the *RCA Tube Handbook* the grid resistor should not exceed 1.0 megohm. In order to see if the desired response can be obtained in this way, the phase response of the respective RC coupling networks can be plotted and the frequency found at which 180° phase shift is obtained. It can be assumed that the low-frequency limit is determined by a time constant of 0.1 sec resulting from one coupling network whose constants have the maximum values given above. It is also assumed that the other coupling networks will not decrease the gain at 500 cps by more than 5 per cent. By a straightforward application of network analysis, the central frequencies f_1 of the other networks can be found.

$$\frac{1}{\sqrt{1 + \left(\dfrac{f_1}{500}\right)^2}} = 0.95,$$

or

$$\frac{f_1}{500} = \sqrt{0.1} = 0.3, \qquad f_1 \approx 150 \qquad \text{cps,}$$

where $f_1 = 1/2\pi RC$. Figure 9·29 shows the phase response of the loop in the case where a phase shift of 45° occurs at 150 cps for two of the coupling networks and at 1.6 cps for the third (corresponding to $R = 1$ megohm and $C = 0.1$ μf). The over-all phase shift other than that of the phase advance of the cathode-bypass networks reaches 180° at $f = 12$ cps; at this frequency the attenuation is approximately $(\frac{12}{150})^2 = 0.0064$. This does not quite suffice to reduce the gain to unity,[1] since

$$170(0.0064) = 1.1.$$

Some small alterations of circuit constants might suffice to reduce this value below unity; however, to provide a larger safety factor additional networks are used. The resulting design will therefore indicate how considerably higher gains may be stabilized. The introduction of a network of the type shown in Fig. 9·7 for low-frequency stabilization has the advantage not only of introducing an additional equivalent phase-advance network (which, as was shown, can attenuate without introducing phase shift at low frequencies) but also of moving the low-frequency limiting time constant to a lower frequency. The reason for this is that in the stabilization network of Fig. 9·7, the low-frequency phase response is determined largely by R_1C_1 as shown in Eq. (24c); the limitation on C_1 is still the same as for the single RC-network, but R_1 can be considerably larger, since it is not in the d-c grid-return path.

If the circuit is designed with three such networks, full advantage will be taken of this effect. The values of R_1 and C_1 used are 5.1 megohms

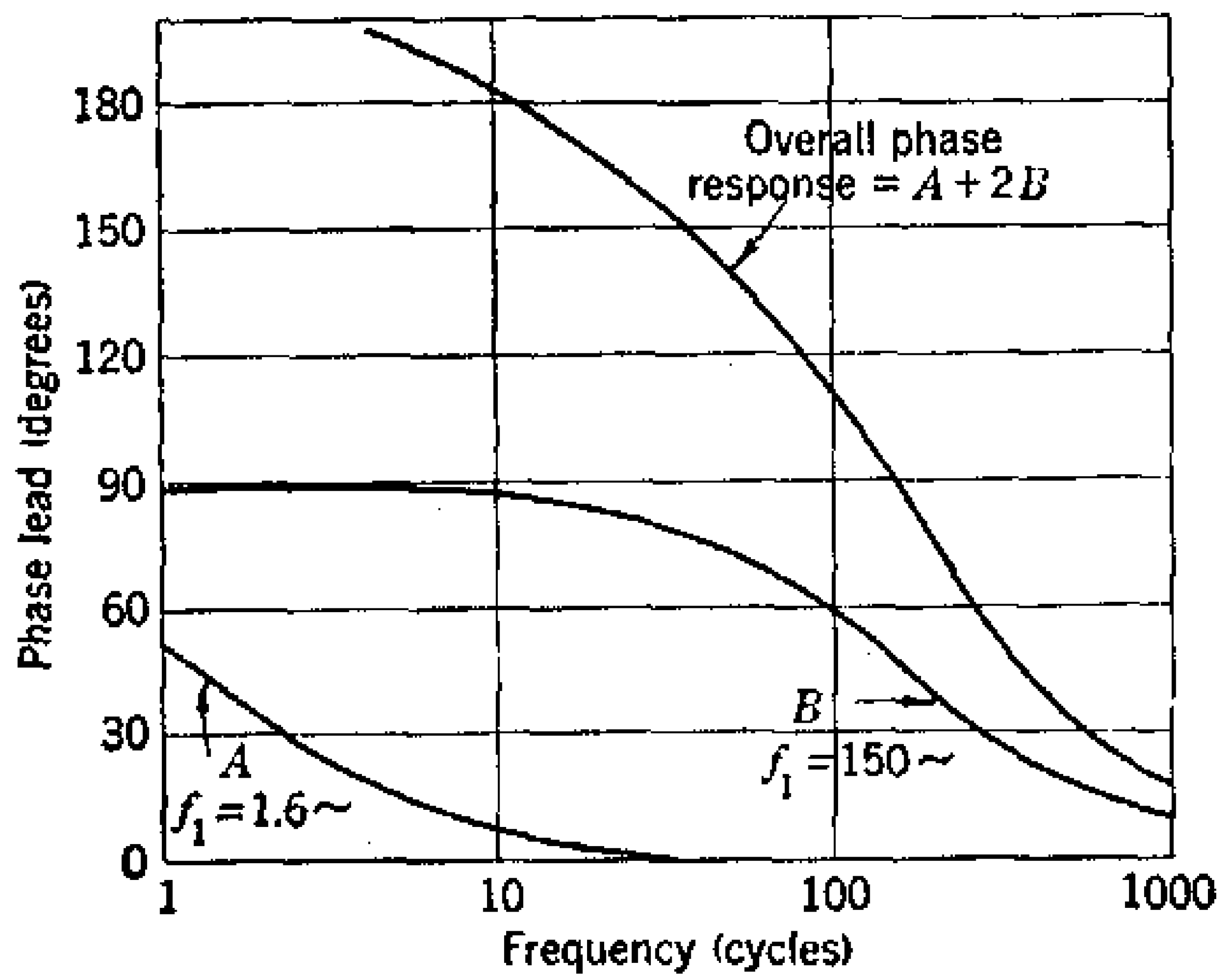

FIG. 9·29.—Phase response of three-stage driver (loop open) with single RC-coupling networks.

and 0.1 μf respectively, the resistance value now being limited only by possible leakage paths. The corresponding central frequency, $1/2\pi R_1C_1$, is 0.3 cps. The use of these networks affords the possibility of adding three phase-advance curves to the limiting curve, which is determined approximately by the R_1C_1's. The design procedure will be to choose these three curves so that they add to give an over-all phase response that rises fairly rapidly to about 150° phase shift (as the frequency is decreased from 500 cps) and remains in this vicinity until the limiting curve takes over and brings the phase shift to 180°. In this the designer may be guided approximately by the phase-area theorem.[1] This states that for networks whose gain changes from one fixed value at zero frequency to another at infinite frequency, the area under the phase-shift curve is proportional to the gain ratio. The theorem is applicable to phase-advance networks. In order to have a fast rise of phase angle with respect to frequency and to increase the phase area between 50 and 500 cps, at least two of the curves should have effect near 500 cps. It seems desirable that the third have effect at lower frequencies. A further restriction is that the two precision resistors at the input grid of the driver constitute part of the coupling network. This restricts the value of R_2 for this network because of the other requirements on R_B (see Fig. 9·25): that it have a high value in order to increase the maximum output but that it cannot be higher than a conveniently obtainable value for precision wire-wound resistors. The general nature of the desired phase response is shown in Fig. 9·30. This diagram

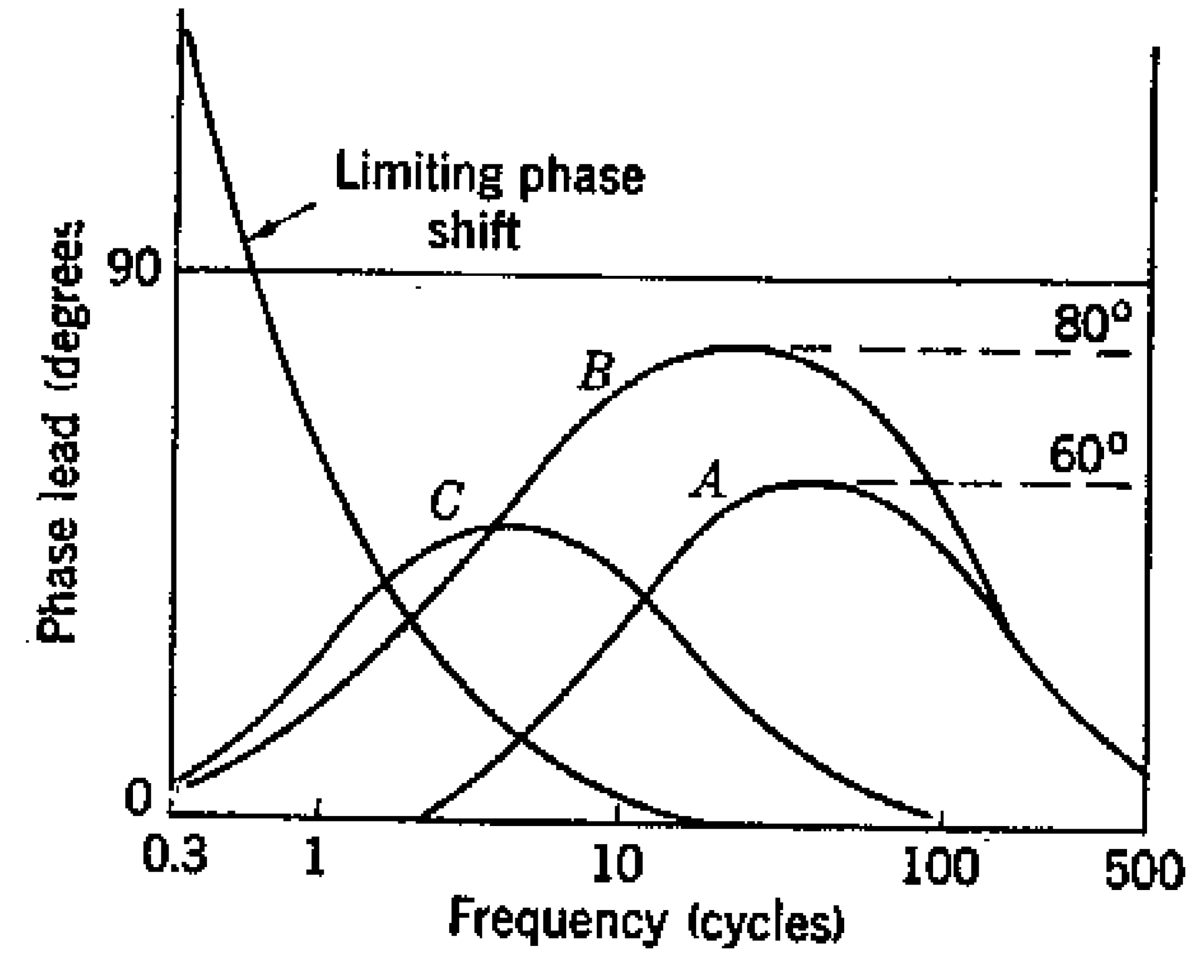

FIG. 9·30.—First approximation of synthesis of phase networks.

was arrived at by successive trials of different phase-advance curves. The following terminology is used: coupling network from first plate to second grid, Network A; from second plate to third grid, Network B; from third plate to first grid, Network C.

The procedure is to find the constants of networks having approximately the response sketched and then to calculate their properties more accurately. It has already been decided that R_1 = 5.1 megohms and $C_1 = 0.1\ \mu$f for each of the three networks. Furthermore, for Networks A and B the sharp rise from 500 cps necessitates[1] that $1/2\pi R_2C_2 \approx 110$, or $R_2C_2 = 0.0015$ sec. The only other information necessary to the design of the stabilization networks is the value of R_2/R_1 for each network, this ratio being approximately equal to p_2/p_1 for the phase-advance network. The expression $\phi_{\max} = 2(\tan^{-1}\sqrt{p_2/p_1} - 45°)$ [Eq. (21)] yields $p_2/p_1 = 14$ for $\phi = 60°$ (Network A) and 120 for $\phi = 80°$ (Net-

[1] It can be shown that if single RC-circuits are used to attenuate at high and low frequencies, the frequencies at which the output is $1/n$ of its maximum value ($n \gg 1$) are closest together if both RC products are equal to $1/\omega_c$, where ω_c is the design or computing frequency. This would mean setting $f_1 = 500$ cps if the amplifier had enough gain to spare a factor of $1/\sqrt{2}$ for each network.

TABLE 9·4.—CONSTANTS OF NETWORKS A AND B

Constant	Network A	Network B
R_1	5.1 megohms	5.1 megohms
C_1	0.1 μf	0.1 μf
R_2 (first approx.)	$\frac{5100k}{14} = 360k$	$\frac{5100k}{120} = 43k$
C_2 (first approx.)	$\frac{0.0015 \text{ sec}}{360k} = 0.0042\ \mu f$	$\frac{0.0015 \text{ sec}}{43k} = 0.035\ \mu f$
C_2 (final values)	0.005 μf	0.02 μf
R_2 (final values)	300k	75k

work B). The resulting constants are shown in Table 9·4. The reason for making a second approximation to R_2 is that the condenser C_2 is available only in values such as 0.01, 0.02, 0.05, and 0.1 μf. Thus, when the nearest C_2 has been selected, the time constant R_2C_2 is wrong as regards its effect at 500 cps. The procedure is to readjust R_2 to make R_2C_2 again equal to 0.0015 sec. The effect on the maximum phase shift of the phase-advance networks is small. The phase response of these two networks will now be plotted in order to determine more precisely what characteristics the third network should have. The roots p_i may be found from Eq. (24):

$$p_2 = -\left(\frac{1}{R_1C_1} + \frac{1}{R_1C_2}\right),$$

$$p_{3,4} = \frac{-\left(\frac{1}{R_1C_1} + \frac{1}{R_2C_2} + \frac{1}{R_1C_2}\right)}{2} \pm \sqrt{\frac{\left(\frac{1}{R_1C_1} + \frac{1}{R_2C_2} + \frac{1}{R_1C_2}\right)^2}{4} - \frac{1}{R_1R_2C_1C_2}}.$$

For Network A:

Roots	Corresponding frequency $= \frac{-p_i}{2\pi}$, cps
$p_2 = -41\ \text{sec}^{-1}$	6.5
$p_3 = -706\ \text{sec}^{-1}$	112
$p_4 = -1.85\ \text{sec}^{-1}$	0.29

Similarly, for Network B:

Roots	Corresponding frequency
$p_2 = -11.8\ \text{sec}^{-1}$	1.9
$p_3 = -676\ \text{sec}^{-1}$	108
$p_4 = -1.93\ \text{sec}^{-1}$	0.31

The corresponding inverse-tangent curves and their algebraic sum, including the curves for p_4 but not for p_2 or p_3 for Network C, are shown in Fig. 9·31. From this characteristic it appears that the third phase-advance network should have maximum phase shift at 1.6 cps and that this maximum should be approximately 50°. Therefore, from Fig. 9·6,

$$\sqrt{p_2p_3} = 2\pi \times 1.6 \text{ cps} = 10 \qquad \text{radians/sec},$$

and from Eq. (21)

$$50° = 2\left(\tan^{-1}\sqrt{\frac{p_3}{p_2}} - 45°\right) \qquad \text{or} \qquad \sqrt{\frac{p_3}{p_2}} = 2.75.$$

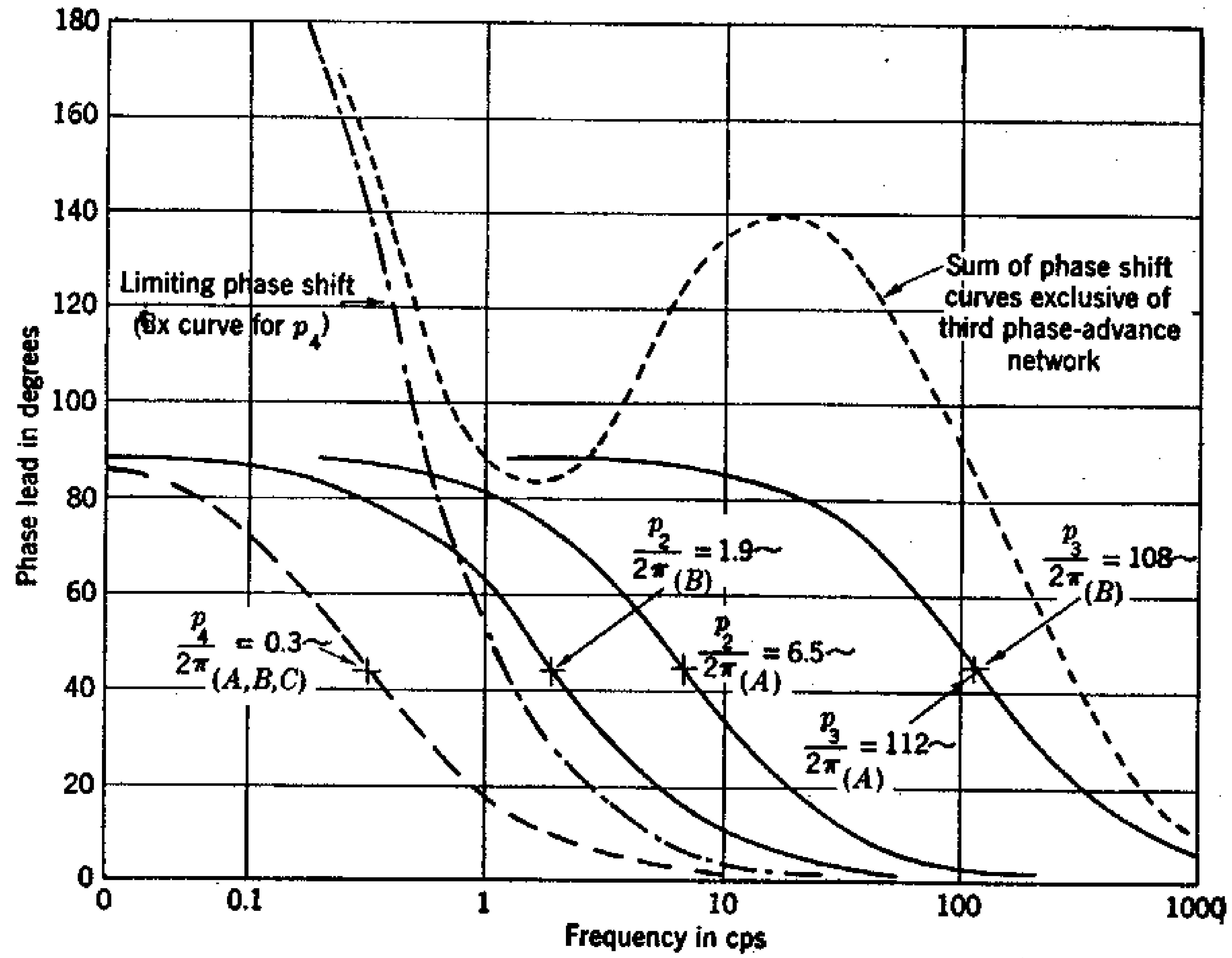

FIG. 9·31.—Phase characteristics for two stabilization networks.

Therefore, for Network C:

Roots	Corresponding frequency, cps
$p_2 = 3.6\ \text{sec}^{-1}$	0.57
$p_3 = 27.5\ \text{sec}^{-1}$	4.4

The constants of Network C may now be selected. It has already been decided that $R_1 = 5.1$ megohms, $C_1 = 0.1\ \mu f$. From the approximate versions of Eq. (24c),

$$p_2 \approx \frac{1}{R_1C_2}, \qquad p_3 \approx \frac{1}{R_2C_2}.$$

Therefore, approximately,

$$C_2 = 0.055\ \mu f \text{ (use } C = 0.05\ \mu f\text{)},$$
$$R_2 = 680 \text{ kilohms}.$$

Finally, for one of these networks, the sum of the resistances of the precision resistors at the input terminals of the driver constitutes R_2. Therefore, the procedure will be to specify values for these resistors consistent with the low-frequency-stabilization design. A satisfactory solution is to use the values of 550 and 125 kilohms, which add to 675 kilohms and have the ratio 4.4. The calculated over-all phase-shift characteristic for the three networks *A*, *B*, and *C* is shown in Fig. 9·32. The phase margin afforded is 20° over a frequency range extending down to 0.5 cps. The attenuation at 0.5 cps due to the three networks can

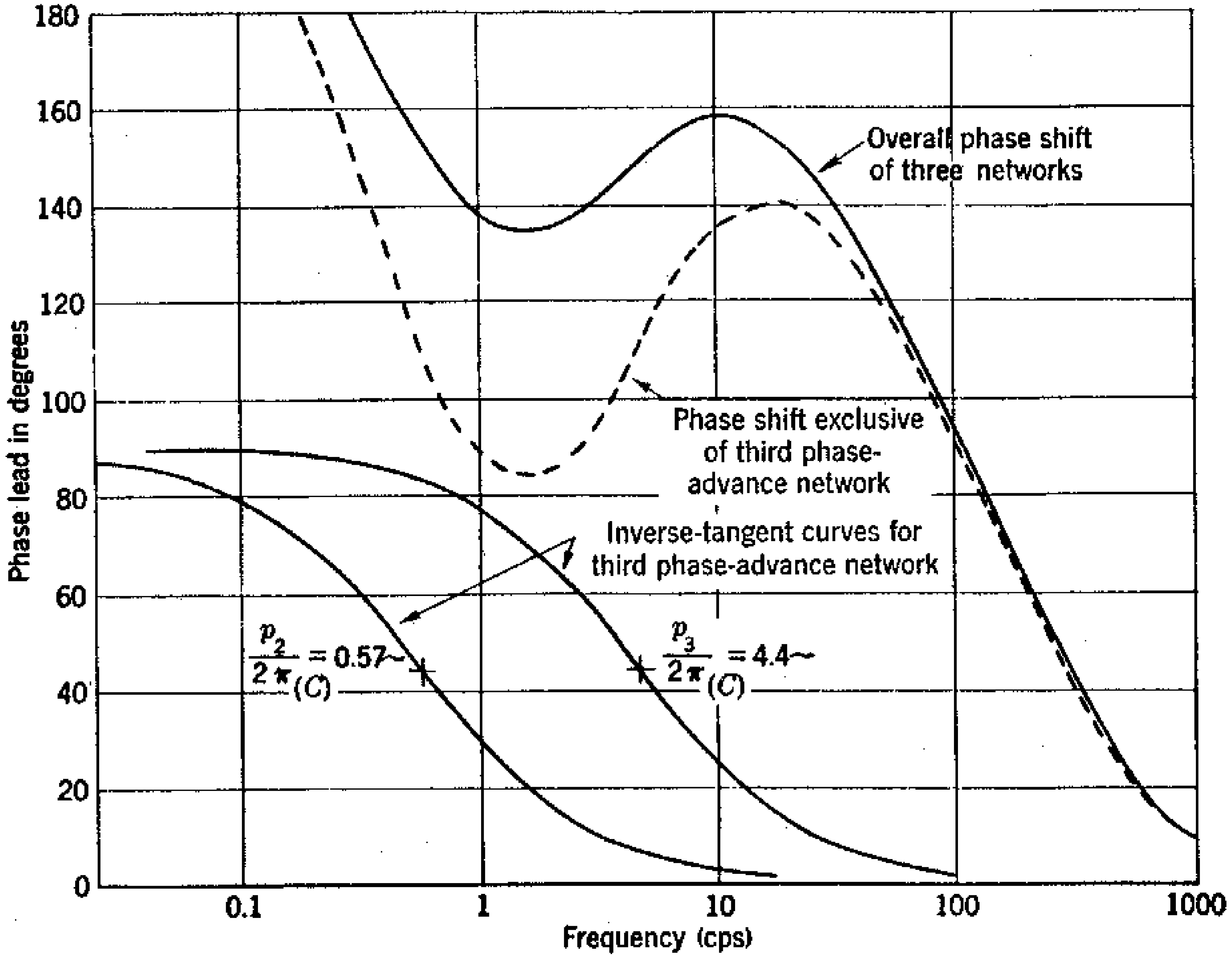

FIG. 9·32.—Calculated phase response of three low-frequency stabilization networks.

now be calculated. The reactance values in the networks at this frequency are shown in Fig. 9·33. It may be seen by inspection that the attenuation of Network *A* is about $\frac{1}{20}$; that of Network *B*, about $\frac{1}{50}$; and that of Network C, about $\frac{1}{4}$. Thus the over-all attenuation is $\frac{1}{4000}$ (72 db). This is considerably greater than the factor of 190 (46 db) required. However, the expense in parts is not much greater than if Networks *A* and *B* alone had been used (which would probably have sufficed), and the design indicates the order of gain that could be stabilized by this method.

9·14. Stabilization against High-frequency Oscillation.—At high frequency the limiting phase shifts are determined largely by tube characteristics (variational plate resistance and input capacitance). The first step in design of stabilizing networks is to find the limiting (asymptotic) phase-shift characteristic. For the first two 6C4's, the plate resistance is approximately 10 kilohms, and for the third, 25 kilohms. The presence of a series resistor between the third plate and the first grid would, of course, introduce a considerably higher output impedance than r_p, but this can be reduced, if desired, by the use of a bypass condenser. The interelectrode capacitances given[1] are $C_{gk} = 1.8$ μμf, $C_{gk} = 1.6$ μμf, and $C_{gp} = 1.3$ μμf. The input capacitance of a triode amplifier with fixed cathode potential is

$$C_{in} = C_{gk} + (1 - G_1)C_{gp} \qquad (49)$$

(cf. Sec. 9·2). Here G_1, the gain of the stage from grid to plate, is a negative quantity. The gains of the three stages as calculated in Eqs.

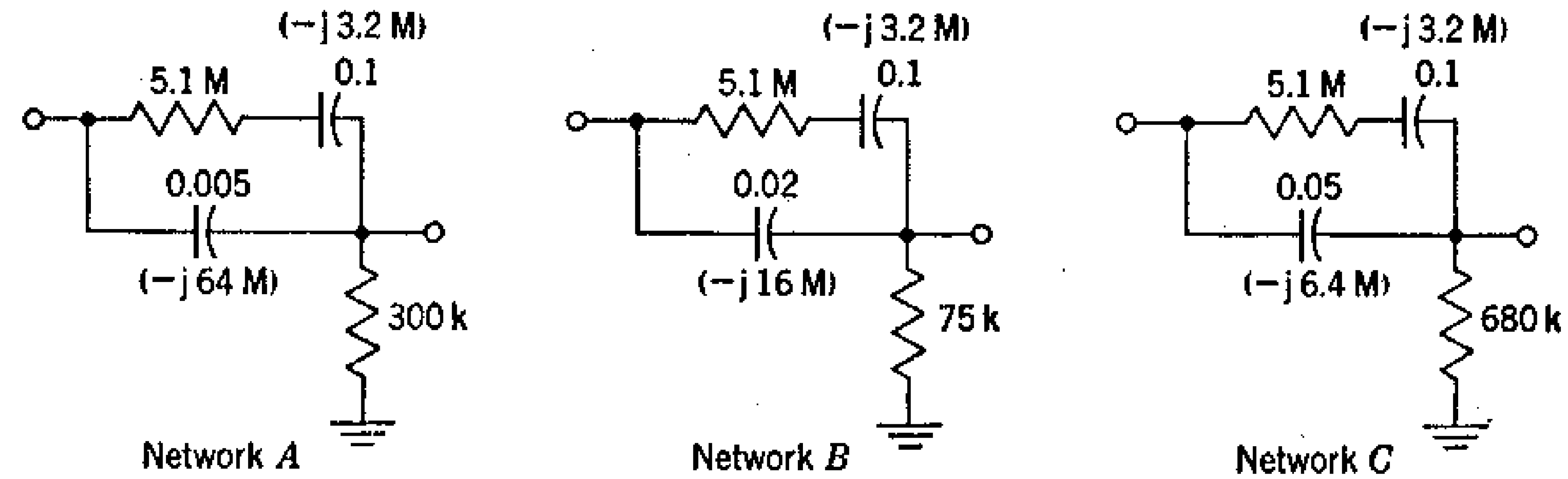

FIG. 9·33.—Low-frequency stabilization networks with reactances at 0.5 cps.

(48*a*) and (*b*) are respectively 16, 16, and 11; consequently the corresponding input capacitances are 23.7, 23.7, and 17.2 μμf. Since allowances must be made for stray wiring capacity and the effect of output capacitances of previous stages, safe figures to use are 35, 35, and 25 μμf.[2] The corresponding values of r_p are 10, 10, and 25 kilohms; however, if no condenser is put across the resistor from third plate to first grid, the effective output impedance of the third stage is 600 kilohms. The frequencies at which the phase shifts due to the first and second coupling networks are 45° are 450 and 630 kc/sec respectively. If it is assumed that these phase shifts add to give 90° at about 500 kc/sec, the question arises as to whether or not it is possible to stabilize the amplifier by attenuating with a single *RC*-network, such as the 600-kilohm resistor combined with a coupling condenser from the third to the first stage. It will be desirable to let the phase shift of the high-frequency networks at 500 cps be a lag of 23° in order to cancel the lead resulting from the low-frequency networks (Fig. 9·32). As was mentioned above, a lag of 45° would be better if the amplifier were capable of com-

[2] If pentodes had been used, these figures might have been reduced considerably.

pensating for the corresponding reduction in gain (by a factor of $1/\sqrt{2}$). If the network produces 23° phase shift at 500 cps, its central frequency (of 45° phase shift) must be 1250 cps. This will not quite suffice to attenuate by a factor of $\frac{1}{300}$ before a frequency of 500 kc/sec is reached. If two of the networks are made to attenuate rapidly, they must then have a central frequency such that 500 cps will be the logarithmic mean between it and 110 cps, the corresponding frequency for the low-frequency networks if there is to be zero phase shift at 500 cps. Thus, $500^2/110 =$ 2270 cps; and if the third network has a central frequency of 630 kc/sec, stabilization is possible[1] but with a very small safety factor.

The next alternative is to attenuate by means of a single *RC*-circuit and a single phase-retard network. If this is done, it seems desirable to start both phase-shift curves near 500 cps, as was done on the low-

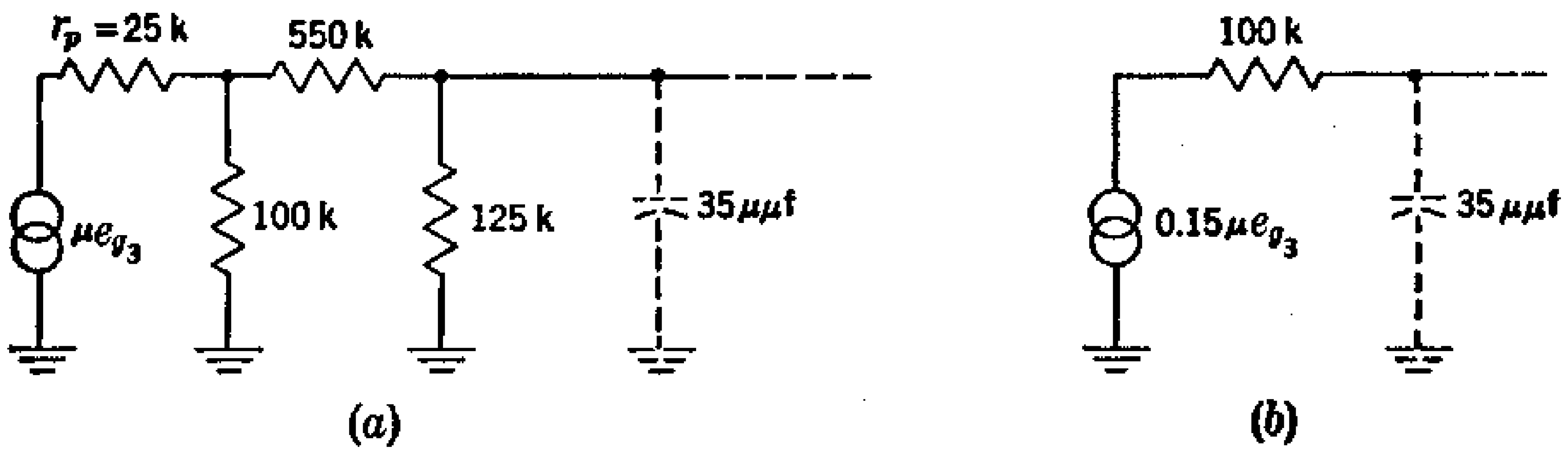

FIG. 9·34.—(*a*) High-frequency network at first grid; (*b*) Thévenin's theorem equivalent circuit.

frequency side. The network from the third plate to the first grid may be transformed by use of Thévenin's theorem, as is shown in Fig. 9·34. Its central frequency, if no additional condensers are used, is 45 kc/sec. The central frequency required for the first two inverse-tangent curves is 2270 cps, as was calculated previously. The procedure for selecting the other inverse-tangent curve in the phase-retard network will be to plot the response exclusive of this curve and then determine its position by a graphical trial-and-error process (Fig. 9·35). This process leads to the conclusion that the central frequency of the final curve should be about 50 kc/sec.

The constants of the networks may now be selected. First, a condenser will be inserted from the first grid to ground in order to produce a central frequency of 2270 cps. The value of this condenser that makes the capacitive reactance equal to the resistance (Sec. 9·3) is

$$C_3 = \frac{1}{2\pi fR} - C_s = \frac{1}{6.28 \times 1.0 \times 10^5 \times 2270} \text{ farad} - 35 \ \mu\mu f = (680 - 35) \quad \mu\mu f. \quad (50)$$

A value of 680 μμf will be used. Next, a phase-retard *RC*-network as shown in Fig. 9·36 will be introduced into the coupling circuit between the first and second stages. It has the same form as that discussed in

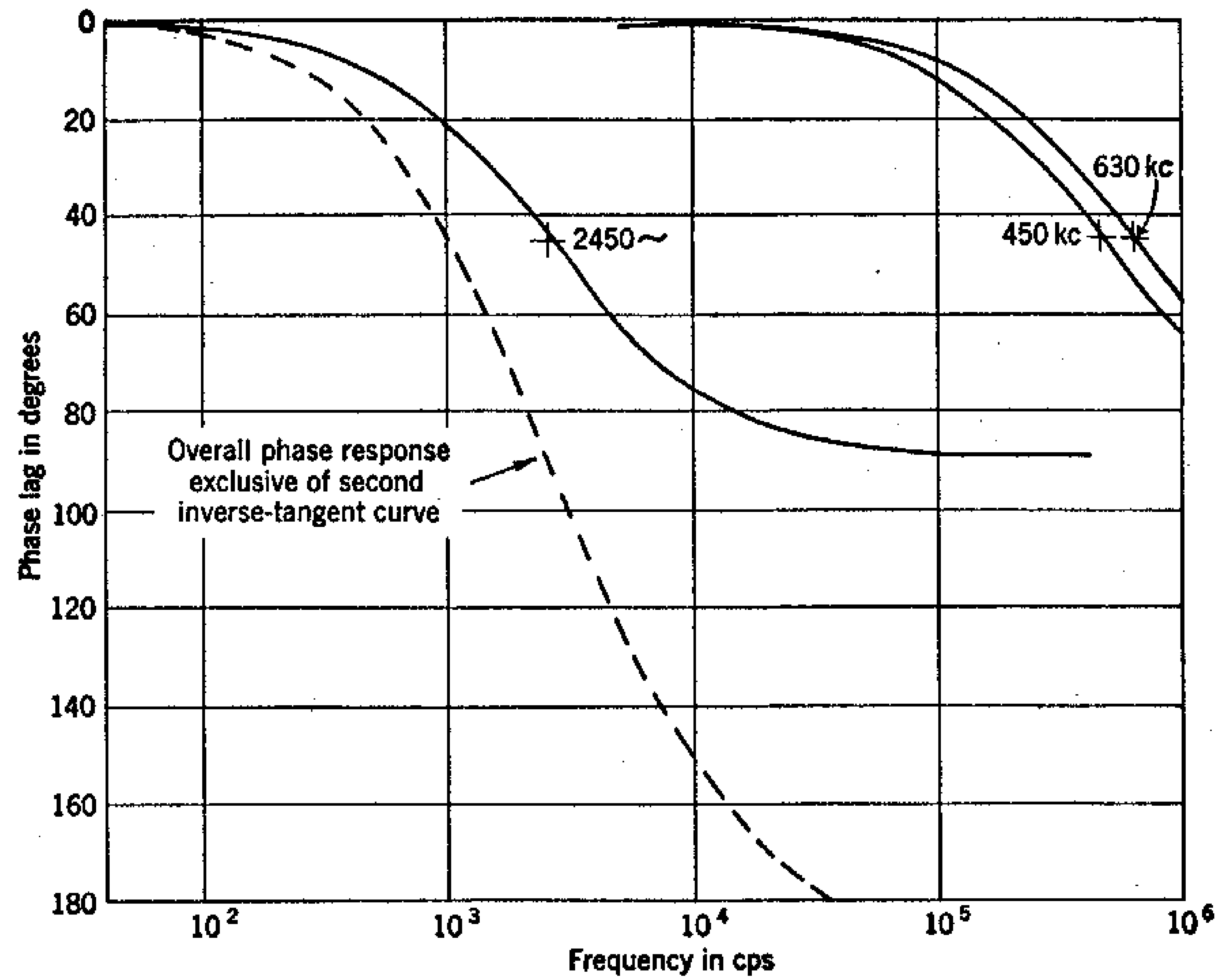

FIG. 9·35.—Calculated phase characteristics of high-frequency network.

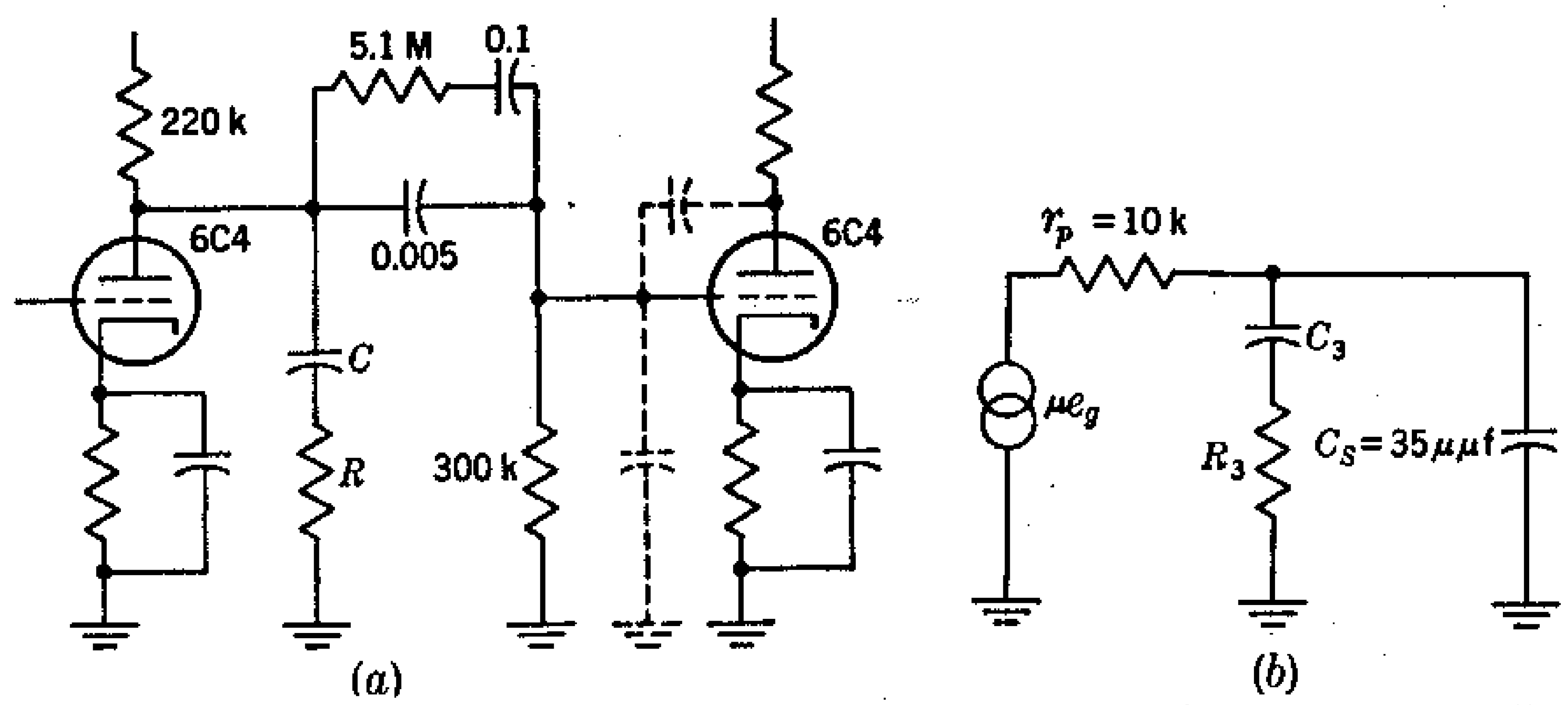

FIG. 9·36.—Coupling network between first and second stage. (*a*) Interstage coupling network; (*b*) approximate high-frequency equivalent circuit.

Sec. 9·3. The behavior of the network near 500 cps is determined largely by r_p and C_3 and is characterized by a central frequency of 2270 cps; $r_p = 10$ kilohms; therefore $C_3 = 6800$ μμf, and an approximate value of

0.006 μf is used. The other central frequency is 50 kc/sec and is determined by R_3C_s of Eq. (25). Therefore

$$R_3 = \frac{1}{6.28 \times 6 \times 10^{-9} \times 5 \times 10^4} = 540 \qquad \text{ohms.}$$

The nearest RMA value, 560 ohms, will be used. The roots p_i and the corresponding central frequencies may now be calculated, using the values r_{out} = 10 kilohms, C_s = 35 $\mu\mu$f, R_3 = 560 ohms, C_3 = 0.006 μf.

$$p_2 = -\frac{1}{R_3C_3}$$

$$p_{3,4} = -\frac{\left(\frac{1}{R_3C_3} + \frac{1}{r_{out}C_S} + \frac{1}{R_3C_S}\right)}{2} \pm \sqrt{\left(\frac{\frac{1}{R_3C_3} + \frac{1}{r_{out}C_S} + \frac{1}{R_3C_S}}{2}\right)^2 - \frac{1}{R_3r_{out}C_3C_s}}$$

Therefore

$$-p_2 = 3.02 \times 10^5 \text{ sec}^{-1} \qquad f_2 = 47 \text{ kc/sec}$$
$$-p_3 = 57 \times 10^6 \text{ sec}^{-1} \qquad f_3 = 9.1 \text{ Mc/sec}$$
$$-p_4 = 14{,}900 \text{ sec}^{-1} \qquad f_4 = 2.4 \text{ kc/sec}$$

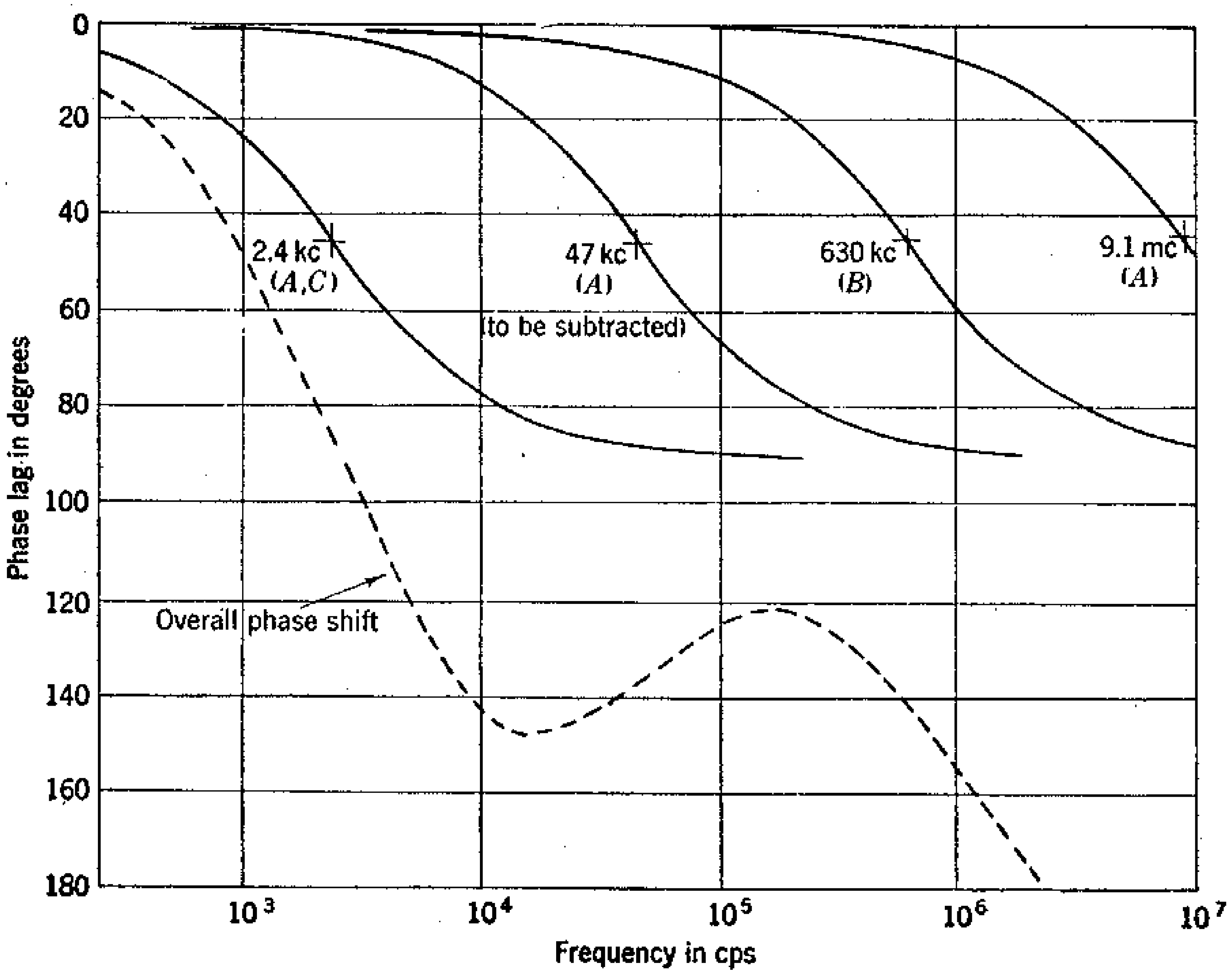

FIG. 9·37.—Over-all phase characteristic of amplifier at high frequencies (calculated).

It may be noted that the limiting high-frequency characteristic for this network has been moved from 450 kc/sec to 9.1 Mc/sec. Whereas the central frequency determined by the plate resistance of the first stage and the input capacitance of the second was 450 kc/sec, the addition of the stabilization network effectively puts a 560-ohm resistance in parallel

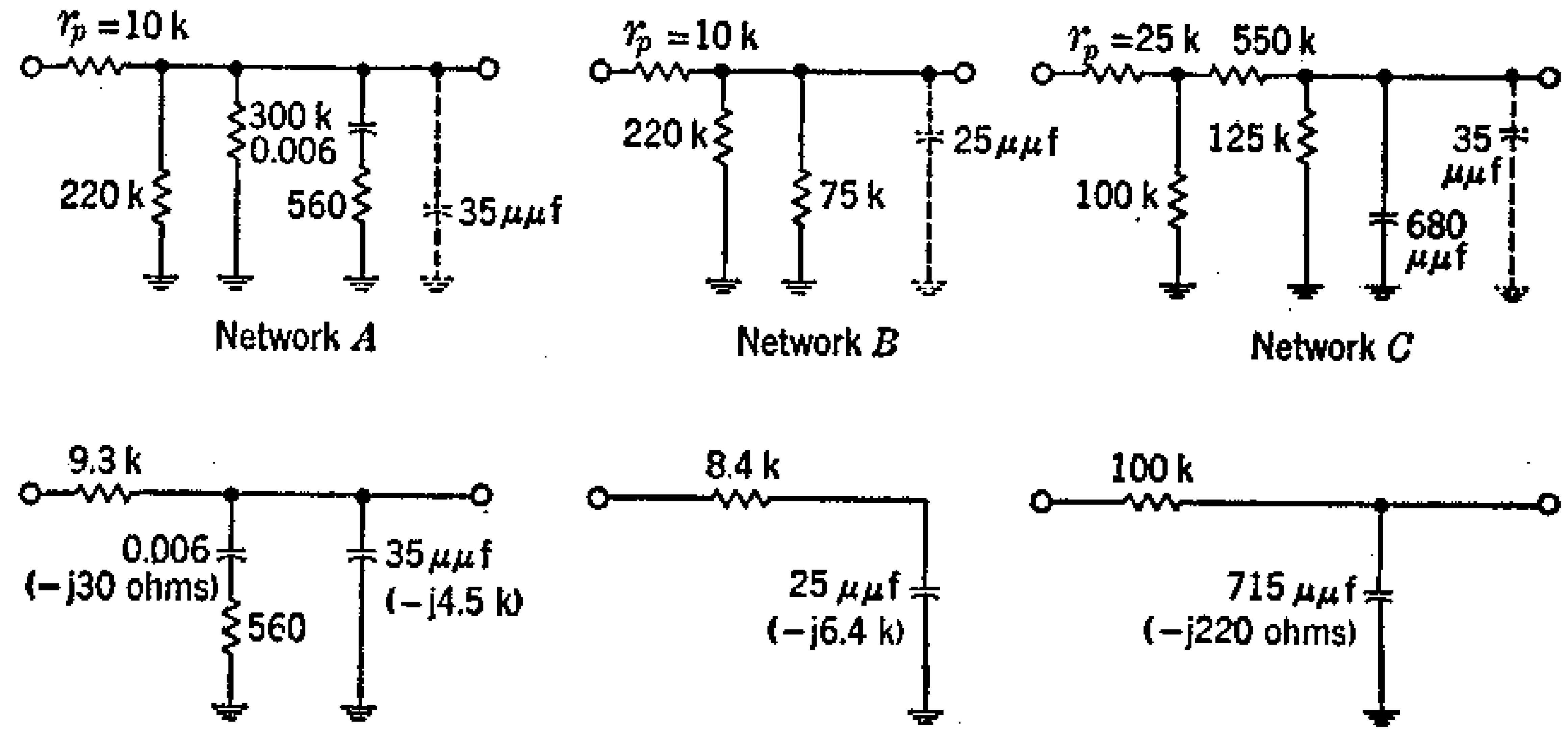

FIG. 9·38.—High-frequency stabilization networks with reactances at 1.0 Mc/sec.

with the input capacitance at high frequencies. The resulting phase response is determined not by the plate resistance of the first stage alone but by the parallel combination of this resistance and 560 ohms. This results from an effect like the one taken into account by means of Thévenin's theorem for the network at the first grid. At sufficiently high

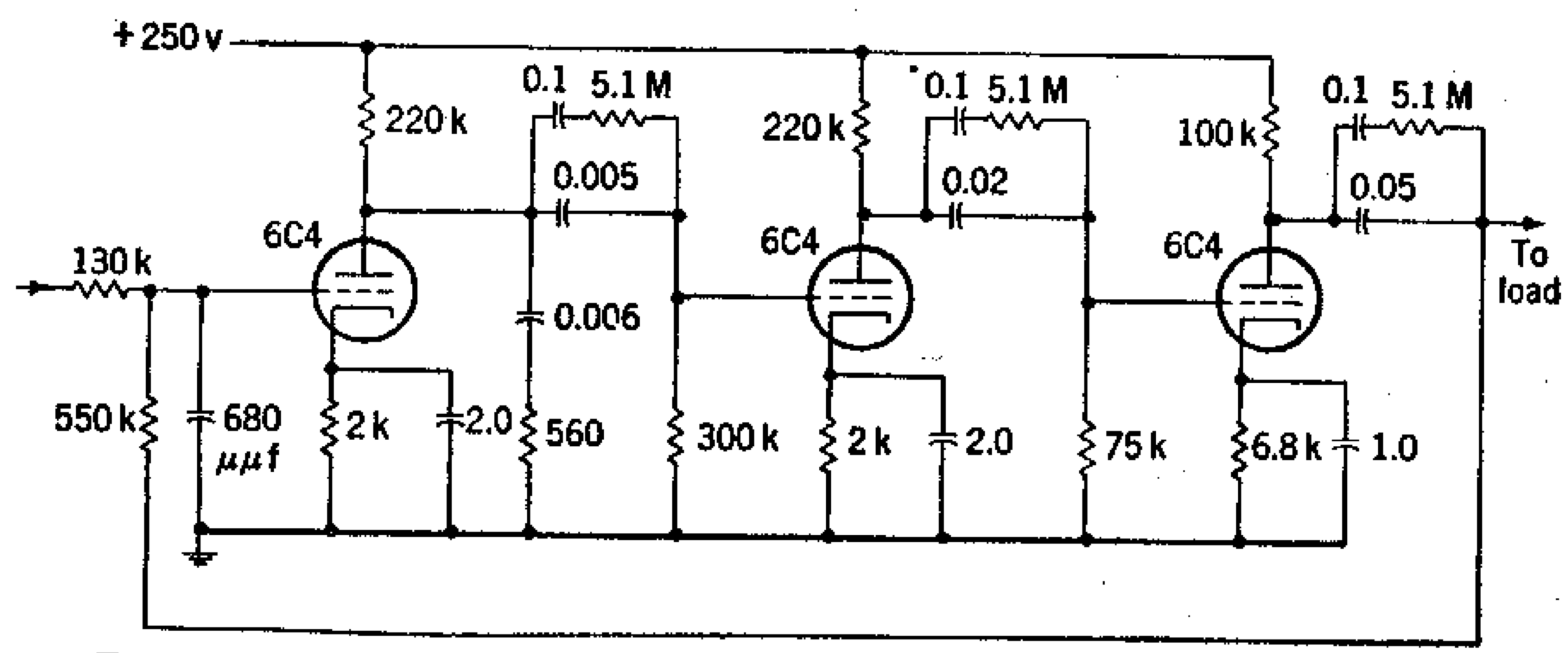

FIG. 9·39.—Design of three-stage feedback amplifier with stabilization networks.

frequencies the impedance of C_3 is small, and the resistances r_p and R_3 form a similar combination. The phase response of the high-frequency networks is plotted in Fig. 9·37. The phase shift is less than 160° up to a frequency of 1 Mc/sec. The attenuation can now be estimated as was done for the low-frequency network. The three interstage networks are shown in Fig. 9·38, with reactance values calculated at 1 Mc/sec. The plate-load and grid-leak resistances, which have been neglected so far, are included, and it will be seen that their effects are small. In the case of Network C, the output capacitance of the third triode cannot rigorously be lumped with the input capacitance of the following stage, but this fact has been ignored in getting an approximate result. The estimated values of attenuation at 1 Mc/sec are $\frac{1}{17}$, $\frac{1}{2}$, and $\frac{1}{450}$ for Networks A, B, and C, respectively. The corresponding over-all attenuation is 15,000 (84 db).

The final paper design of the amplifier is shown in Fig. 9·39.

9·15. Experimental Checks and Completion of the Design.—A test model of the circuit of Fig. 9·39 was set up. No oscillations were observed. The maximum output was about 70 volts rms before distortion was observed at the first grid. When the 5·1-megohm resistor and 0.1-μf condenser of Network A were disconnected, oscillations occurred at a frequency of 12 cps. This is about what would be predicted from Fig. 9·31 if the phase-shift curve continued up from 500 cps as would be caused by the two single RC-coupling networks alone. Disconnecting the 5.1-megohm resistor and the 0.1-μf condenser in both the second and third networks did not produce oscillations. Disconnecting the 560-ohm resistor and the 0.006-μf condenser in Network A produced oscillations at 180 kc/sec; the curves in Fig. 9·35 labeled 2.4, 450 and 630 kc/sec would add to give 180° phase shift at about 500 kc/sec. When the 680-$\mu\mu$f condenser at the first grid was disconnected, however, no oscillation occurred. These measurements show that large safety factors were allowed. They are still no assurance in themselves, however, that if the circuit were produced in quantity, Network A alone could be used for stabilization, because a combination of adverse parameter variations within the allowed tolerances might still cause oscillation.

The measured loop gain was 430, the respective stage gains being 15.5, 13.3, and 11 as against the predicted values of 16, 16, and 11 respectively. The d-c electrode voltages were roughly as predicted.

The ratio of zero-frequency to infinite-frequency gain as regards the cathode-bypass condensers was found by removing one condenser at a time and measuring gains. The respective ratios were 1.5, 1.5, and 1.8 as compared with the predicted values 1.22, 1.22, and 1.75, and the measured over-all ratio was 4.0 instead of 2.6. Some of this discrepancy is probably due to the fact that the R_g's were changed for the stabilization circuits after the calculations of gain ratios were made. This again means that the precautions taken in low-frequency stabilization were unnecessarily great, for the effective loop gain that had to be reduced by the networks was $\frac{430}{4} = 107$ rather than 190.

The loop gain and loop phase shift were measured over a limited frequency range (10 cps to 30 kc/sec) and were found to agree with the predicted values.

To complete the circuit diagram, it is necessary to include tolerances and wattages and to specify parts that may be procured. This will not be done in the present case, except to state that every condenser or resistor except the two precision resistors at the first grid could probably be assigned a tolerance of ± 20 per cent.

The design of this circuit is by no means complete for production. It should be laid out and built with the proper physical arrangement of parts, and this model should be tested for oscillation, mounting rigidity, life of tubes, etc. The problem of parasitic oscillations that arise from parameters not represented in the circuit diagram (stray wiring capacities, lead inductances) must be attacked separately. If the additional parameters can be represented as lumped constants, an analysis can be made, but the usual procedure is to insert experimentally small shunting capacitors or small series resistors in grid circuits in order to suppress such oscillations.

In designs of circuits to suppress oscillations, it is desirable to have large safety factors. This not only reduces the chance of oscillation but makes it possible to select circuit components that are manufactured to wider tolerances.

The high-frequency network in this circuit, a single phase-retard network, was more effective in reducing gain than was the low-frequency one, which involved three phase-advance networks. This is shown by the fact that over a frequency range of a factor of 2000 (500 cps to 1 Mc/sec) the high-frequency network attenuated by a factor of 15,000 whereas over a frequency factor of 1000 ($\frac{1}{2}$ to 500 cps) the low-frequency network attenuated by a factor of only 4000.

It is of interest to note that the asymptotic characteristic or limiting phase-shift curve is not a fixed limit. The use of low-frequency or high-frequency stabilization networks, as in this circuit, has the effect of pushing both asymptotes farther out (for different reasons in the two cases).