Explanation of Maximum Ratings for Thyristors

Data sheets for SCRs and triacs give vital information regarding maximum ratings and characteristics of thyristors. If the ***maximum ratings*** of the thyristors are surpassed, possible irreversible damage may occur. The characteristics describe various pertinent device parameters which are guaranteed as either minimums or maximums. Some of these characteristics relate to the ratings but are not ratings in themselves. The characteristic does not define what the circuit must provide or be restricted to but defines the device characteristic. For example, a minimum value is indicated for the dv/dt because this value depicts the guaranteed worst-case limit for all devices of the specific type. This minimum dv/dt value represents the maximum limit that the circuit should allow.

V_{RRM}: Peak Repetitive Reverse Voltage

SCR: The peak repetitive reverse voltage rating is the maximum peak reverse voltage that may be continuously applied to the main terminals (anode, cathode) of an SCR (see Figure 21.1). An open-gate condition and gate resistance termination is designated for this rating. An increased reverse leakage can result due to a positive gate bias during the reverse voltage exposure time of the SCR. The repetitive peak reverse voltage rating relates to case temperatures up to the maximum rated junction temperature.

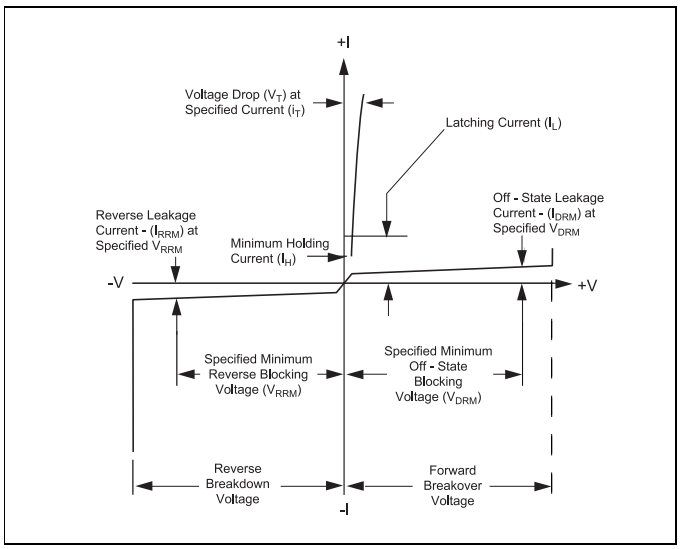

Figure 21.1 V-I Characteristics of SCR Device

V_{DRM}: Peak Repetitive Forward (Off-State) Voltage

SCR: The peak repetitive forward (off-state) voltage rating, (see Figure 1) refers to the maximum peak forward voltage which may be continuously applied to the main terminals (anode, cathode) of an SCR. This rating represents the maximum voltage the SCR should be required to block in the forward direction. The SCR may or may not go into conduction at voltages above the VDRM rating. This rating is specified for an open-gate condition and gate resistance termination. A positive gate bias should be avoided since it will reduce the forward-voltage blocking capability. The peak repetitive forward (off-state) voltage rating applies for case temperatures up to the maximum rated junction temperature.

Triac: The peak repetitive off-state voltage rating should not be surpassed on a typical, non-transient, working basis (see Figure 21.2). VDRM should not be exceeded even instantaneously. This rating applies for either positive or negative bias on main terminal 2 at the rated junction temperature. This voltage is less than the minimum breakover voltage so that breakover will not occur during operation. Leakage current is controlled at this voltage so that the temperature rise due to leakage power does not contribute significantly to the total temperature rise at rated current.

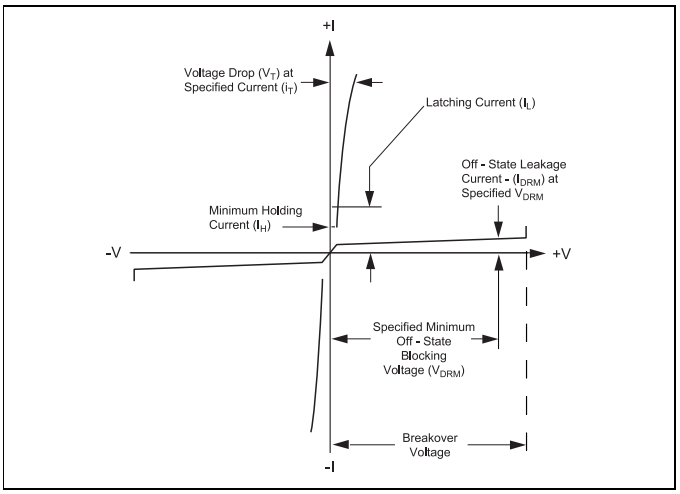

Figure 21.2

I_T Current Rating

SCR: For RMS and average currents, the restricting factor is usually confined so that the power dissipated during the on-state and as a result of the junction-to-case thermal resistance will not produce a junction temperature in excess of the maximum junction temperature rating. Power dissipation is changed to RMS and average current ratings for a 60-Hz sine wave with a 180° conduction angle. The average current for conduction angles less than 180° is derated because of the higher RMS current connected with high peak currents. The DC current rating is higher than the average value for 180° conduction since no RMS component is present.

There are several ways to determine the dissipation for non-sinusoidal waveshapes. Graphically plotting instantaneous dissipation as a function of time is one method used. The total maximum allowable power dissipation P_D may be determined using the following equation for temperature rise:

$$P_D = \frac{T_{J(MAX)} - T_C}{R_{\theta JC}}$$

where T_J(max) is the maximum rated junction temperature (at zero rated current), T_C is the actual operating case temperature, and $R_{\theta JC}$ is the published junction-to-case thermal resistance. Transient thermal resistance curves are required for short interval pulses.

Triac: The limiting factor for RMS current is determined by multiplying power dissipation by thermal resistance. The resulting current value will ensure an operating junction temperature within maximum value. For convenience, dissipation is converted to RMS current at a 360° conduction angle. The same RMS current can be used at a conduction angle of less than 360°. For information on non-sinusoidal waveshapes and a discussion of dissipation, refer to the preceding description of SCR current rating.

I_{TSM}: Peak Surge (Non-Repetitive) On-State Current

SCR and Triac: The peak surge current is the maximum peak current that may be applied to the device for one full cycle of conduction without device degradation. The maximum peak current is usually specified as sinusoidal at 50 or 60 Hz. This rating applies when the device is conducting rated current before the surge and, thus, with the junction temperature at rated values before the surge. The junction temperature will surpass the rated operating temperature during the surge, and the blocking capacity may be decreased until the device reverts to thermal equilibrium.

The surge-current curve shows the peak current that may be applied as a function of surge duration (See Figure 21.3). This surge curve is not intended to depict an exponential current decay as a function of applied overload. Instead, the peak current shown for a given number of cycles is the maximum peak surge permitted for that time period. The current must be derated so that the peak junction temperature during the surge overload does not exceed maximum rated junction temperature if blocking is to be retained after a surge.

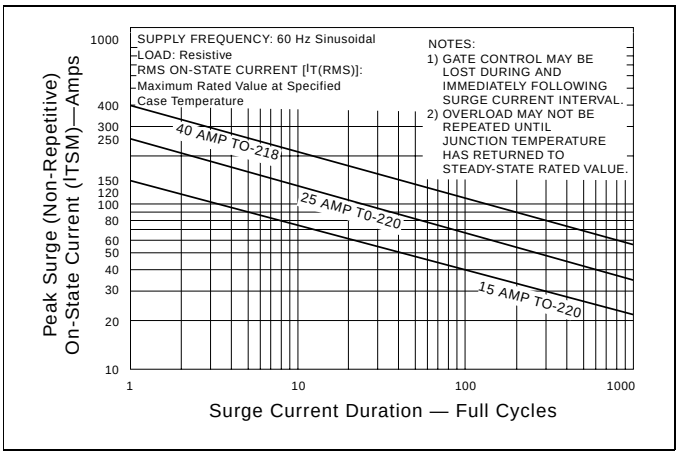

Figure 21.3 Peak Surge Current vs Surge Current Duration

I_{TM}: Peak Repetitive On-State Current

SCR and Triac: The I_{TM} rating specifies the maximum peak current that may be applied to the device during brief pulses. When the device operates under these circumstances, blocking capability is maintained. The minimum pulse duration and shape are defined and control the applied di/dt. The operating voltage, the duty factor, the case temperature, and the gate waveform are also defined. This rating must be followed when high repetitive peak currents are employed, such as in pulse modulators, capacitive-discharge circuits, and other applications where snubbers are required.

di/dt: Rate-of-Change of Forward Current

SCR and Triac: The di/dt rating specifies the maximum rate of rise of current through a thyristor device during turn-on. The value of principal voltage prior to turn-on and the magnitude and rise time of the gate trigger waveform during turn-on are among the conditions under which the rating applies. If the rate of change of current (di/dt) exceeds this maximum value, or if turn-on with high di/dt during minimum gate drive, dv/dt, or overvoltage occurs, then device degradation may occur as a result of localized heating.

During the first few microseconds of initial turn-on, the effect of di/dt is more pronounced. The di/dt capability of the thyristor is greatly increased as soon as the total area of the pellet is in full conduction.

The di/dt effects that can occur as a result of voltage or transient turn-on (non-gated) is not related to this rating. The di/dt rating is specified for maximum junction temperature.

The di/dt of a surge current can be calculated by means of the following equation (See Figure 21.4):

$$\frac{di}{dt} = \frac{\pi(I_{TM})}{t}$$

As example, surge current of 400 amperes at 60 Hz has a di/dt of π400/8.3 or 151.4 A/ms.

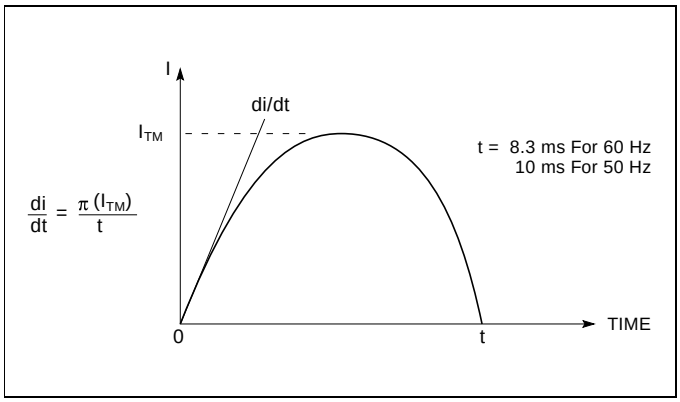

Figure 21.4 Relationship of Maximum Current Rating to Time

I^2t Rating

SCR and Triac: The I^2t rating gives an indication of the energy-absorbing capability of the thyristor device during surge-overload conditions. The rating is the product of the square of the RMS current $(I_{RMS})^2$ that flows through the device and the time during which the current is present and is expressed in A^2s. This rating is given for fuse selection purposes. It is important that the I^2t rating of the fuse is less than that of the thyristor device. Without proper fuse or current limit, overload or surge current will permanently damage the device due to excessive junction heating.

P_G: Gate Power Dissipation

SCR and Triac: Gate power dissipation ratings define both the peak power (P_{GM}) forward or reverse and the average power [$P_{G(AV)}$] that may be applied to the gate. Damage to the gate can occur if these ratings are not observed. The width of the applied

gate pulses must be considered in calculating the voltage and current allowed since the peak power allowed is a function of time. The peak power that results from a given signal source relies on the gate characteristics of the specific unit. The average power resulting from high peak powers must not exceed the average-power rating.

Temperature Range

SCR and Triac: The maximum storage temperature (T_S) is greater than the maximum operating temperature (actually maximum junction temperature). Maximum storage temperature is restricted by material limits defined not so much by the silicon but by peripheral materials such as solders used on the chip/die and lead attachments as well as the encapsulating epoxy. The forward and off-state blocking capability of the device determines the maximum junction (T_J) temperature. Maximum blocking voltage and leakage current ratings are established at elevated temperatures near maximum junction temperature; therefore, operation in excess of these limits may result in unreliable operation of the thyristor.

Characteristics

V_{BO}: Instantaneous Breakover Voltage

SCR and Triac: Breakover voltage (see Figure 1) is the voltage at which a device would turn on (switch to on-state by voltage breakover). This value applies for open-gate or gate resistance termination. Positive gate bias lowers the breakover voltage. Breakover is temperature sensitive and will occur at a higher voltage if the junction temperature is kept below maximum T_J value. If SCRs and Triacs are turned on as a result of an excess of breakover voltage, instantaneous power dissipations may be produced that can damage the chip/die.

I_{DRM}: Peak Repetitive Off-State (Blocking) Current

SCR: I_{DRM} is the maximum leakage current permitted through the SCR when the device is forward biased with rated positive voltage on the anode (DC or instantaneous) at rated junction temperature and with the gate open or gate resistance termination. A one thousand ohm resistor connected between gate and cathode is required on all sensitive SCRs. Leakage current decreases with decreasing junction temperatures. Effects of the off-state leakage currents on the load and other circuitry must be considered for each circuit application. Leakage currents can usually be ignored in applications that control high power.

Triacs: The description of peak off-state (blocking/leakage) current is the same for the triac as for the SCR except that it applies with either positive or negative bias on main terminal 2. (See Figure 21.2.)

I_{RRM}: Peak Repetitive Reverse Current

SCR: This characteristic is essentially the same as the peak forward off-state (blocking/leakage) current except negative voltage is applied to the anode (reverse biased).

V_{TM}: Peak On-State Voltage

SCR and Triac: The instantaneous on-state voltage (forward drop) is the principal voltage at a specified instantaneous current and case temperature when the thyristor is in the conducting state. To prevent heating of the junction, this characteristic is measured with a short current pulse. Note the current pulse should be at least 100 microseconds duration to ensure the device is in full conduction. The forward-drop characteristic determines the on-state dissipation (see Figure 5 and also refer to the preceding paragraph concerning current rating, I_T).

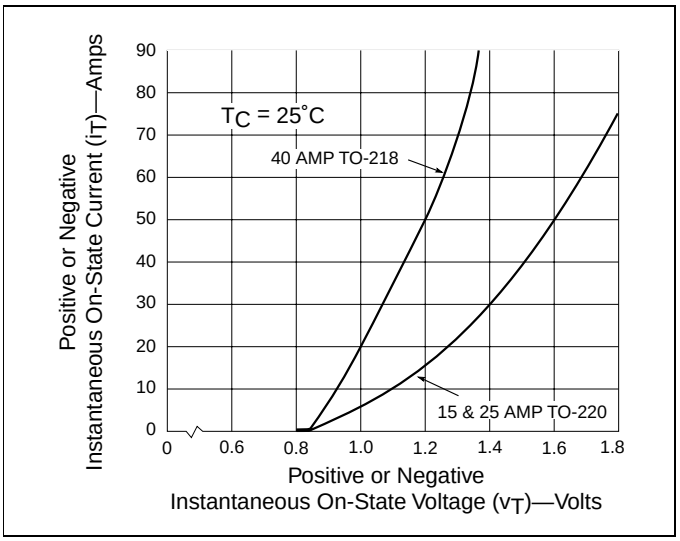

Figure 21.5 On-State Current vs On-State Voltage (Typical)

I_{GT}: DC Gate Trigger Current

SCR: I_{GT} is the minimum DC gate current required to cause the thyristor to switch from the non-conducting to the conducting state for a specified load voltage and current as well as case temperature. Figure 21.6 characteristic curve shows that trigger current is temperature dependent. The thyristor becomes less sensitive (requires more gate current) with decreasing junction temperatures. The gate current should be increased by a factor of 2 to 5 times the minimum threshold DC trigger current for best operation. Where fast turn-on is demanded and high di/dt is present or low temperatures are expected, the gate pulse may be 10 times the minimum I_{GT}, plus it must be fast rising and of sufficient duration in order to properly turn on the thyristor.

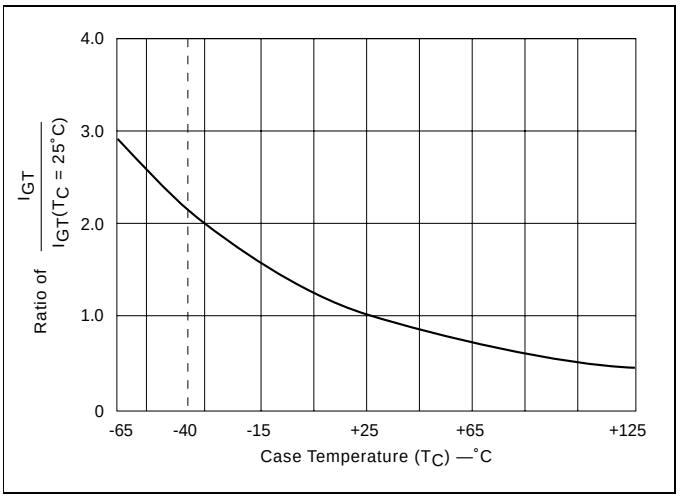

Figure 21.6 Normalized DC Gate Trigger Current for All Quadrants vs Case Temperature

Triac: The description for the SCR applies as well to the triac with the addition that the triac can be fired in four possible modes (Figure 21.7):

Quadrant I (main terminal 2 positive, gate positive)

Quadrant II (main terminal 2 positive, gate negative)

Quadrant III (main terminal 2 negative, gate negative)

Quadrant IV (main terminal 2 negative, gate positive)

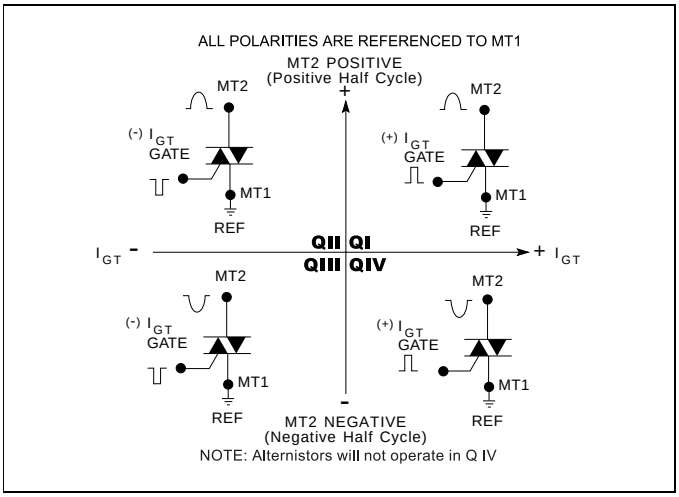

Figure 21.7 Definition of Operating Quadrants

V_{GT}: DC Gate Trigger Voltage

SCR: V_{GT} is the DC gate-cathode voltage that is present just prior to triggering when the gate current equals the DC trigger current. As shown in the characteristic curve (see Figure 21.8), the gate trigger voltage is higher at lower temperatures. The gate-cathode voltage drop can be higher than the DC trigger level if the gate is driven by a current higher than the trigger current.

Triac: The difference in V_{GT} for the SCR and the triac is that the triac can be fired in four possible modes. There can be a slight difference in the threshold trigger voltage depending which of the four operating modes is actually used.

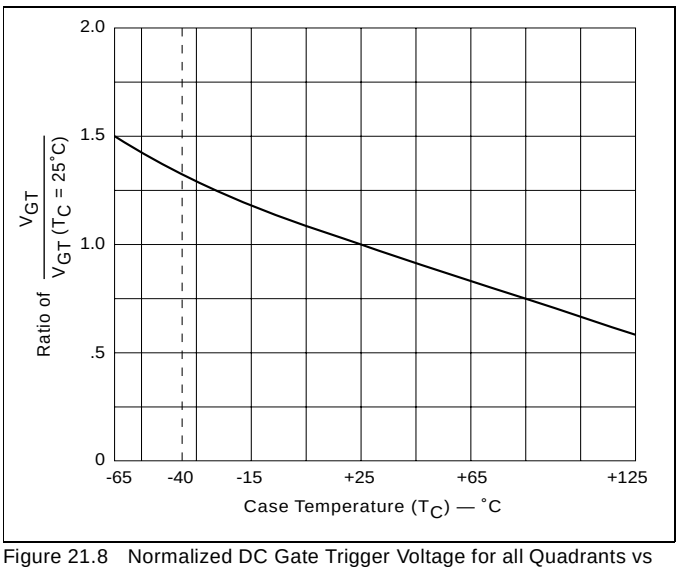

Figure 21.8 Normalized DC Gate Trigger Voltage for all Quadrants vs Case Temperature

I_L: Latching Current

SCR: Latching current is the DC anode current above which the gate signal can be withdrawn and the device will stay on. It is related to, has the same temperature dependence as, and is somewhat greater than the DC gate trigger current (see Figures 21.1 and 21.2). Latching current is at least equal to or much greater than the holding current depending on the thyristor type.

Latching current is greater for fast-rise-time anode currents since not all of the chip/die is in conduction. It is this “dynamic” latching current that determines whether a device will stay on when the gate signal is replaced with very short gate pulses. The dynamic latching current varies with the magnitude of the gate drive current and pulse duration. In some circuits, the anode current may oscillate and may drop back below the holding level or may even go negative; hence, the unit may turn off and not latch if the gate signal is removed too quickly.

Triac: The description of this characteristic is the same for the triac as for the SCR with addition that the triac can be latched on in four possible modes (quadrants). Also, the required latching is significantly different depending on which gating quadrants are used. Figure 21.9 illustrates typical latching current requirements for the four possible quadrants of operation.

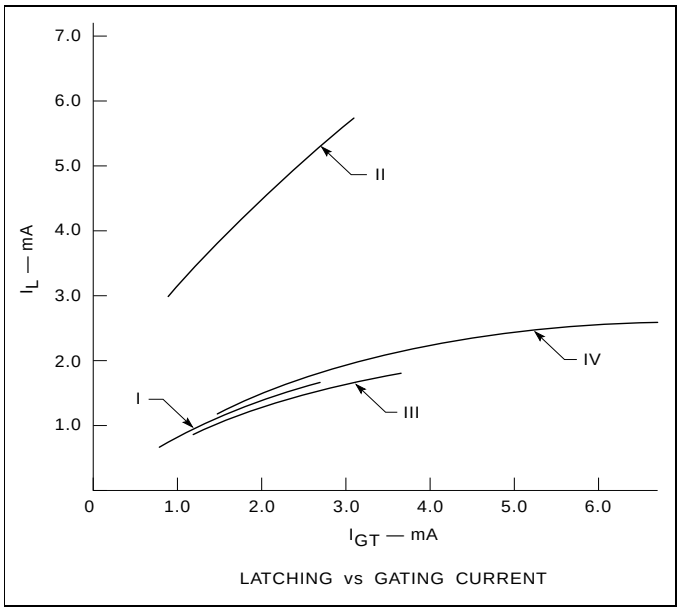

Figure 21.9 Typical Triac Latching (I_L) Requirements for Four Quadrants vs I_{GT}

I_H: Holding Current

SCR and Triac: The holding current is the DC principal on-state current below which the device will not stay in regeneration/on-state after latching and gate signal is removed. This current is equal to or lower in value than the latching current (see Figures 21.1 and 21.2) and is related to and has the same temperature dependence as the DC gate trigger current (see Figure 21.10). Both minimum and maximum holding current may be important. If the device is to stay in conduction at low anode currents, the maximum holding current of a device for a given circuit must be considered. The minimum holding current of a device must be considered if the device is expected to turn off at a low DC anode current. Note that the low DC principal current condition is a DC turn-off mode, and that an initial on-state current (latching cur-

rent) is required to ensure that the thyristor has been fully turned on prior to a holding current measurement.

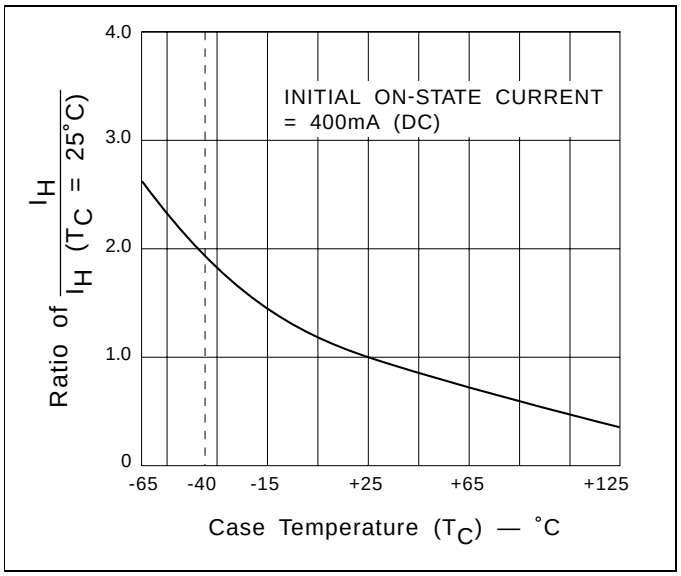

Figure 21.10 Normalized DC Holding Current vs Case Temperature

dv/dt, Static: Critical Rate-of-Rise of Off-State Voltage

SCR and Triac: Static dv/dt (see Figure 21.11 for exponential definition) is the minimum rate-of-rise of off-state voltage that a device will hold-off, with gate open, without turning on. This value will be reduced by a positive gate signal. This characteristic is temperature dependent and is lowest at the maximum-rated junction temperature. Therefore, the characteristic is determined at rated junction temperature and at rated forward off-state voltage which is also a worst-case situation. Line or other transients which might be applied to the thyristor in the off state must be reduced, so that neither the rate-of-rise nor the peak voltage are above specifications if false firing is to be prevented. Turn on as result of dv/dt is non-destructive as long as the follow current remains within current ratings of device being used.

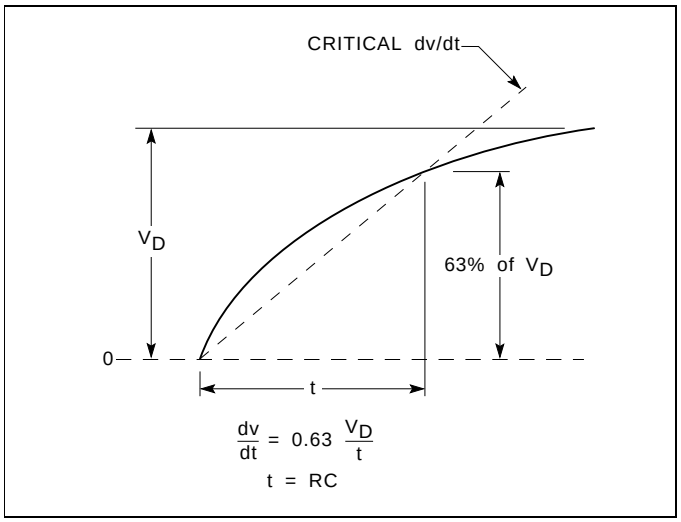

Figure 21.11 Exponential Rate-of-Rise of Off-State Voltage Defining dv/dt

dv/dt, Commutating: Critical Rate-of-Rise of Commutation Voltage

Triac: Commutating dv/dt is the rate-of-rise of voltage across the main terminals that a triac can support (block without switching back on) when commutating from the on-state in one half-cycle to the off-state in the opposite half-cycle. This parameter is specified at maximum rated case (equaled to T_J) temperature since it is temperature dependent. It is also dependent on current (commutating di/dt) and peak reapplied voltage (line voltage) and is specified at rated current and voltage. All devices are guaranteed to commutate rated current with a resistive load at 50 to 60 Hz. Commutation of rated current is not guaranteed at higher frequencies, and no direct relationship can be made with regard to current/temperature derating for higher-frequency operation. With inductive loading, when the voltage is out of phase with the load current, there will be a voltage stress (dv/dt) across the main terminals of the triac during the zero-current crossing (see Figure 21.12). A snubber (series RC across the triac) should be used with inductive loads to decrease the applied dv/dt to an amount below the minimum value which the triac can be guaranteed to commutate off each half-cycle.

Commutating dv/dt is specified for a half sinewave current at 60 Hz which fixes the di/dt of the commutating current. The commutating di/dt for 50 Hz is approximately 20 percent lower and for the same I_{RMS} (see Figure 21.4).

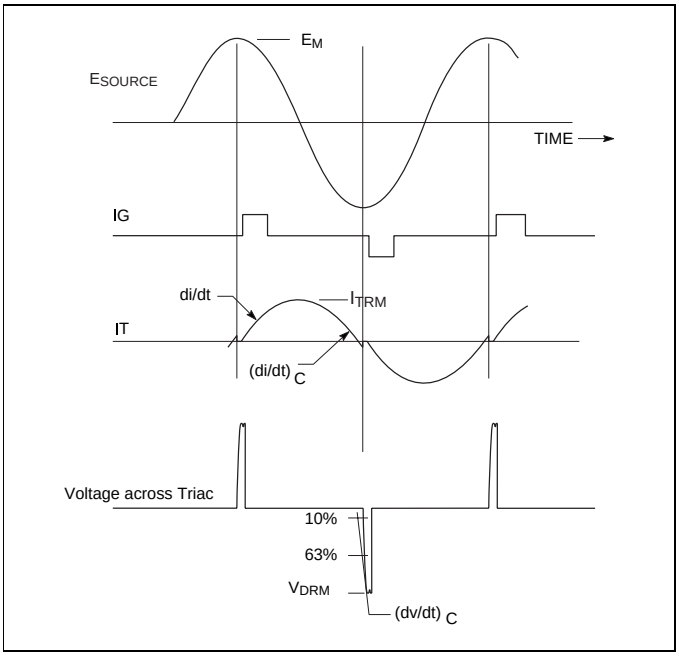

Figure 21.12 Waveshapes of Commutating dv/dt and Associated Conditions

t_{gt}: Gate Controlled Turn-On Time

SCR and Triac: The t_{gt} is the time interval between the application of a gate pulse and the on-state current reaching 90 percent of its steady-state value (see Figure 21.13). Turn-on time is a function of gate drive as would be expected. Shorter turn-on times occur for increased gate drives. This turn-on time is actually only valid for resistive loading. For example, inductive loading would restrict the rate-of-rise of anode current. For this reason, this parameter does not indicate the time which must be allowed for the device to stay on if the gate signal is removed (refer to the description of latching current I_L). However, if the

load were resistive and equal to the rated load current value, the device definitely would be operating at a current above the dynamic latching current in the turn-on time interval since current through the device is at 90 percent of its peak value during this interval.

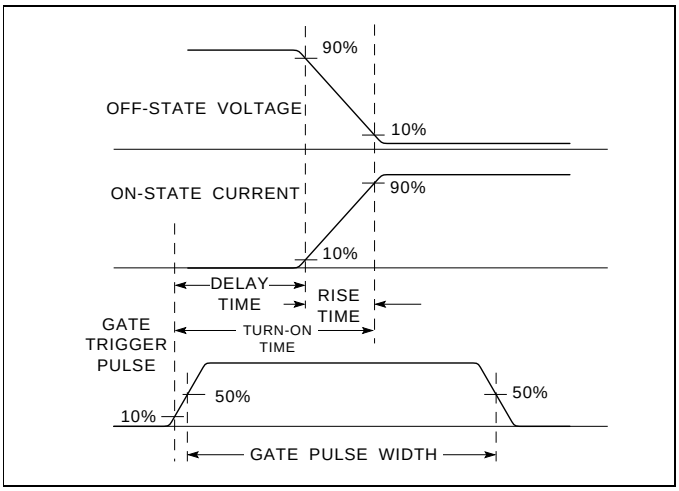

Figure 21.13 Waveshapes for Turn-On Time and Associated Conditions

t_q: Circuit - Commutated Turn-Off Time

SCR: The circuit-commutated turn-off time of the device is the time during which the circuit provides reverse bias to the device (negative anode) to commutate it off. The turn-off time occurs between the time when the anode current goes negative and when the anode positive voltage may be reapplied (see Figure 21.14). Turn-off time is a function of many parameters and is very dependent on temperature and gate bias during the turn-off interval. Turn-off time is lengthened for higher temperature so a high junction temperature is specified. The gate is open during the turn-off interval. Positive bias on the gate will lengthen the turn-off time; negative bias on the gate will shorten it.

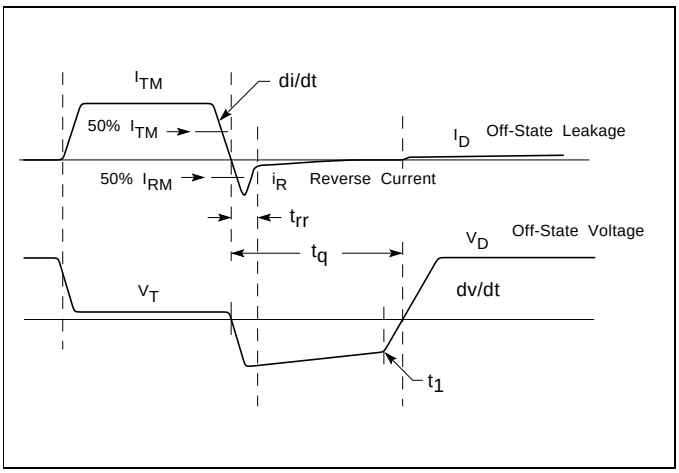

Figure 21.14 Waveshapes of t_q Rating Test and Associated Conditions

$R_{\theta JC}$, $R_{\theta JA}$: Thermal Resistance (Junction-to-Case, Junction-to-Ambient)

SCR and Triac: The thermal-resistance characteristic defines the steady-state temperature difference between two points at a given rate of heat-energy transfer (dissipation) between the points. The thermal-resistance system is an analog to an electrical circuit where thermal resistance is equivalent to electrical resistance, temperature difference is equivalent to voltage difference, and rate of heat-energy transfer (dissipation) is equivalent to current. Dissipation is represented by a constant current generator since heat generated must flow (steady-state) no matter what the resistance in its path. Junction-to-case thermal resistance establishes the maximum case temperature at maximum rated steady-state current. The case temperature must be held to the maximum at maximum ambient temperature when the device is operating at rated current. Junction-to-ambient thermal resistance is established at a lower steady-state current where the device is in free air with no external heatsinking except what the device package offers in itself. For $R_{\theta JA}$, power dissipation is limited by what the device package can dissipate in free air without any additional heatsink.