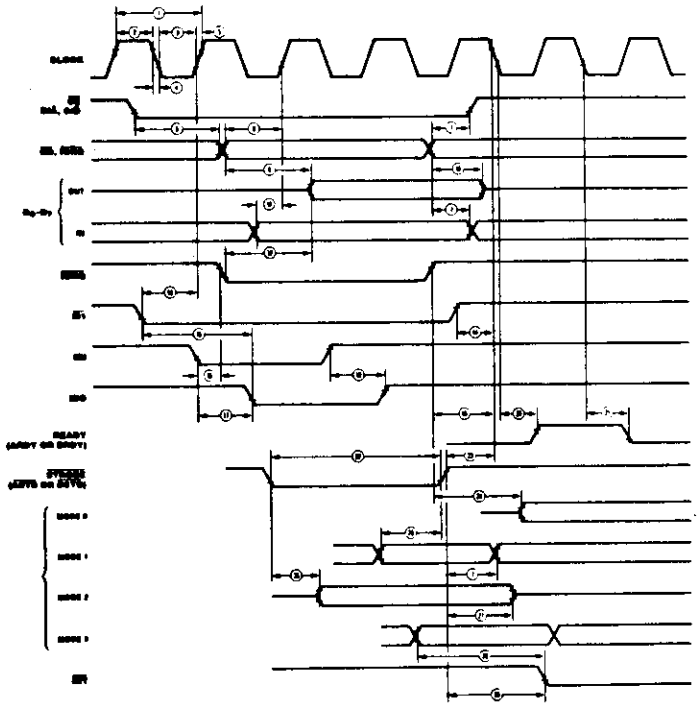
# Zilog

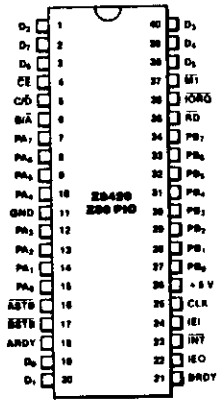
Z08420 Customer
Procurement Spec (CPS)

**GENERAL DESCRIPTION**

The Z80 PIO Parallel I/O Circuit is a programmable, dual port device that provides a TTL-compatible interface between peripheral devices and the Z80 CPU (Figures 1 and 2). The CPU configures the Z80 PIO to interface with a wide range of peripheral devices with no other external logic. Typical peripheral devices that are compatible with the Z80 PIO include most keyboards, paper tape readers and punches, printers, and PROM programmers.

**AC TIMING DIAGRAM**






**40-pin Dual-In-Line Package (DIP), Pin Assignments**



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## AC CHARACTERISTICS†

| | Number | Symbol | Parameter | Z80 PIO* Min | Z80 PIO* Max | Z80-A PIO* Min | Z80-A PIO* Max | Z80-B PIO* Min | Z80-B PIO* Max | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| a | 1 | TcC | Clock Cycle Time | 400 | [1] | 250 | [1] | 165 | [1] | |
| a | 2 | TwCh | Clock Width (High) | 170 | 2000 | 105 | 2000 | 65 | 2000 | |
| a | 3 | TwCl | Clock Width (Low) | 170 | 2000 | 105 | 2000 | 65 | 2000 | |
| a | 4 | TfC | Clock Fall Time | | 30 | | 30 | | 20 | |
| a | 5 | TrC | Clock Rise Time | | 30 | | 30 | | 20 | |
| a | 6 | TsCS(RI) | $\overline{CE}$, B/$\overline{A}$, C/$\overline{D}$ to $\overline{RD}$, $\overline{IORQ}$ ↓ Setup Time | 50 | | 50 | | 50 | | [6] |
| a | 7 | Th | Any Hold Times for Specified Setup Time† | 0 | | 0 | | 0 | 0 | |
| a | 8 | TsRI(C) | $\overline{RD}$, $\overline{IORQ}$ to Clock ↑ Setup Time | 110 | | 115 | | 70 | | |
| a | 9 | TdRI(DO) | $\overline{RD}$, $\overline{IORQ}$ ↓ to Data Out Delay | | 430 | | 380 | | 300 | [2] |
| a | 10 | TdRI(DOs) | $\overline{RD}$, $\overline{IORQ}$ ↑ to Data Out Float Delay | | 160 | | 110 | | 70 | |
| a | 11 | TsDI(C) | Data In to Clock ↑ Setup Time | 50 | | 50 | | 40 | | CL = 50 pf |
| a | 12 | TdIO(DOI) | $\overline{IORQ}$ ↓ to Data Out Delay (INTACK Cycle) | | 340 | | 160 | | 120 | [3] |
| a | 13 | TsM1(Cr) | $\overline{M1}$ ↓ to Clock ↑ Setup Time | 210 | | 90 | | 70 | | |
| a | 14 | TsM1(Cf) | $\overline{M1}$ ↑ to Clock ↓ Setup Time ($\overline{M1}$ Cycle) | 0 | | 0 | | 0 | | [8] |
| a | 15 | TdM1(IEO) | $\overline{M1}$ ↓ to IEO ↓ Delay (Interrupt Immediately Preceding $\overline{M1}$ ↓) | | 300 | | 190 | | 100 | [5,7] |
| a | 16 | TsIEI(IO) | IEI to $\overline{IORQ}$ ↓ Setup Time (INTACK Cycle) | 140 | | 140 | | 100 | | [7] |
| a | 17 | TdIEI(IEO) | IEI ↓ to IEO ↓ Delay | | 190 | | 130 | | 120 | [5] CL = 50 pf |
| a | 18 | TdIEI(IEOr) | IEI ↑ to IEO ↑ Delay (after ED Decode) | | 210 | | 160 | | 150 | [5] |
| a | 19 | TcIO(C) | $\overline{IORQ}$ ↑ to Clock ↓ Setup Time (To Activate READY on Next Clock Cycle) | 220 | | 200 | | 170 | | |
| a | 20 | TdC(RDYr) | Clock ↓ to READY ↑ Delay | | 200 | | 180 | | 170 | [5] CL = 50 pf |
| a | 21 | TdC(RDYf) | Clock ↓ to READY ↓ Delay | | 180 | | 140 | | 120 | [5] |
| a | 22 | TwSTB | $\overline{STROBE}$ Pulse Width | 150 | | 150 | | 120 | | [4] |
| a | 23 | TsSTB(C) | $\overline{STROBE}$ ↑ to Clock ↓ Setup Time (To Activate READY on Next Clock Cycle) | 220 | | 220 | | 150 | | [5] |
| a | 24 | TdIO(PD) | $\overline{IORQ}$ ↑ to PORT DATA Stable Delay (Mode 0) | | 200 | | 180 | | 160 | [5] |
| a | 25 | TsPD(STB) | PORT DATA to $\overline{STROBE}$ ↑ Setup Time (Mode 1) | 280 | | 230 | | 190 | | |
| a | 26 | TdSTB(PD) | $\overline{STROBE}$ ↓ to PORT DATA Stable (Mode 2) | | 230 | | 210 | | 190 | [5] |
| a | 27 | TdSTB(PDr) | $\overline{STROBE}$ ↑ to PORT DATA Float Delay (Mode 2) | | 200 | | 180 | | 160 | CL = 50 pf |
| a | 28 | TdPO(INT) | PORT DATA Match to $\overline{INT}$ ↓ Delay (Mode 3) | | 540 | | 480 | | 430 | |
| a | 29 | TdSTB(INT) | $\overline{STROBE}$ ↑ to $\overline{INT}$ ↓ Delay | | 480 | | 440 | | 350 | |

NOTES:
[1] TcC = TwCh + TwCl + TrC + TfC
[2] Increase TdRI(DO) by 10 ns for each 50 pf increase in load up to 300 pf max
[3] Increase TdIO(DOI) by 10 ns for each 50 pf increase in loading up to 300 pf max
[4] For Mode 2 TwSTB > TsPD(STB)
*Clock-cycle time-dependent characteristics. See Footnotes to AC Characteristics.
• Timings are preliminary and subject to change. Units in nanoseconds.
a Tested
b Guaranteed by Design
c Guaranteed by Characterization
[5] Increase these values by 2 ns for each 10 pf increase in loading up to 100 pf max
[6] TsCS(RI) may be reduced. However the time subtracted from TsCS(RI) will be added to TdRI(DO)
[8] $\overline{M1}$ must be active for a minimum of two clock cycles to reset the PIO
† Units in nanoseconds (ns).

## DC CHARACTERISTICS

| Symbol | Parameter | Min | Max | Unit | Test Condition |
|---|---|---|---|---|---|
| $V_{ILC}$ | Clock Input Low Voltage | −0.3 | +0.45 | V | |
| $V_{IHC}$ | Clock Input High Voltage | $V_{CC}$ −0.6 | $V_{CC}$ +0.3 | V | |
| $V_{IL}$ | Input Low Voltage | −0.3 | +0.8 | V | |
| $V_{IH}$ | Input High Voltage | +2.0 | $V_{CC}$ | V | |
| $V_{OL}$ | Output Low Voltage | | +0.4 | V | $I_{OL}$ = 2.0 mA |
| $V_{OH}$ | Output High Voltage | +2.4 | | V | $I_{OH}$ = −250 μA |
| $I_{LI}$ | Input Leakage Current | | ±10 | μA | $V_{IN}$ = 0 to $V_{CC}$ |
| $I_{LO}$ | 3 State Output Leakage Current in Float | | ±10 | μA | $V_{OUT}$ = 0.4V to $V_{CC}$ |
| $I_{CC}$ | Power Supply Current | | 100 | mA | |
| $I_{OHD}$ | Darlington Drive Current Port B Only | −1.5 | | mA | $V_{OH}$ = 1.5V $R_{EXT}$ = 390 Ω |

Over specified temperature and voltage range