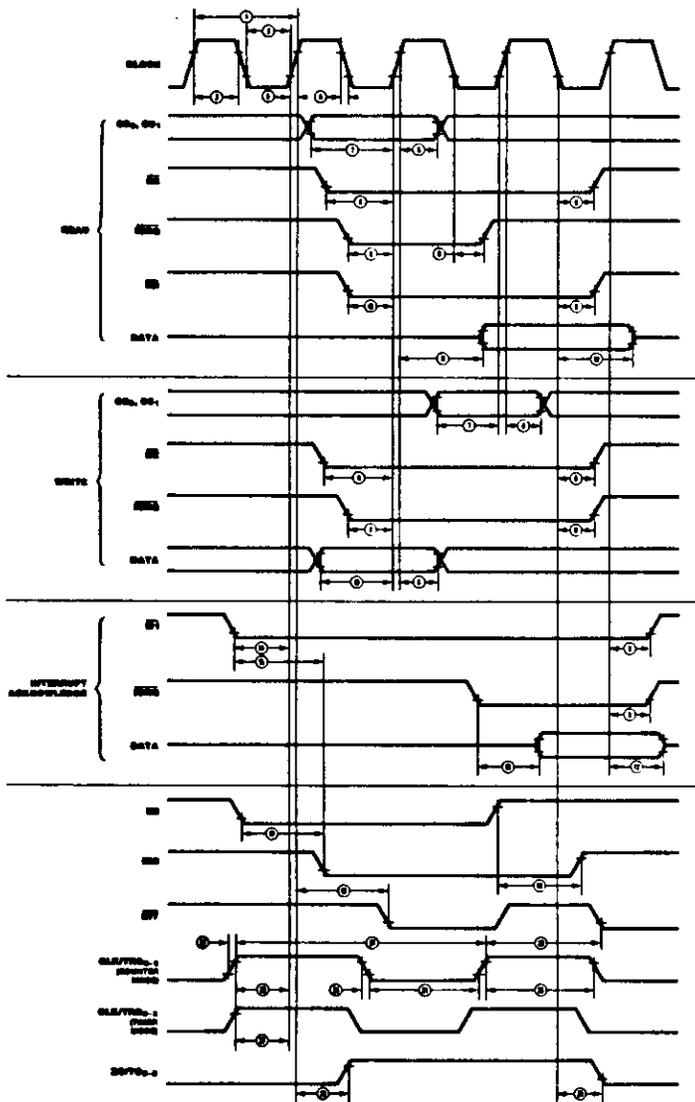


Zilog

Z08430 Customer Procurement Spec (CPS)



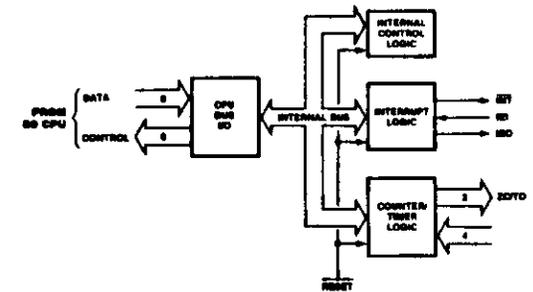
GENERAL DESCRIPTION

The Z80 CTC four-channel counter/timer can be programmed by system software for a broad range of counting and timing applications. The four independently programmable channels of the Z80 CTC satisfy common microcomputer system requirements for event counting, interrupt and interval timing, and general clock rate generation.

System design is simplified because the CTC connects directly to both the Z80 CPU and the Z80 SIO with no additional logic. In larger systems, address decoders and buffers may be required.

Programming the CTC is straightforward: each channel is programmed with two bytes, a third is necessary when interrupts are enabled. Once started, the CTC counts down, automatically reloads its time constant, and resumes counting. Software timing loops are completely eliminated. Interrupt processing is simplified because only one vector need be specified; the CTC internally generates a unique vector for each channel.

The Z80 CTC requires a single +5V power supply and the standard Z80 single-phase system clock. It is fabricated with n-channel silicon-gate depletion-load technology, and packaged in a 28-pin and a 44-pin chip carrier DIP.



Functional Block Diagram

Z80 is a registered trademark of Zilog, Inc.

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Telephone (408)370-8000 TWX 910-338-7621

AC CHARACTERISTICS

Parameter	2900 CTC		290A CTC		290B CTC	
	Min	Max	Min	Max	Min	Max

1	TC	Clock Cycle Time	400	(1)	250	(1)
2	hCh	Clock Width (High)	170	2000	100	2000
3	hCl	Clock Width (Low)	170	2000	100	2000
4	tTC	Clock Fall Time	20		30	
5	tC	Clock Rise Time	20		30	

6	tH	All Hold Times	0		0	
7	t(CS)	CS to Clock Setup Time	250	150	100	100
8	t(CE)	CE to Clock Setup Time	200	150	100	100
9	t(WR)	RD to Clock Setup Time	250	115	70	70
10	t(WR)	RD to Clock Setup Time	240	115	70	70

11	t(DQ)	Clock to Data Out Delay	240	200	130	130
12	t(DQ)	Clock to Data Out Float Delay				
13	t(DQ)	Data in to Clock Setup Time	80	50	40	40
14	t(MT)	MT to Clock Setup Time	210	80	70	70
15	t(MT)	MT to RD + Delay (predecoding M1)				

16	t(WD)	RD to Data Out Delay (M1 Cycle)	340	180	110	110
17	t(WR)	RD to RD + Delay (M1 Cycle)	180	130	100	100
18	t(WR)	RD to RD + Delay (M1 Cycle)	180	130	100	100
19	t(WR)	RD to RD + Delay (M1 Cycle)	220	180	110	110
20	t(WR)	RD to RD + Delay (M1 Cycle)	(1) + (26)	(1) + (26)	(1) + (26)	(1) + (26)

21	t(CR)	CLK/TKG Cycle Time	270C	270C	270C	270C
22	t(CR)	CLK/TKG Rise Time	50	50	50	50
23	t(CR)	CLK/TKG Fall Time	50	50	50	50
24	t(CR)	CLK/TKG Width (Low)	200	200	200	200
25	t(CR)	CLK/TKG Width (High)	200	200	200	200

26	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
27	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
28	t(CR)	Clock to ZC/TD + Delay	210	260	210	210
29	t(CR)	Clock to ZC/TD + Delay	180	180	180	180
30	t(CR)	Clock to ZC/TD + Delay	140	140	140	140

31	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
32	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
33	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
34	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
35	t(CR)	CLK/TKG to Clock Setup	300	210	180	180

36	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
37	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
38	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
39	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
40	t(CR)	CLK/TKG to Clock Setup	300	210	180	180

41	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
42	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
43	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
44	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
45	t(CR)	CLK/TKG to Clock Setup	300	210	180	180

46	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
47	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
48	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
49	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
50	t(CR)	CLK/TKG to Clock Setup	300	210	180	180

51	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
52	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
53	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
54	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
55	t(CR)	CLK/TKG to Clock Setup	300	210	180	180

56	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
57	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
58	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
59	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
60	t(CR)	CLK/TKG to Clock Setup	300	210	180	180

61	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
62	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
63	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
64	t(CR)	CLK/TKG to Clock Setup	300	210	180	180
65	t(CR)	CLK/TKG to Clock Setup	300	210	180	180

NOTES:
 (1) t(CR) = hCh + hCl + tC
 (2) Increase delay by 10 ns for each 50 pF increase in loading, 200 pF maximum for data lines and 100 pF for control lines.
 (3) Increase delay by 2 ns for each 10 pF increase in loading, 100 pF maximum.
 (4) Transfer mode.
 (5) Control mode.
 (6) Parameter numbers reference the same number of a parameter.
 (7) Parameter numbers in parentheses are for a parameter of a parameter.
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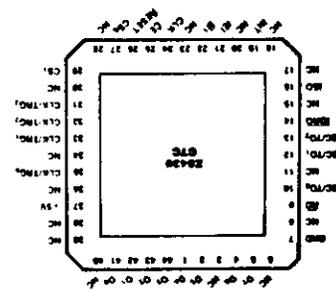
DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Condition
V _{IC}	Check Input High Voltage	-0.3V	+0.45V	V	
V _{IC}	Check Input Low Voltage	0.3V	V _{CC} - 0.3V	V	
V _{IN}	Input High Voltage	-0.3V	V _{CC} + 0.3V	V	
V _{IN}	Input Low Voltage	0.3V	V _{CC} - 0.3V	V	
V _{OL}	Output High Voltage	V _{CC} - 0.3V	V _{CC}	V	
V _{OL}	Output Low Voltage	0.3V	0.4V	V	
V _{OH}	Output High Voltage	0.4V	V _{CC}	V	
V _{OH}	Output Low Voltage	0.3V	0.4V	V	
I _{CC}	Power Supply Current	+120 μ A		mA	V _{IN} = 0.4 to V _{CC} V _{OH} = 1.5V
I _{IO}	Input Leakage Current	±10 μ A		mA	V _{IN} = 0.4 to V _{CC} V _{OH} = 1.5V
I _{IO}	Output Leakage Current in Float	±10 μ A		mA	V _{OH} = 1.5V
I _{DM}	Demagnetization Drive Current	-1.5A		A	I _{OH} = 20 mA

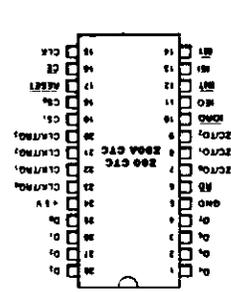
Not tested
 Guaranteed by Design

Not tested
 Guaranteed by Design

44-pin Quad-Line Package (DIP)



40-pin Dual-In-Line Package (DIP)



AC Characteristics:
 - Timing are preliminary and subject to change. Write in memorandum.
 - Tested
 - Guaranteed by Design
 - Guaranteed by Characterization

DC Characteristics:
 - Timing are preliminary and subject to change. Write in memorandum.
 - Tested
 - Guaranteed by Design
 - Guaranteed by Characterization