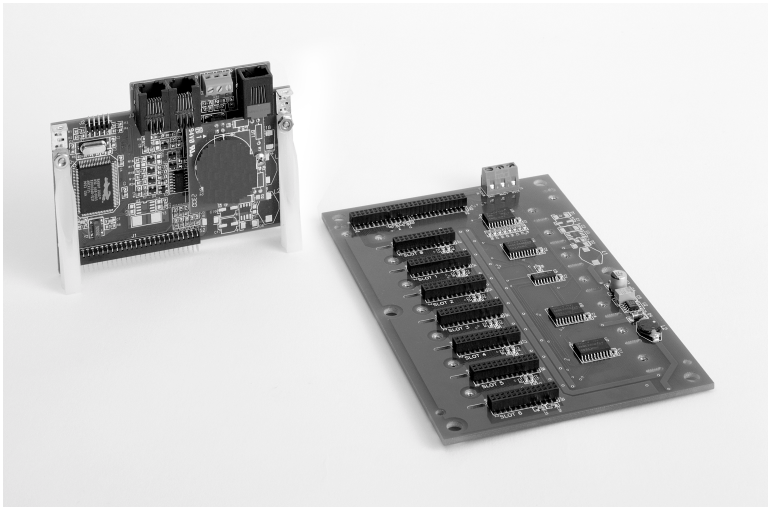

Smart Star (SR9000)

Modular C-Programmable Control System

User's Manual

010215 - A

Smart Star (SR9000) User's Manual

Part Number 019-0084 • 010215 - A • Printed in U.S.A.

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Notice to Users

When a system failure may cause serious consequences, protecting life and property against such consequences with a backup system or safety device is essential. The buyer agrees that protection against consequences resulting from system failure is the buyer's responsibility.

This device is not approved for life-support or medical systems.

All Z-World products are 100 percent functionally tested. Additional testing may include visual quality control inspections or mechanical defects analyzer inspections. Specifications are based on characterization of tested sample units rather than testing over temperature and voltage of each unit. Z-World may qualify components to operate within a range of parameters that is different from the manufacturer's recommended range. This strategy is believed to be more economical and effective. Additional testing or burn-in of an individual unit is available by special arrangement.

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TABLE OF CONTENTS

1. INTRODUCTION

Chapter 1 introduces the Smart Star embedded control system and describes the features associated with the backplane chassis and the CPU card. The tool kit containing the hardware essentials to begin using the Smart Star is described, and the software highlights are presented.

The Smart Star is a modular and expandable embedded control system whose configuration of digital I/O, A/D converter, D/A converter, and relay I/O cards can be tailored to a large variety of demanding real-time control and data acquisition applications.

The typical Smart Star system consists of a rugged backplane with a built-in voltage regulator, a CPU card, and one or more I/O cards. The CPU card plugs into a designated slot on the backplane chassis, which has seven additional slots available for I/O cards to be used in any combination. A high-performance Rabbit 2000 microprocessor on the CPU card operates at 25.8 MHz to provide fast data processing.

1.1 Features

- C-programmable to create a custom user interface
- Flexible functionality—modular configuration allows interchanging or replacing individual I/O cards
- Expandable—up to 168 I/O ports
- RS-232 and RS-485 serial ports allow networking to other Smart Star units, controllers, or enterprise computing centers
- 128K SRAM and 512K flash memory, optional 512K SRAM
- Real-time clock
- Watchdog supervisor
- Optional backup battery
- RabbitLink Ethernet gateway available for remote download/debug, Web serving, and E-mail

Table 1 lists the I/O cards that are available for the Smart Star control system. Appendix A provides detailed specifications for the Smart Star backplane and the CPU card.

Table 1. Smart Star I/O Cards

I/O Card	Model	Features
Digital I/O	SR9200	16 digital inputs, 8 digital sinking outputs
	SR9210	8 digital inputs, 16 digital sinking outputs
	SR9220	8 digital inputs, 8 digital sinking outputs
	SR9205	16 digital inputs, 8 digital sourcing outputs
	SR9215	8 digital inputs, 16 digital sourcing outputs
	SR9225	8 digital inputs, 8 digital sourcing outputs
A/D Converter	SR9300	12-bit A/D converter, 11 channels, 0 V – 10 V
	SR9310	12-bit A/D converter, 11 channels, -10 V – +10 V
	SR9320	12-bit A/D converter, 11 channels, 4 mA – 20 mA

Table 1. Smart Star I/O Cards (continued)

I/O Card	Model	Features
D/A Converter	SR9400	12-bit D/A converter, 8 channels, 0 V – 10 V
	SR9410	12-bit D/A converter, 8 channels, -10 V – +10 V
	SR9420	12-bit D/A converter, 8 channels, 4 mA – 20 mA
Relay	SR9500	5 SPST relays and 1 SPDT relay, each protected with onboard snubbers
	SR9510	8 SPDT relays (no snubbers)

1.2 User Connections

Connections to the I/O cards are made via a ribbon cable connector or optional field wiring terminals that are either pluggable or have screw terminals. Three different Field Wiring Terminals (FWTs) are available. Table 2 lists the I/O cards and the Z-World part numbers for the corresponding FWTs.

Table 2. Guide to FWT Selection

FWT Description	I/O Cards	Z-World Part Number	
		Pluggable Terminals	Screw Terminals
			
FWT27	Digital I/O Relay (SR9510)	101-0420	101-0424
FWT18	A/D Converter D/A Converter	101-0421	101-0425
FWT18R	Relay (SR9500)	101-0422	101-0426

Appendix B, “Field Wiring Terminals,” provides further information on FWTs, including their dimensions.

1.3 Development and Evaluation Tools

1.3.1 Tool Kit

The Tool Kit has the hardware essentials that you need to create and use your own Smart Star control system.

The items in the Tool Kit and their use are as follows:

- ***Smart Star (SR9000) User's Manual*** with schematics for backplane chassis and CPU card (this document).
- User manuals for available I/O cards.
- Programming cable, used to connect your PC serial port to the Smart Star CPU card to write and debug C programs that run on the Smart Star control system.
- FWT27 pluggable field wiring terminal.
- Screwdriver.
- DC power supply, used to power the backplane, which in turn supplies power to the CPU card and the I/O cards. The DC power supply accepts an AC input of 100 V to 240 V at up to 0.6 A, and delivers a DC output up to 1.1 A at 24 V.

1.3.2 Software

The Smart Star control system is programmed using Z-World's Dynamic C Premier, an integrated development environment that includes an editor, a C compiler, and a debugger. Library functions and software drivers provide an easy-to-use interface for the Smart Star control system. Dynamic C Premier is sold separately.

The programming cable has a level converter board in the middle of the cable since the Smart Star control system programming port on the CPU card supports CMOS logic levels, and not the higher voltage RS-232 levels that are used by PC serial ports. When the programming cable is connected, Dynamic C running on the PC can hard-reset the Smart Star control system and cold-boot it. The cold boot includes compiling and downloading a BIOS program that stays resident while you work. If you crash the target, Dynamic C will automatically reboot and recompile the BIOS if it senses that a target communication error occurred or that the BIOS source code has changed.

You have a choice of doing your software development in the flash memory or in the static RAM included on the CPU card. The advantage of working in RAM is to save wear on the flash memory, which is limited to about 100,000 writes.

Note that an application can be developed in RAM, but cannot run standalone from RAM after the programming cable is disconnected. All standalone applications can only run from flash memory.

The disadvantage of using flash is that interrupts must be disabled for approximately 5 ms whenever a break point is set in the program. This can crash fast interrupt routines that are running while you stop at a break point or single-step the program. Flash memory or SRAM is selected on the **Options** > **Compiler** menu.

2. GETTING STARTED

Chapter 2 explains how to connect the power supply to the Smart Star backplane, how to install the CPU card on the backplane, and how to connect the programming cable to the CPU card. Once you run a sample program to demonstrate that you have connected everything correctly, you will be ready to go on to install I/O cards and finish developing your system.

2.1 Attach the CPU Card to the Backplane

1. Orient the backplane with the **PROCESSOR SLOT** facing away from you as shown in Figure 1.

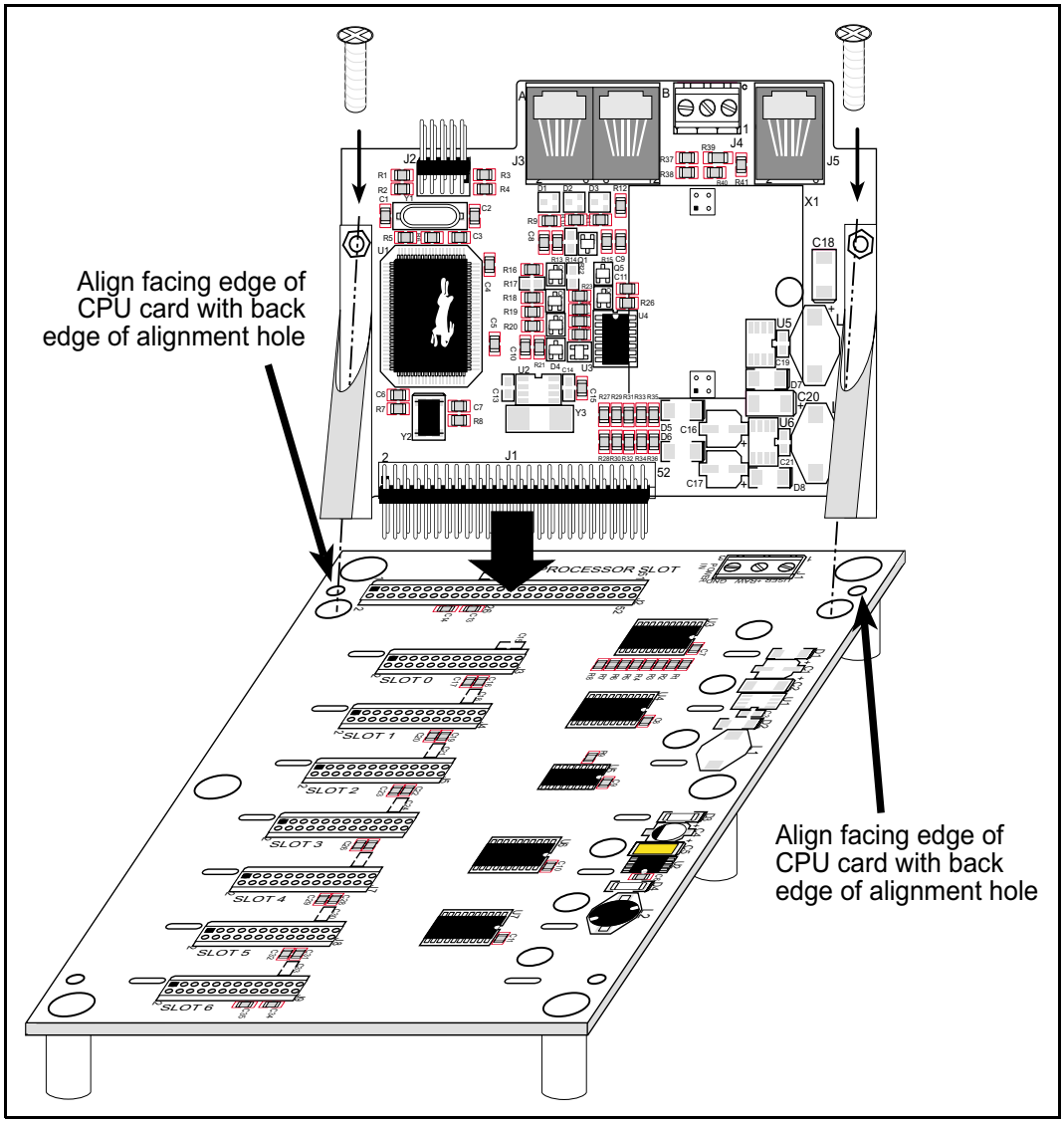


Figure 1. Attach the CPU Card to the Backplane

The CPU card is supplied without the optional backup battery board. If you have purchased a backup battery board, refer to Section C.2.4 for installation instructions. It is more convenient to install the backup battery board ***before*** the CPU card is mounted on the backplane.

2. Position the CPU card above the backplane as shown in Figure 1.
3. Carefully insert the CPU card header into the **PROCESSOR SLOT** on the backplane and line up the facing edge of the CPU card with the back edge of the alignment holes on the backplane as shown in Figure 1.
4. Use the two 4-40 screws supplied with the CPU card to anchor the plastic brackets so that they hold the CPU card firmly in place on the backplane.

2.2 Connect the Power Supply

Connect the power supply to the **POWER IN** connector on the backplane—the red (positive) wire to **+RAW** and the black (negative) wire to **GND**, as shown in Figure 2.

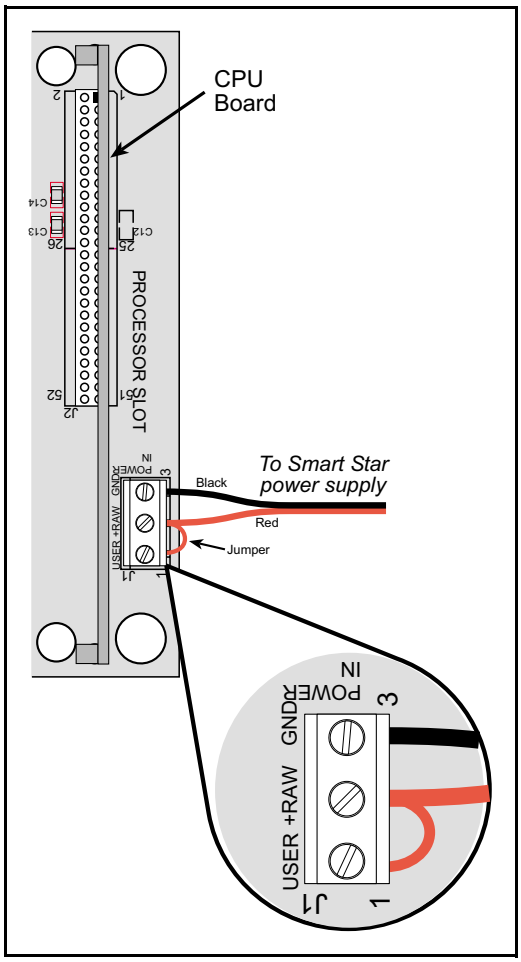


Figure 2. Power Supply Connections

> Be careful to hook up the positive and negative leads ***exactly*** as described. Only the +5 V circuitry is protected against reverse polarity.

A **USER** connection is supplied on the backplane to allow an independent power supply to be used for future development. For now, use a jumper to connect **USER** to **+RAW** so that they share the same power supply.

Notice to Customers Outside North America

The power supply included with the Smart Star Tool Kit may be used worldwide. Customers outside North America simply need to exchange the line cord and plug from the power supply to their wall outlet with one available locally.

1. To exchange the line cord and plug, first remove the existing line cord. To access the screws, use a screwdriver to gently lift up and remove the plastic insulating cover.

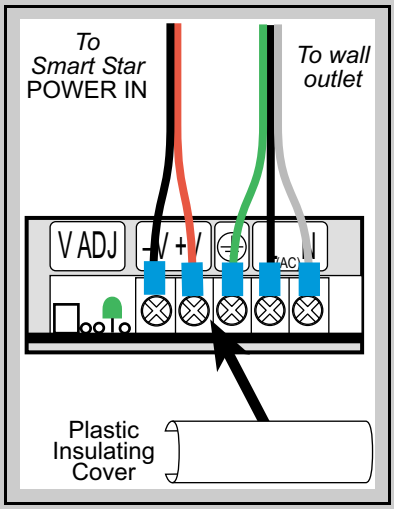


Figure 3. Power Supply Connections

2. Unscrew the wires at the ground, **L**, and **N** terminals.
3. Attach the line cord that you obtained locally to the power supply. Be sure to follow any color-coding conventions, for example, green/yellow to ground, brown to **L**, and blue to **N** terminals.
4. Ensure that the wires are attached securely and are not touching each other. Snap on the plastc insulating cover.

> The power supply included with the Smart Star Tool Kit is intended for development purposes only.

2.3 Programming Cable Connections

1. Connect the programming cable to the CPU card.

Connect the 10-pin **PROG** connector of the programming cable to header J2 on the CPU card as shown in Figure 4. Connect the other end of the programming cable to a COM port on your PC. Note that COM1 on the PC is the default COM port in the Dynamic C Premier installation.

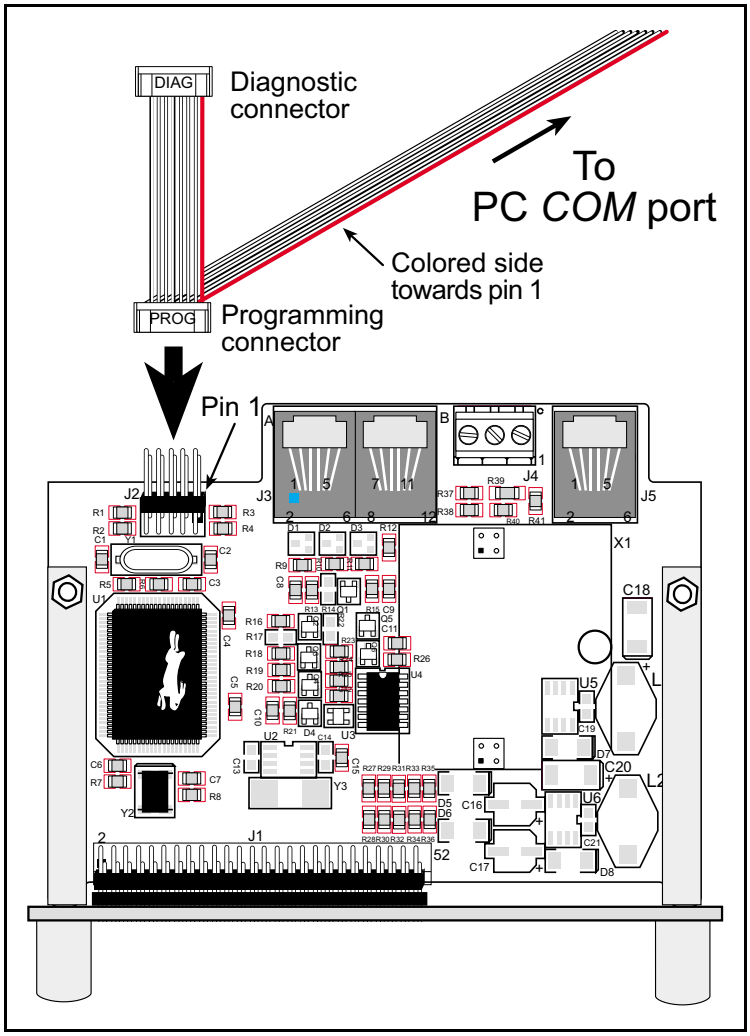


Figure 4. Programming Cable Connections

2. Apply power.

Plug the power supply in to a nearby outlet. The CPU card is now ready to be used.

A hardware RESET is accomplished by unplugging the power supply, then plugging it back in.

2.4 Installing Dynamic C Premier

If you have not yet installed Dynamic C Premier, you may do so by inserting the Dynamic C Premier CD in your PC's CD-ROM drive. The CD will auto-install unless you have disabled auto-install on your PC.

If the CD does not auto-install, click **Start > Run** from the Windows **Start** button and browse for the **setup.exe** file on your CD drive. Click **OK** to begin the installation once you have selected the **setup.exe** file.

The ***Dynamic C Premier User's Manual*** provides detailed instructions for the installation of Dynamic C and any future upgrades.

2.5 Starting Dynamic C

Once the CPU card is installed and connected as described above, start Dynamic C by double-clicking on the Dynamic C icon or by double-clicking on the **.exe** file associated with **DcRab** in the Dynamic C directory.

Dynamic C should detect the CPU card and go through a sequence of steps to cold-boot the CPU card and to compile the BIOS. If the error message "Rabbit Processor Not Detected" appears, you have probably connected to a different PC serial port than the default serial port selected during the installation of Dynamic C Premier. You can change the serial port used by Dynamic C with the **OPTIONS** menu, then try to get Dynamic C to recognize the CPU card by selecting **Recompile BIOS** on the **Compile** menu. Try the different COM ports in the **OPTIONS** menu until you find the one you are connected to. If you still cannot get Dynamic C to recognize the target on any port, then the hookup may be wrong or the COM port is not working on your PC.

If you receive the "BIOS successfully compiled …" message after pressing **<Ctrl-Y>** or starting Dynamic C, and this message is followed by "Target not responding," it is possible that your PC cannot handle the 115,200 bps baud rate. Try changing the baud rate to 57,600 bps as follows.

1. Open the BIOS source code file named **RABBITBIOS.C**, which can be found in the **BIOS** directory.
2. Change the line

   ```
   #define USE115KBAUD 1   // set to 0 to use 57600 baud
   ```

   to read as follows.

   ```
   #define USE115KBAUD 0   // set to 0 to use 57600 baud
   ```

3. Locate the **Serial options** dialog in the Dynamic C **Options** menu. Change the baud rate to 57,600 bps, then press **<Ctrl-Y>**.

When you receive the "BIOS successfully compiled …" message and do not receive a "Target not responding" message, the target is now ready to compile a program.

2.6 PONG.C

You are now ready to test your set-up by running a sample program.

Find the file **PONG.C**, which is in the Dynamic C **SAMPLES** folder. To run the program, open it with the **File** menu (if it is not still open), compile it using the **Compile** menu, and then run it by selecting **Run** in the **Run** menu. The **STDIO** window will open and will display a small square bouncing around in a box.

This program does not test the serial ports on the CPU card, but does ensure that the CPU is basically functional.

2.7 Where Do I Go From Here?

If there are any problems at this point, call Z-World Technical Support at (530)757-3737.

If the sample program ran fine, you are now ready to go on to install I/O cards, explore other Smart Star features, and develop your own applications.

Chapter 3, "Subsystems," provides detailed information about the CPU card, and how to install the I/O cards. Be sure to take the total current consumption of the individual cards into account when selecting a power supply. Appendix C.1, "Current Requirements," provides more detailed information. Chapter 4, "Software," describes the Dynamic C software libraries and introduces some sample programs for use with the CPU card. Appendix A, "Smart Star Specifications," provides specifications for the backplane and the CPU card, including mounting and clearance recommendations.

Separate manuals have been prepared for the various I/O cards, and include complete information about their pinouts and Dynamic C software libraries, including sample programs.

Once you have developed your application and bench-tested the finished system, you may install the finished system.

3. SUBSYSTEMS

Chapter 3 describes the principal subsystems for the Smart Star.

- Switching Between Program Mode and Run Mode
- Power Distribution
- Smart Star CPU Card Subsystems
- Serial Communication
- Memory
- Installing I/O Cards

3.1 Switching Between Program Mode and Run Mode

The CPU card is automatically in Program Mode when it is powered up with the programming cable attached, and is automatically in Run Mode when it is powered up with no programming cable attached. See Figure 5. The CPU card remains in Run Mode when the **DIAG** connector on the programming cable is attached to allow the programming port to be used as a diagnostic port as explained in Appendix D.

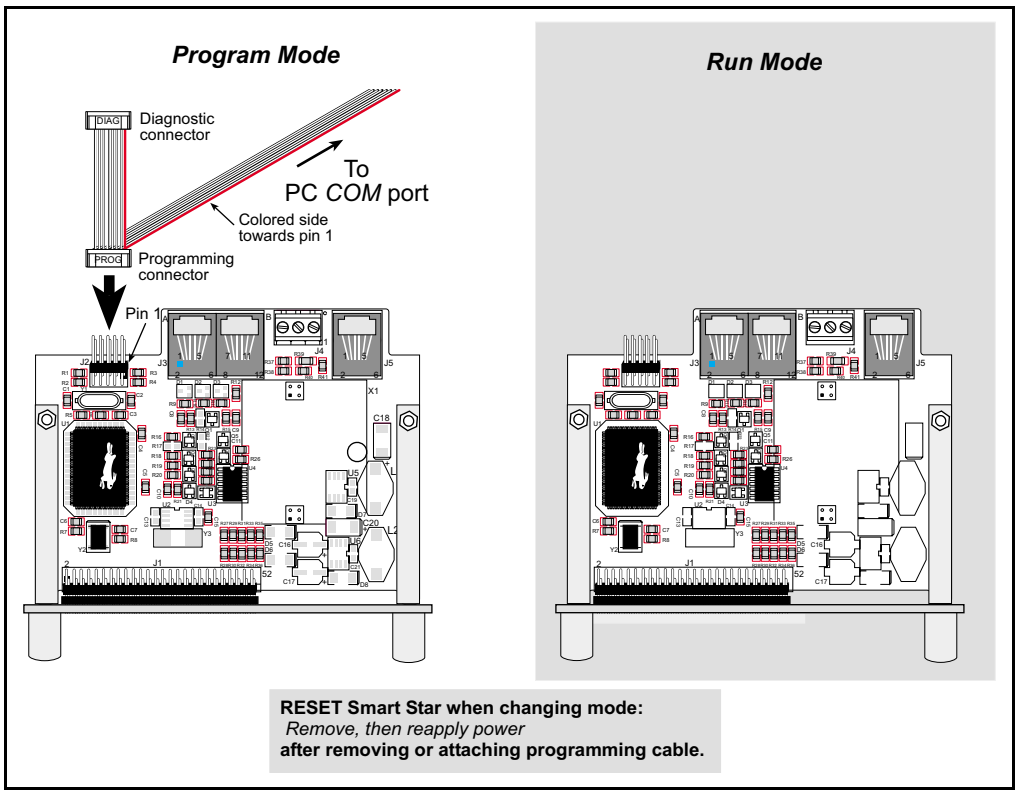


Figure 5. Smart Star Program Mode and Run Mode Set-Up

3.1.1 Detailed Instructions: Changing from Program Mode to Run Mode

1. Disconnect the programming cable from header J2 of the CPU card.
2. Reset the Smart Star by unplugging the power supply, then plugging it back in.

The Smart Star is now ready to operate in the Run Mode.

3.1.2 Detailed Instructions: Changing from Run Mode to Program Mode

1. Attach the programming cable to header J2 of the CPU card.
2. Reset the Smart Star by unplugging the power supply, then plugging it back in.

The Smart Star is now ready to operate in the Program Mode.

3.2 Power Distribution

Power is supplied to the Smart Star control system from an external source through header J1 on the backplane. The +5 V circuitry on the Smart Star control system is protected against reverse polarity by a Schottky diode at D3 as shown in Figure 6.

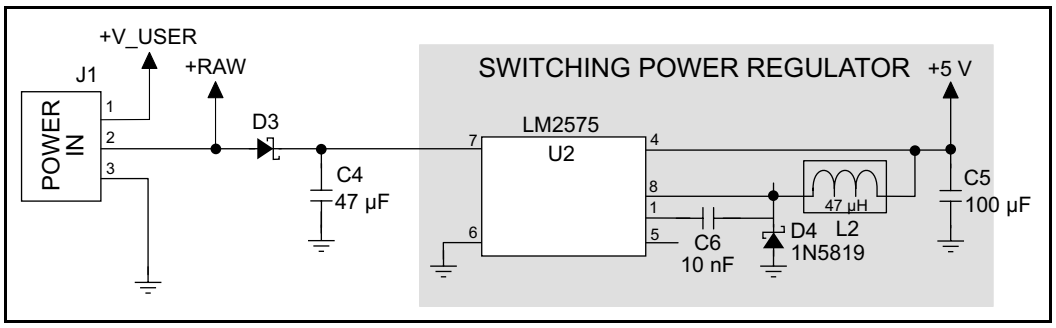


Figure 6. Smart Star Control System Power Supply Schematic

Capacitor C4 provides surge current protection for the voltage regulator, and allows the external power supply to be located some distance away from the Smart Star control system. A switching power regulator is used. The **+RAW** input voltage may range from 9 V to 30 V (15 V to 30 V you plan to use a D/A converter card).

The backplane has inputs for two separate power supplies on header J1, **+RAW** and **USER**. The **+RAW** power supply goes to the switching power regulator, which outputs the +5 V DC used by the CPU card and by the I/O cards plugged into the backplane. The **USER** connection allows a different voltage to be available on the I/O cards for future development.

Always connect **USER** to **+RAW** with a jumper wire between terminals 1 and 2 on header J1 for the development activities described in the Smart Star manuals.

The backplane also has room for a +3.3 V power supply, and the CPU card has room for a +5 V and a +3.3 V power supply. These locations were included for future development of the Smart Star control system, and are not supported at the present time.

Figure 7 shows how the power supplies are distributed on the backplane and on the CPU card.

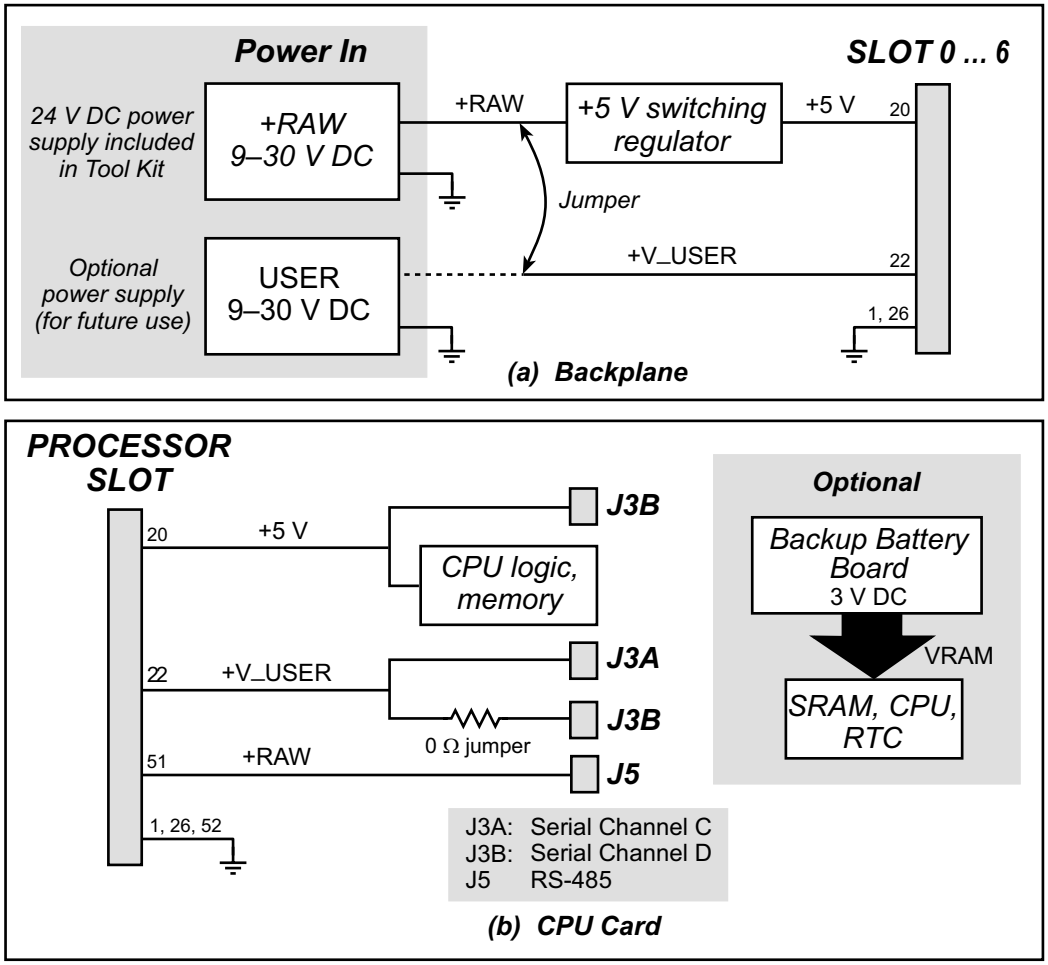


Figure 7. Smart Star Power Supplies—Backplane and CPU Card

Figure 8 shows how the power supplies are distributed on the I/O cards.

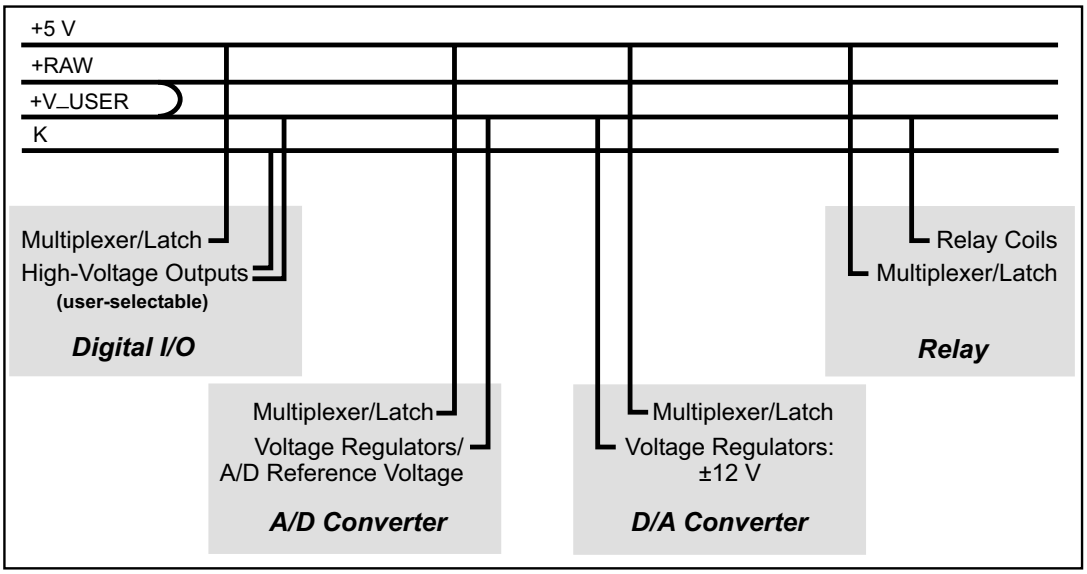


Figure 8. Smart Star Power Distribution on I/O Cards

Note that Z-World recommends tying **+RAW** to **+V_USER** as explained in Section 2.2, "Connect the Power Supply."

The user has the option of using a separate power supply to K when configuring the high-power outputs for the digital I/O cards. The connection to K is through the user interface on the digital I/O card. Further details are provided in the ***Digital I/O Cards User's Manual***.

3.3 Smart Star CPU Card Subsystems

Figure 9 shows the Rabbit-based subsystems designed into the Smart Star CPU card.

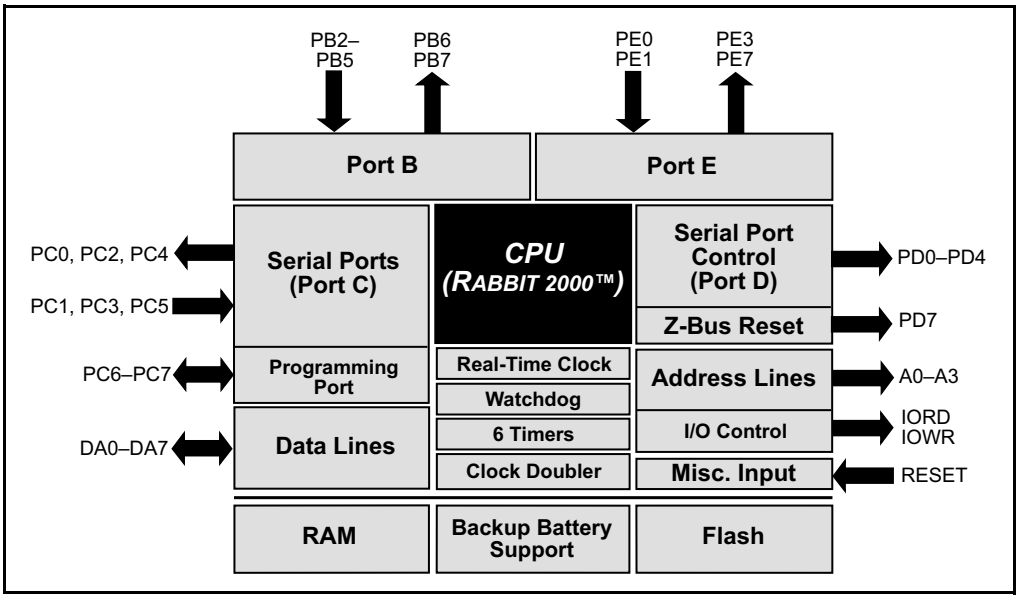


Figure 9. Smart Star CPU Card Rabbit-Based Subsystems

3.3.1 Backplane Slots

The backplane serves to make the CPU card accessible to up to seven I/O cards plugged in to **SLOT 0** through **SLOT 6** on the backplane. Figure 10 shows the pinout for **SLOT 0** through **SLOT 6** (headers J3–J9) on the backplane.

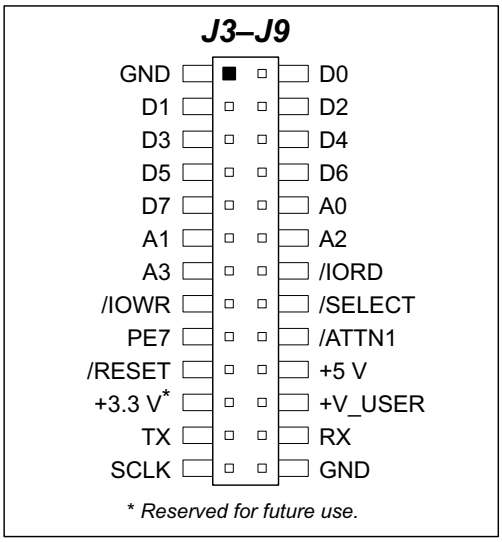


Figure 10. Pinout for SLOT 0 Through SLOT 6 (Headers J3–J9) on the Backplane

3.4 Serial Communication

The CPU card has one screw terminal header for RS-485 serial communication (J4), one RJ-12 jack for RS-485 serial communication (J5), and two RJ-12 jacks for RS-232 serial communication (J3A, J3B). The pinouts are shown in Figure 11.

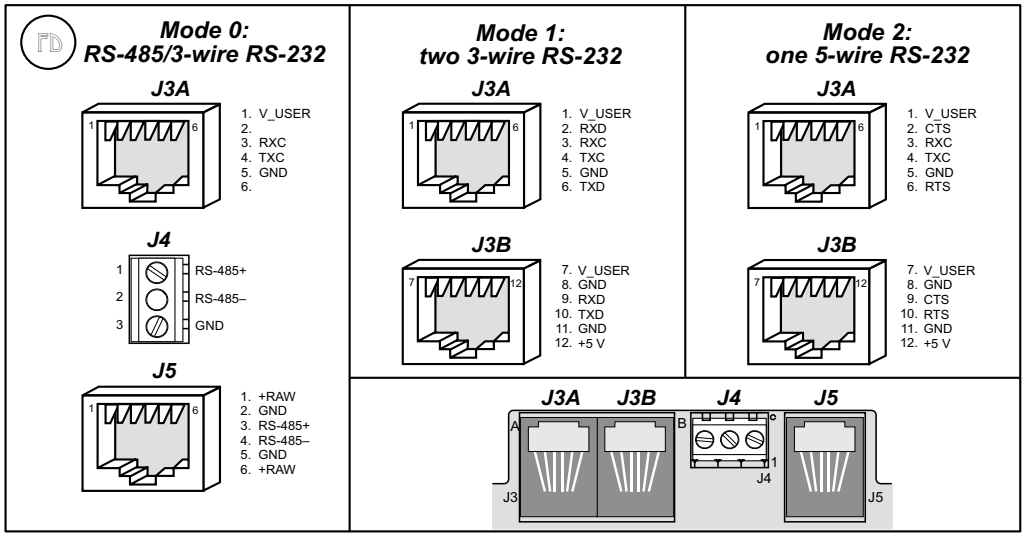


Figure 11. Smart Star CPU Card Serial Pinout

The factory default for the CPU card is one RS-232 (3-wire) and one RS-485 serial channel, corresponding to Mode 0 in Figure 11. The other modes shown in Figure 11 are set in software via the Dynamic C **`serMode`** function call (see Section 4.3, "Serial Communication APIs.")

3.4.1 RS-232

The CPU card's RS-232 serial channel is connected to an RS-232 transceiver. The transceiver provides the voltage output, slew rate, and input voltage immunity required to meet the RS-232 serial communication protocol. Basically, the chip translates the Rabbit 2000's 0 V to +Vcc signals to RS-232 signal levels. Note that the polarity is reversed in an RS-232 circuit so that +5 V is output as approximately -10 V and 0 V is output as approximately +10 V. The transceiver also provides the proper line loading for reliable communication.

The maximum baud rate is 115,200 bps. RS-232 can be used effectively at this baud rate for distances up to 15 m.

The Rabbit 2000 serial port C TXD and RXD signals are presented either as RS-232 TX and RX or as RTS/CTS handshaking, depending on the mode selected with the Dynamic C function **`serMode`**. The RS-232 signals are available on headers J3A and J3B, which are RJ-12 jacks.

3.4.2 RS-485

The CPU card has one RS-485 serial channel, which is connected to the Rabbit 2000 serial port C through an RS-485 transceiver. The chip's slew rate limiters provide for a maximum baud rate of 250,000 bps, and allows networking over a distance of up to 300 m (or 1000 ft.). The half-duplex communication uses the Rabbit 2000's PD4 pin to control the data enable on the communication line.

The RS-485 signals are available on the CPU card through screw terminal header J4 and on header J5, an RJ-12 jack.

The Smart Star control system can be used in an RS-485 multidrop network. Connect the 485+ to 485+ and 485– to 485– using single twisted-pair wires on the CPU card's header J4 as shown in Figure 12.

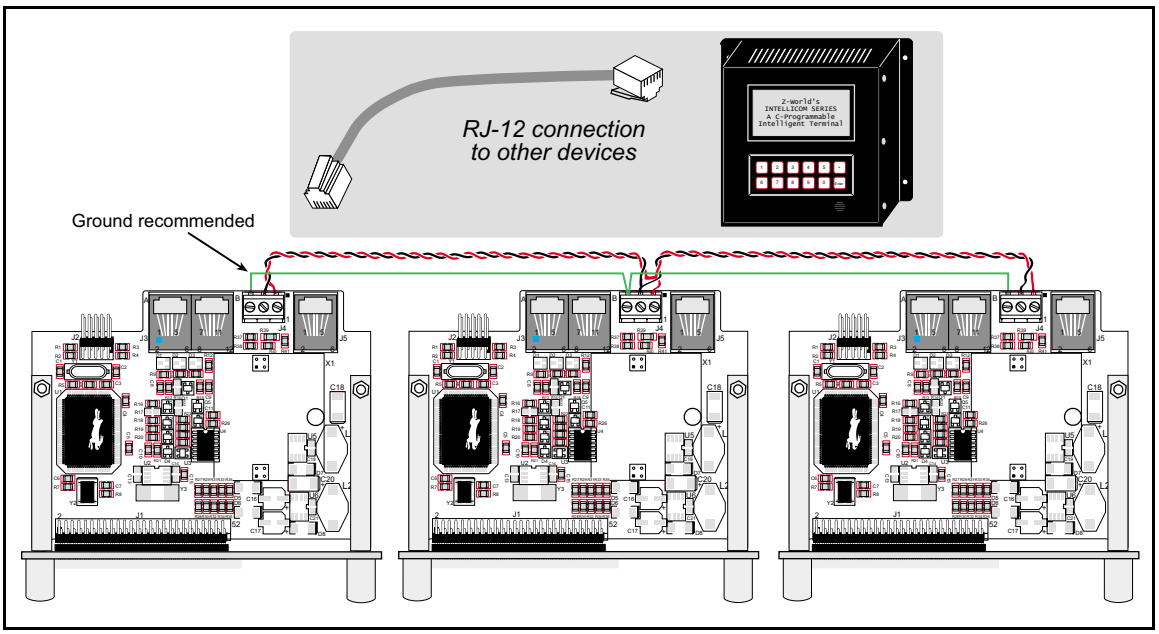


Figure 12. Multidrop Smart Star Network

The Smart Star's CPU card may be hooked up to a single RS-485 compatible device through the RS-485 RJ-12 jack, J5, using cables with RJ-12 plugs. Note that J5 has +RAW and GND, which means up to 250 mA can be supplied to a device such as Z-World's Intellicom operator interface whose RJ-12 jack is wired compatibly. In this case, no separate power supply is needed for the attached device.

All Smart Star control systems on an RS-485 multidrop network must be connected through header J5 on the CPU card.

The CPU card comes with a 220 Ω termination resistor and 681 Ω bias resistors already installed, as shown in Figure 13.

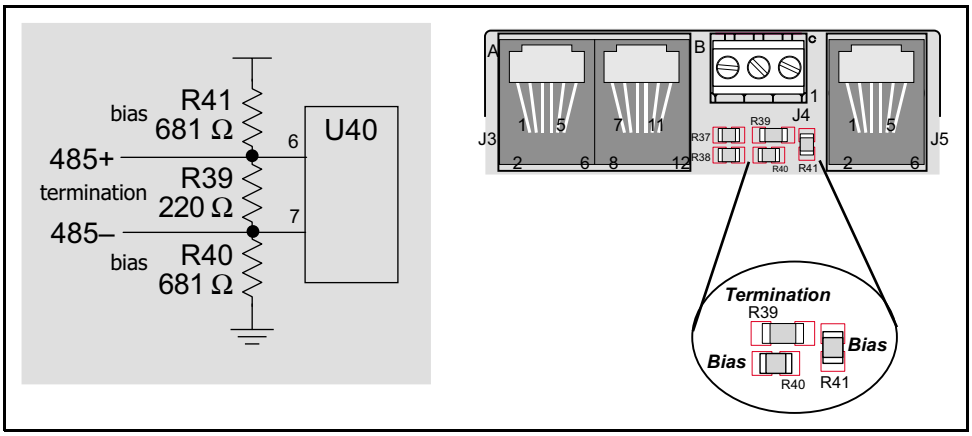


Figure 13. RS-485 Termination and Bias Resistors

The load these bias and termination resistors present to the RS-485 transceiver limits the number of Smart Star systems in a multidrop network to one master and three slaves, unless the bias and termination resistors are removed. When using more than four Smart Star systems in a multidrop network, leave the 681 Ω bias resistors in place on the master Smart Star system, and leave the 220 Ω termination resistor in place on the Smart Star system at each end of the network.

3.4.3 Programming Port

The CPU card has a 10-pin programming header labeled J2. The programming port uses the Rabbit 2000's serial port A for communication. The Rabbit 2000 startup-mode pins (SMODE0, SMODE1) are presented to the programming port so that an externally connected device can force the Rabbit 2000 to start up in an external bootstrap mode.

Refer to the ***Rabbit 2000 Microprocessor User's Manual*** for more information related to the bootstrap mode.

The programming port can also be used as a diagnostic port when the **DIAG** connector on the programming cable is used to connect the programming port to a PC or other device. See Appendix D, "Programming Cable," for more information.

3.5 Memory

3.5.1 SRAM

The Smart Star CPU card is designed to accept 128K or 512K of static RAM packaged in an SOIC case.

The standard models come with 128K of static RAM. Figure 14 shows the locations and the jumper settings for the jumpers at JP1 used to set the SRAM size. The "jumpers" are 0 Ω surface-mounted resistors.

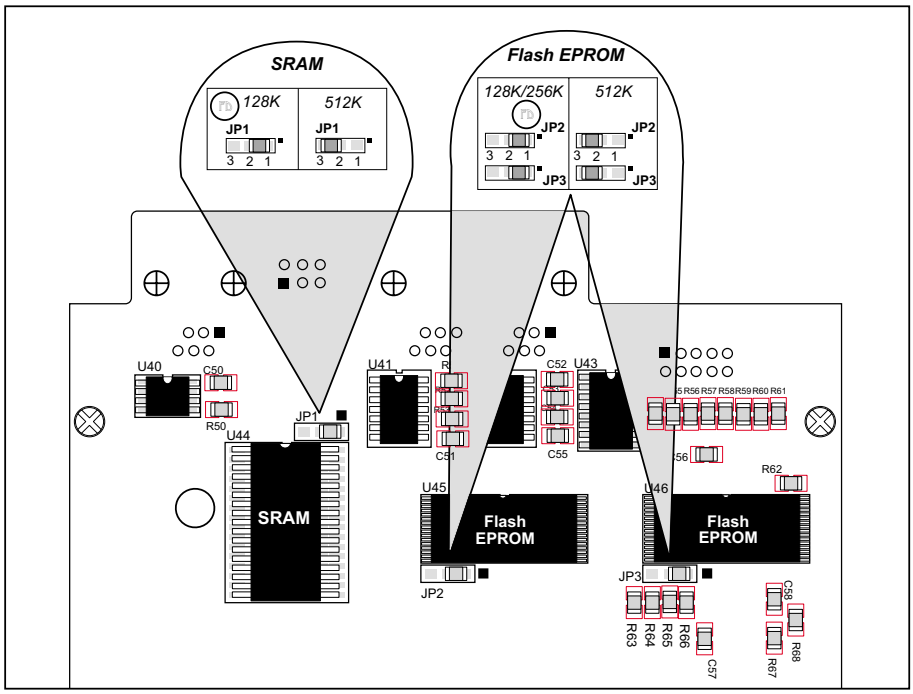


Figure 14. Smart Star CPU Card Jumper Settings for Static RAM and Flash Memory Size

3.5.2 Flash EPROM

The Smart Star CPU card is also designed to accept 128K to a total of 512K of flash memory packaged in a TSOP case.

The CPU card comes with two 256K flash memory chips. Figure 14 shows the locations and the jumper settings for the jumpers at JP2 and JP3 used to set the flash memory size. The "jumpers" are 0 Ω surface-mounted resistors.

Z-World recommends that any customer applications should not be constrained by the sector size of the flash memory since it may be necessary to change the sector size in the future.

3.5.3 Dynamic C Premier BIOS Source Files

The Dynamic C Premier BIOS source files handle different standard RAM and flash memory sizes automatically.

3.6 Installing I/O Cards

1. Orient the backplane with the CPU card already installed and facing towards you as shown in Figure 15.

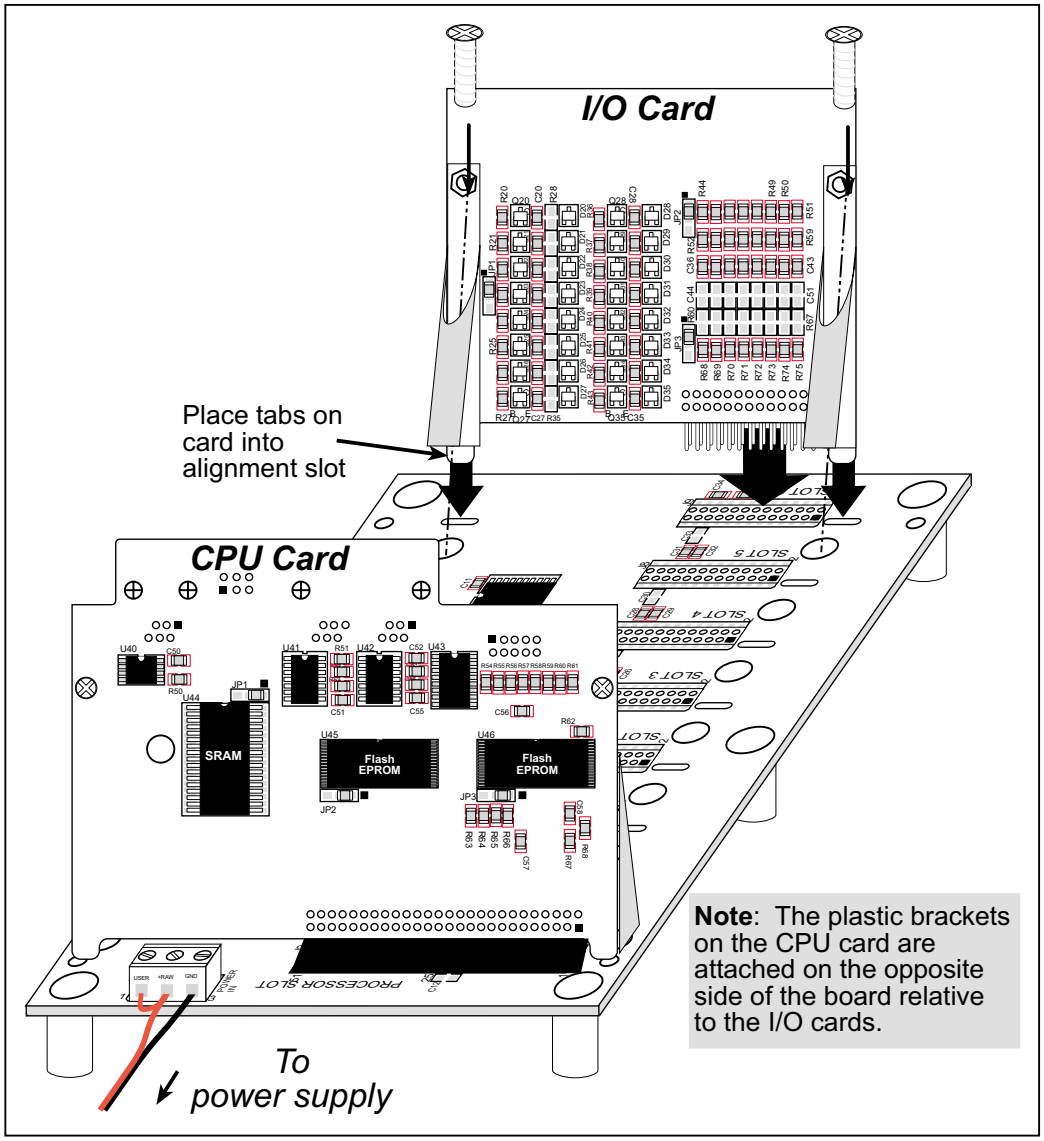


Figure 15. Installing I/O Cards on the Backplane

2. Position the new I/O card above the backplane over any unused slot position (**SLOT 0** to **SLOT 6**) as shown in Figure 15. Note the slot number and the type of I/O card since Dynamic C addresses the I/O cards by slot number.
3. Carefully insert the I/O card header into the slot on the backplane and line up the tabs on the I/O cards with the slots on the backplane as shown in Figure 15.
4. Use the two 4-40 screws supplied with the I/O card to ensure that the plastic brackets anchor the I/O card firmly on the backplane. Tighten the screws as needed.

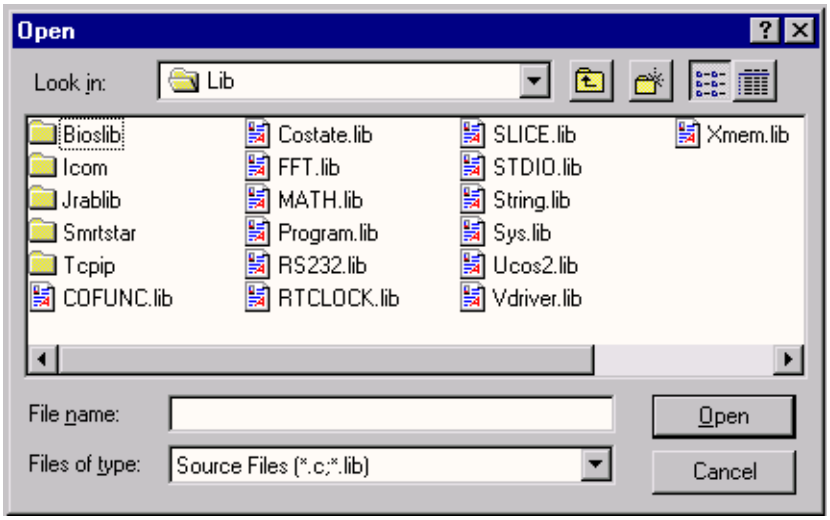
4. SOFTWARE

Dynamic C Premier is an integrated development system for writing embedded software. It runs on an IBM-compatible PC and is designed for use with Z-World controllers and other controllers based on the Rabbit microprocessor.

Chapter 4 provides the libraries, function calls, and sample programs related to the Smart Star backplane and CPU cards.

4.1 Dynamic C Libraries

With Dynamic C running, click **File** > **Open**, and select **Lib**. The following list of Dynamic C libraries and library directories will be displayed.



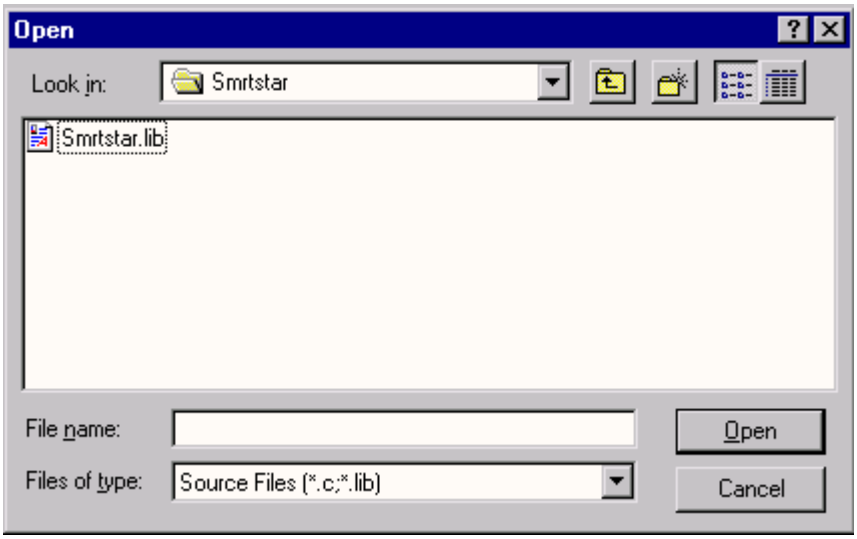
One library directory is specific to the Smart Star.

- **SMRTSTAR**—libraries associated with features specific to the Smart Star control system.

Other functions applicable to all devices based on the Rabbit 2000 microprocessor are described in the ***Dynamic C Premier User's Manual***.

4.1.1 Library Directories

The **SMRTSTAR** directory contains libraries required to operate the Smart Star control system.



- **SMRTSTAR.LIB**—This library supports all the functions needed by the Smart Star systems including digital I/O cards, relay cards, D/A converter and A/D converter cards, and serial communication.

Functions dealing with the backplane and the CPU card are described in this manual. Functions relevant to the individual I/O cards are described in the manual specific to the I/O card.

4.2 Smart Star Backplane Function APIs

4.2.1 Board Reset

```
void brdResetBus();
```

Resets all cards on the bus.

Return Value

None.

4.2.2 Board Initialization

```
void brdInit();
```

Initializes all port registers. Call this function at the beginning of the application.

Return Value

None.

4.3 Serial Communication APIs

```
int serMode(int mode);
```

User interface to set up up serial communication lines for the Smart Star control system. Call this function after **`serXOpen()`**.

Parameters

`mode` is the defined serial port configuration of the CPU card.

Mode	Serial Port	
	C	D
0	RS-232, 3-wire	RS-485
1	RS-232, 3-wire	RS-232, 3-wire
2	RS-232, 5-wire	CTS/RTS

Return Value

0 if correct mode, 1 if not.

ser485Tx();

Enables RS-485 transmission (disables receive) on serial port D.

Return Value

None.

See Also

`ser485Rx`

ser485Rx();

Disables RS-485 transmission (enables receive) on serial port D.

Return Value

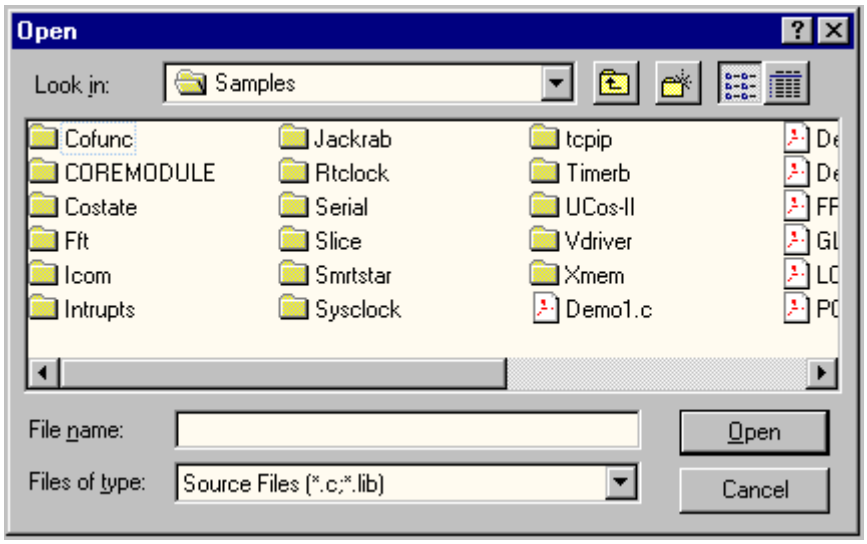
None.

See Also

`ser485Tx`

4.4 Sample Programs

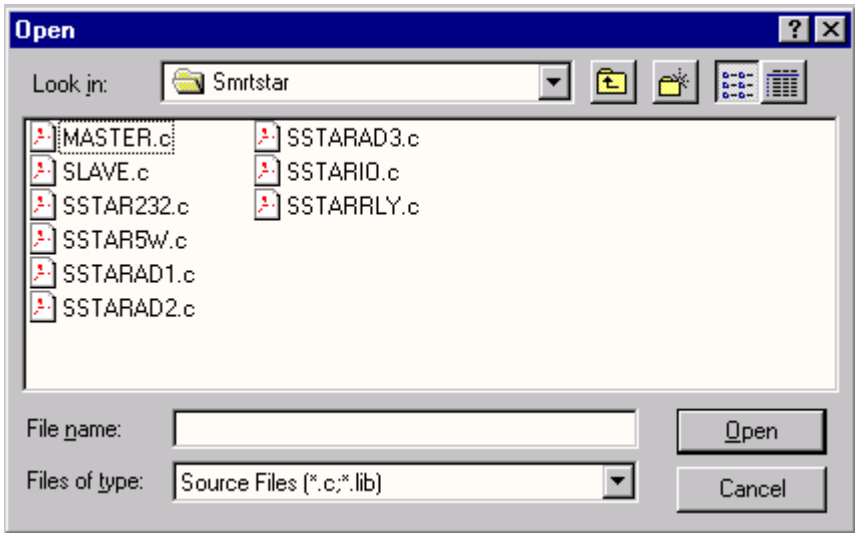
Sample programs are provided in the Dynamic C **Samples** folder, which is shown below.



The various folders contain specific sample programs that illustrate the use of the corresponding Dynamic C libraries. For example, the sample program **PONG.C** demonstrates the output to the **STDIO** window.

The **SMRTSTAR** folder provides sample programs specific to the Smart Star control system. Each sample program has comments that describe the purpose and function of the program. Follow the instructions at the beginning of the sample program.

Let's take a look at sample programs for the backplane and the CPU card in the **SMRTSTAR** folder.



- **MASTER.C**—Demonstrates a simple RS-485 transmission of lower case letters to a slave controller. The slave will send converted upper case letters back to the master controller for display in the **STDIO** window. Use **SLAVE.C** to program the slave controller.
- **SLAVE.C**—Demonstrates a simple RS-485 transmission of alphabetic characters to a master controller. The slave will send converted upper case letters back to the master controller for display in the **STDIO** window. Use **MASTER.C** to program the master controller.
- **SSTAR232.C**—Demonstrates a simple RS-232 loopback using both serial ports C and D.
- **SSTAR5W.C**—Demonstrates simple 5-wire RS-232 communication with flow control.

4.5 Using Dynamic C

To run a sample program, open it with the **File** menu (if it is not still open), compile it using the **Compile** menu, and then run it by selecting **Run** in the **Run** menu. The CPU card must be in Program Mode (see Section 3.1, "Switching Between Program Mode and Run Mode") and must be connected to a PC using the programming cable as described in Section 2.3, "Programming Cable Connections".

More complete information on Dynamic C is provided in the ***Dynamic C Premier User's Manual***.

APPENDIX A.
SMART STAR SPECIFICATIONS

Appendix A provides the specifications for the Smart Star backplane and CPU card, and describes the conformal coating.

A.1 Electrical and Mechanical Specifications

A.1.1 Smart Star Backplane

Figure A-1 shows the mechanical dimensions for the Smart Star backplane.

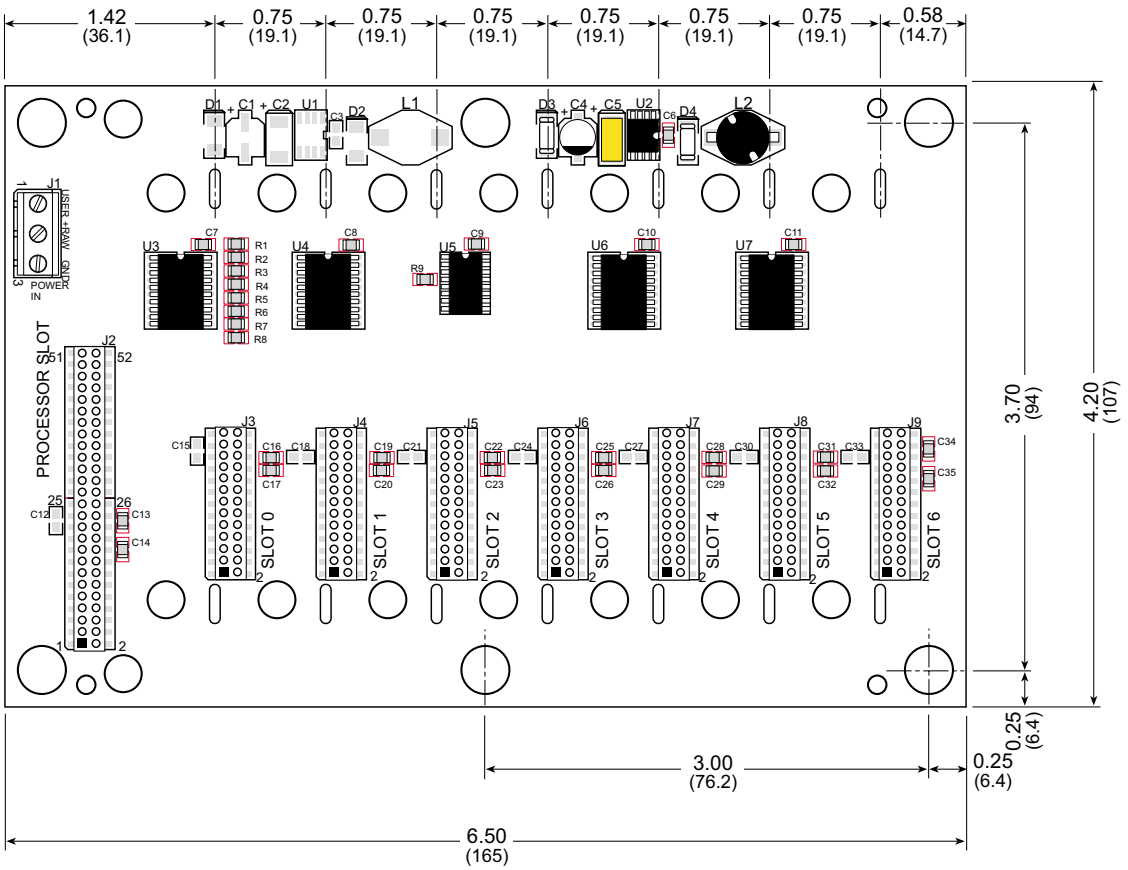


Figure A-1. Smart Star Backplane Dimensions

All diagram and graphic measurements are in inches followed by millimeters enclosed in parentheses.

Table A-1 lists the electrical, mechanical, and environmental specifications for the Smart Star backplane.

Table A-1. Smart Star Backplane Specifications

Parameter	Specification
Board Size	6.50" × 4.20" × 0.56" (165 mm × 107 mm × 14 mm)
Connectors	one 2 × 26 (CPU card slot), 2 mm seven 2 × 13 (I/O card slots), 2 mm
Slot Select	Each slot has a predefined dedicated set of addresses (see Appendix E and the software chapters in the individual I/O card manuals)
Temperature	–40°C to +70°C
Humidity	5% to 95%, noncondensing
External Input Voltage	9 V to 30 V DC at 1 A typical for onboard +5 V regulated supply; provision for independent 9 V to 30 V DC (**V_USER**) voltage source for I/O cards—the exact voltage for the second supply depends on the requirements of the specific I/O cards used (Z-World recommends tying **V_USER** to **+RAW** unless there is a specific need for an independent power supply)
Onboard Voltage Regulator	Surface-mount switching regulator sources 5 V at 1 A
Data Lines	Buffered bidrirectional data lines (D0–D7)
Address Lines	Buffered address lines (A0–A3)
Read/Write Control	Buffered IORD, IOWR
Reset	I/O cards and CPU card can be reset independently

A.1.2 CPU Card

Figure A-2 shows the mechanical dimensions for the CPU card.

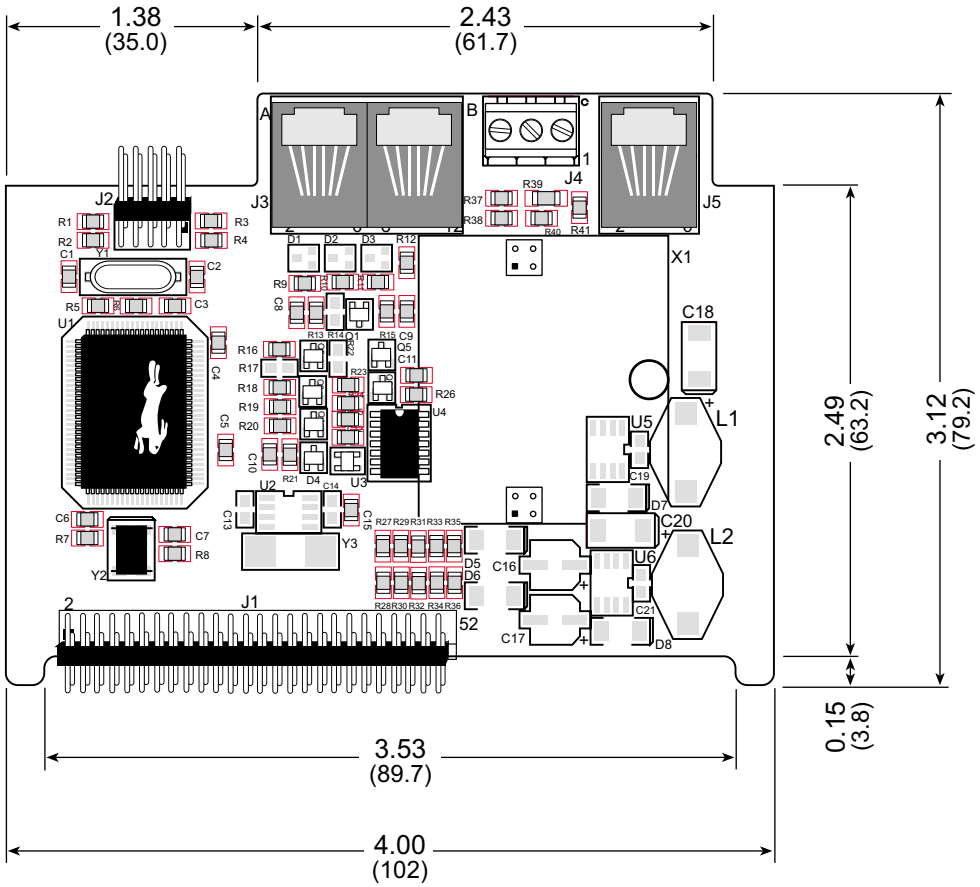


Figure A-2. CPU Card Dimensions

Table A-2 lists the electrical, mechanical, and environmental specifications for the CPU card.

Table A-2. CPU Card Specifications

Parameter	Specification
Board Size (with optional backup battery board)	4.00" × 3.12" × 1.00" (102 mm × 79.2 mm × 25.4 mm)
Temperature	–40°C to +70°C
Humidity	5% to 95%, noncondensing
Input Voltage	5 V DC at 150 mA typical
Microprocessor	Rabbit 2000™
Clock	25.8 MHz
SRAM	128K, surface mounted, 512K option
Flash EPROM	2 × 256K, surface mounted
Timers	Five 8-bit timers cascadable in pairs, one 10-bit timer with 2 match registers that each have an interrupt
Serial Ports	Three serial ports: • one CMOS-compatible programming port • remaining ports software-configurable as two 3-wire RS-232, one 5-wire RS-232, or one 3-wire RS-232/ one RS-485
Serial Rate	Selected baud rates up to 115, 200 bps CMOS-compatible port supports up to 6.45 Mbps (synchronous)
Watchdog/Supervisor	Yes
Time/Date Clock	Yes
Expansion Port	Supports up to 7 I/O cards
Backup Battery	Optional backup battery 3 V, 1000 mA·h

A.2 Conformal Coating

The areas around the crystal oscillator and the battery backup circuit on the CPU card have had the Dow Corning silicone-based 1-2620 conformal coating applied. The conformally coated areas are shown in Figure A-3. The conformal coating protects these high-impedance circuits from the effects of moisture and contaiminants over time.

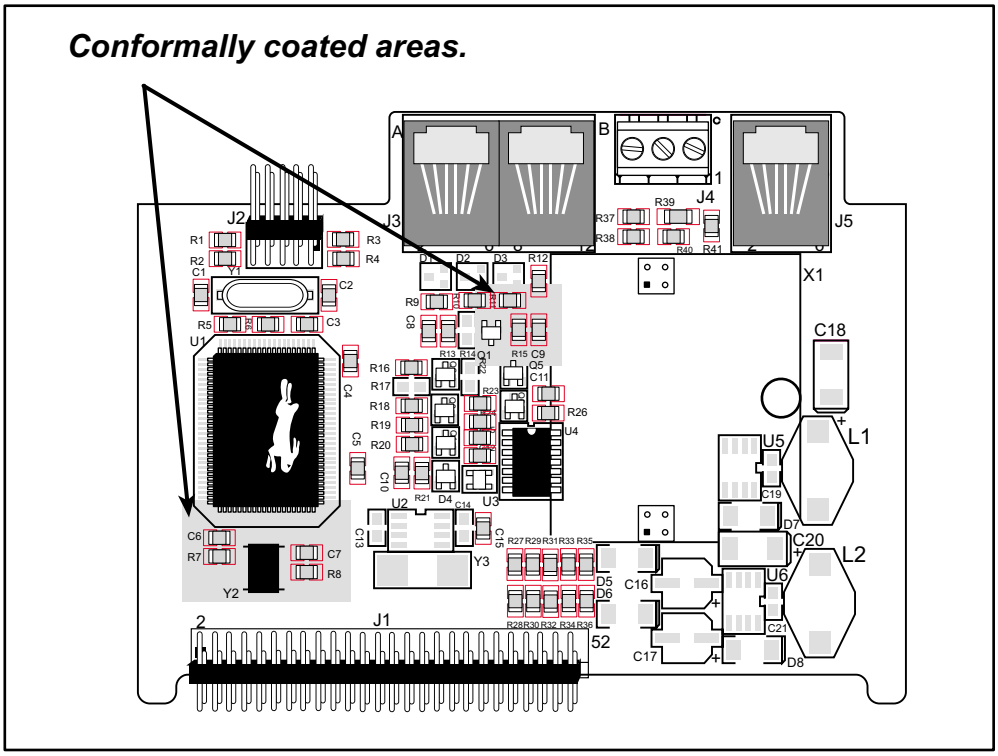


Figure A-3. CPU Card Areas Receiving Conformal Coating

Any components in the conformally coated area may be replaced using standard soldering procedures for surface-mounted components. A new conformal coating should then be applied to offer continuing protection against the effects of moisture and contaminants.

For more information on conformal coatings, refer to Rabbit Semiconductor Technical Note 303, ***Conformal Coatings***.

APPENDIX B. FIELD WIRING TERMINALS

Appendix B explains how to prepare the connector on an I/O card to accept a field wiring terminal, and how to secure the field wiring terminal to the I/O card. The dimensions for the field wiring terminals are included.

B.1 Selecting and Installing a Field Wiring Terminal

Connections to the I/O cards are made via a ribbon cable connector or optional field wiring terminals that are either pluggable or have screw terminals. Three different Field Wiring Terminals (FWTs) are available. Table B-1 lists the I/O cards and the Z-World part numbers for the corresponding FWTs.

Table B-1. Guide to FWT Selection

FWT Description	I/O Cards	Z-World Part Number	
		Pluggable Terminals 	Screw Terminals 
FWT27	Digital I/O (SR9200 series)	101-0420	101-0424
FWT18	A/D Converter (SR9300 series) D/A Converter (SR9400 series) Relay (SR9510)	101-0421	101-0425
FWT18R	Relay (SR9500)	101-0422	101-0426

Before you can install the FWT you selected for your I/O card, you must remove the tabs from the connector on the I/O card. To do so, move the tab inwards as far as possible, as shown in Figure B-1. Then insert a screwdriver into the space below the tab on the side of the connector and gently nudge the tab up and out. If you are careful, the tab will remain intact to be saved and snapped back in place should you need to use a ribbon cable connector in the future.

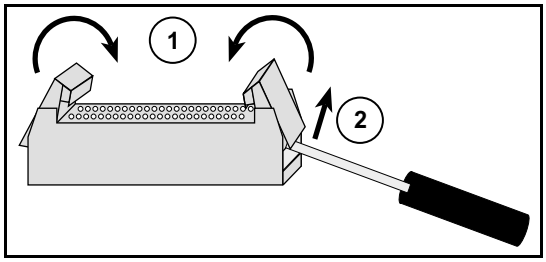


Figure B-1. Remove Tabs from Connector on I/O Card

Plug the FWT connector into the connector on the I/O card. Be sure to position the pluggable or screw connectors so that the edge of the FWT they are on faces outwards from the I/O card as shown in Figure B-2. Position the mylar insulator above the FWT as shown in Figure B-2 to protect the header pins on the printed circuit board, and secure the FWT using the two 4-40 × ¼ screws supplied.

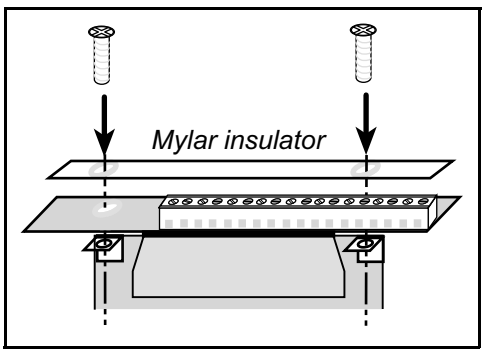


Figure B-2. Secure FWT to I/O Card

B.2 Dimensions

Figure B-3 shows the overall FWT dimensions.

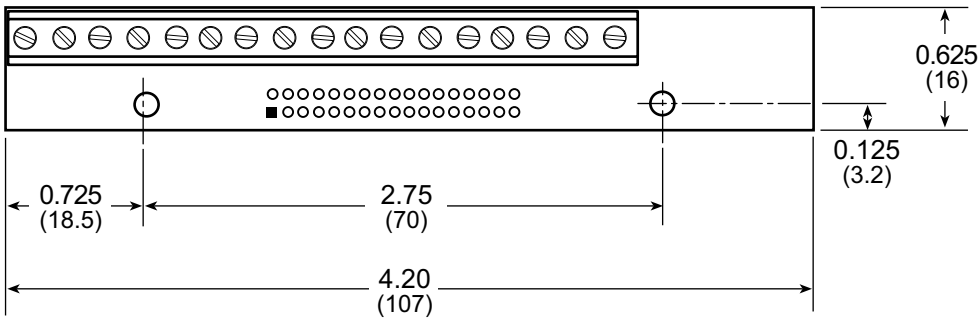


Figure B-3. FWT Dimensions

The actual appearance of the terminals may vary, depending on the number and type of terminals. The pinouts for the FWTs applicable to a particular I/O card are shown in the manuals for the individual I/O cards.

APPENDIX C. POWER MANAGEMENT

Appendix C provides information on the current requirements of the Smart Star I/O cards, the use and installation of a backup battery, and some background on power mangement.

C.1 Current Requirements

Remember to take the current draw of the various I/O cards into consideration when selecting the power supply for your Smart Star control system.

Table C-1 lists the typical current consumption for the CPU card and the I/O cards.

Table C-1. Current Consumption of I/O Cards Attached to Smart Star Backplane

I/O Cards	Current Consumption	
	+5 V Supply	+V_USER Supply
Digital I/O (SR9200 series)	65 mA	up to 200 mA/output*
A/D Converter (SR9300 series) D/A Converter (SR9400 series)	40 mA	35 mA
Relay (SR9500 series)	10 mA	75 mA
CPU card	150 mA	—

* Maximum current 2.0 A per I/O card, 7.0 A for Smart Star system

C.2 Batteries and External Battery Connections

A Z-World battery board with a 1000 mA·h lithium coin cell is sold separately to provide power to the real-time clock and SRAM when external power is removed from the Smart Star control system. This allows the CPU card to continue to keep track of time and preserves the SRAM memory contents while the power is off.

Figure C-1 shows the battery board circuit.

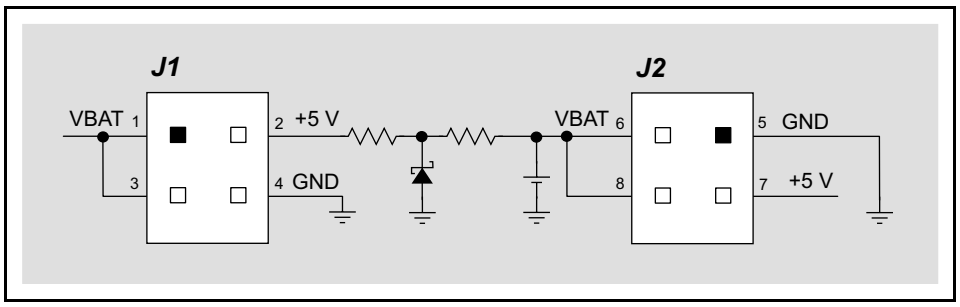


Figure C-1. Z-World Backup Battery Board Schematic

The drain on the battery is typically less than 20 µA when there is no external power applied. The battery can last more than 5 years:

$$\frac{1000\ \text{mA}\cdot\text{h}}{20\ \mu\text{A}} = 5.7\ \text{years}.$$

The drain on the battery is typically less than 4 µA when external power ***is*** applied. The battery can last for its full shelf life:

$$\frac{1000\ \text{mA}\cdot\text{h}}{4\ \mu\text{A}} = 28.5\ \text{years (shelf life = 10 years).}$$

Since the shelf life of the battery is 10 years, the battery can last for its full shelf life when external power is applied most of the time.

C.2.1 Battery Backup Circuit

The battery-backup circuit on the CPU card serves two purposes:

- It reduces the battery voltage to the real-time clock, thereby reducing the current consumed by the real-time clock and lengthening the battery life.
- It ensures that current can flow only ***out*** of the battery to prevent charging the battery.

Figure C-2 shows the battery backup circuitry on the CPU card.

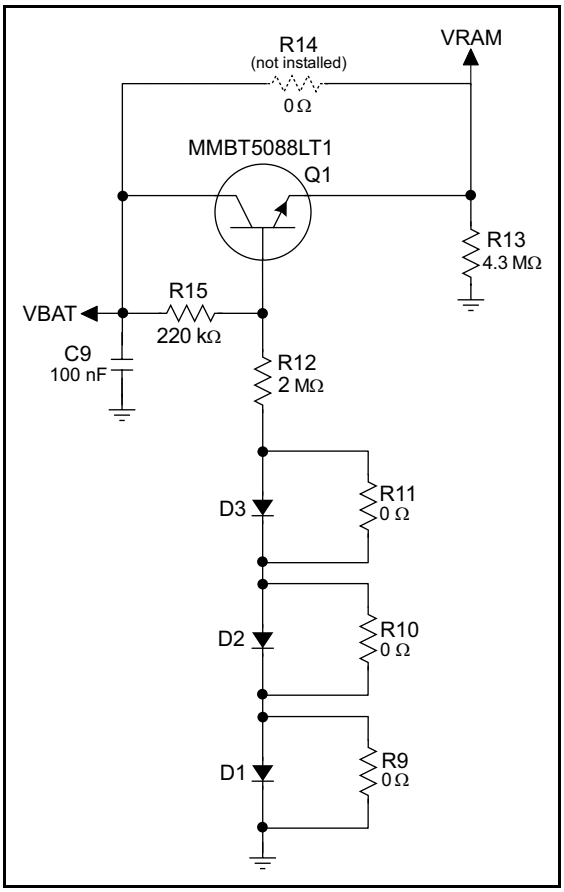


Figure C-2. CPU Card Battery Backup Circuit

Resistor R14, shown in Figure C-2, is typically not stuffed on the CPU card. VRAM and Vcc are nearly equal (<100 mV, typically 10 mV) when power is supplied to the CPU card.

Resistors R12 and R15 make up a voltage divider between the battery voltage and the temperature-compensation voltage at the anode of diode D3. This voltage divider biases the base of Q1 to about 0.9 × VBAT. V_{BE} on Q1 is about 0.55 V. Therefore, VRAM is about 0.9 × VBAT - 0.55 V, or about 2.15 V for a 3 V battery.

These voltages vary with temperature. VRAM varies the least because temperature-compensation resistors R9–R11 will offset the variation with temperature of Q1's V_{BE}. D1–D3 may be stuffed instead of the corresponding R9–R11 to provide more optimum temperature compensation.

Resistor R13 provides a minimum load to the regulator circuit.

C.2.2 Power to VRAM Switch

The VRAM switch, shown in Figure C-3, allows the battery backup to provide power when the external power goes off. The switch provides an isolation between +5 V and the battery when +5 V goes low. This prevents the +5 V line from draining the battery.

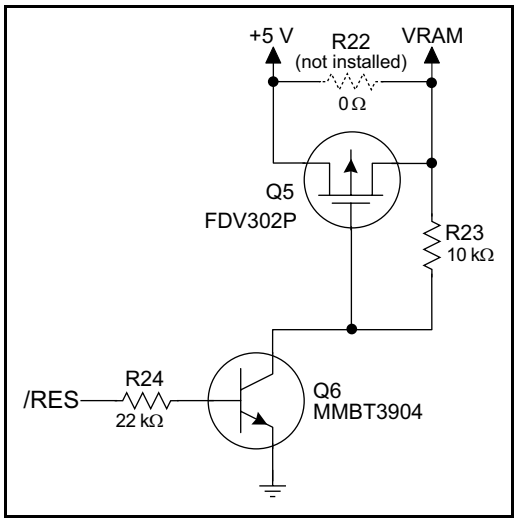


Figure C-3. VRAM Switch

Transistor Q5 is needed to provide a very small voltage drop between +5 V and VRAM (<100 mV, typically 10 mV) so that the processor lines powered by +5 V will not have a significantly different voltage than VRAM.

When the CPU card is ***not*** resetting (pin 2 on U3 is high), the /RES line will be high. This turns on Q6, causing its collector to go low. This turns on Q5, allowing VRAM to nearly equal +5 V.

When the CPU card ***is*** resetting, the /RES line will go low. This turns off Q5 and Q6, providing an isolation between +5 V and VRAM.

The battery backup circuit keeps VRAM from dropping below 2 V.

C.2.3 Reset Generator

The CPU card uses a reset generator, U3, to reset the Rabbit 2000 microprocessor when the voltage drops below the voltage necessary for reliable operation. The reset occurs between 4.50 V and 4.75 V, typically 4.63 V.

C.2.4 Installing the Backup Battery Board

The pluggable backup battery board is easy to install. When installing the backup battery board for the first time, do so before attaching the CPU card to the backplane (see Section 2.1).

1. Align the backup battery board over the outline on the CPU card as shown in Figure C-4, and plug it in. Be careful to align the connectors and the spacer that is attached to the backup battery board.
2. Use the 4-40 screws included with the backup battery board to secure the backup battery board to the CPU card. Use one screw at the front of the backup battery board, and the other screw goes in from the other side of the CPU card.

The CPU card is now ready to be installed on the backplane.

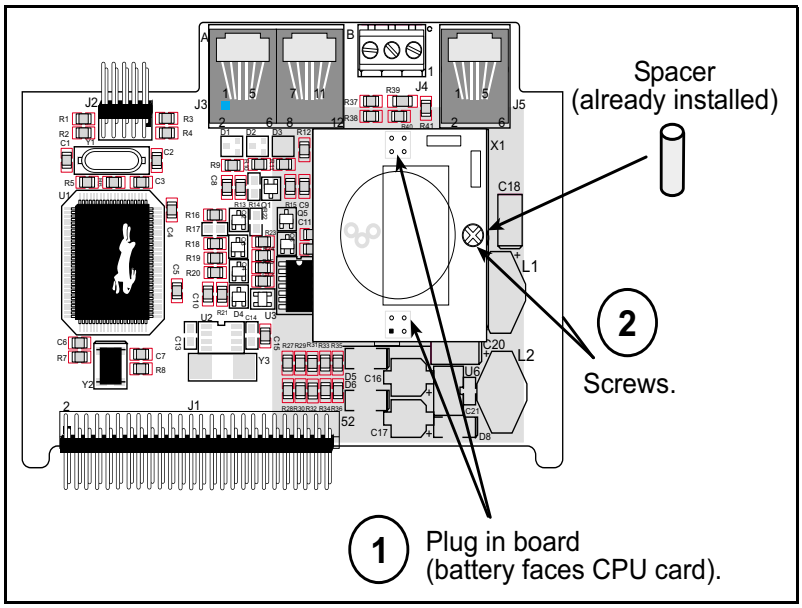


Figure C-4. Installing Backup Battery Board

To replace the backup battery board, remove the CPU card from the backplane, then remove the screw and unplug the old battery board. Align the replacement battery board over the outline, and plug it in. Be careful to align the connectors. Replace the screw.

Before replacing the backup battery board, make sure that the CPU card is receiving power if it is critical that data in RAM are not lost while the CPU card is not installed on the backplane. Connect +5 V to pin 20 of the backplane interface header (J1) and ground pin 1, pin 26, or pin 52 of the backplane interface header (J1) on the CPU card.

Figure C-5 shows the pins on the backplane interface header (J1) where the temporary +5 V power supply connections can be made.

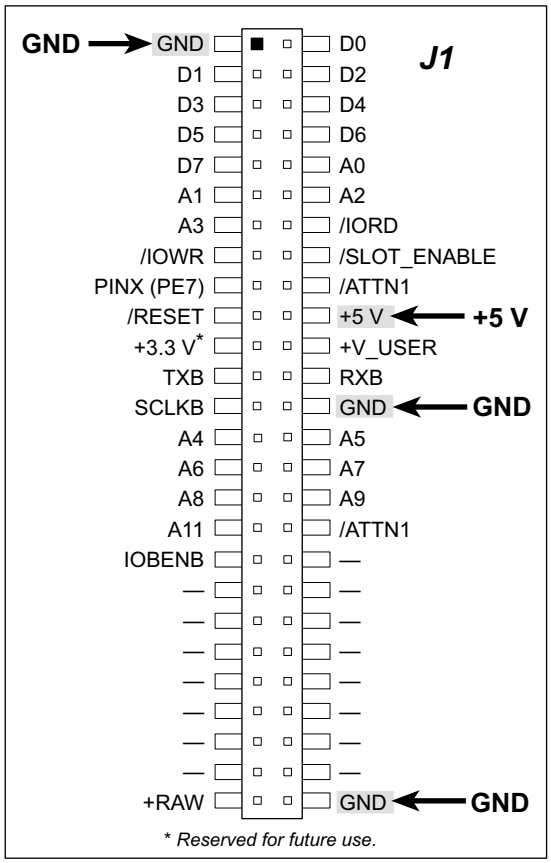


Figure C-5. Temporary +5 V Power Supply Connections

To avoid any risk of explosion or fire, do ***not*** attempt to recharge the old battery, and do ***not*** dispose of it in the regular trash. You may either return the old backup battery board to Z-World for recycling or send the battery yourself to an approved recycling facility.

C.3 Chip Select Circuit

Figure C-6 shows a schematic of the chip select circuit for the RAM.

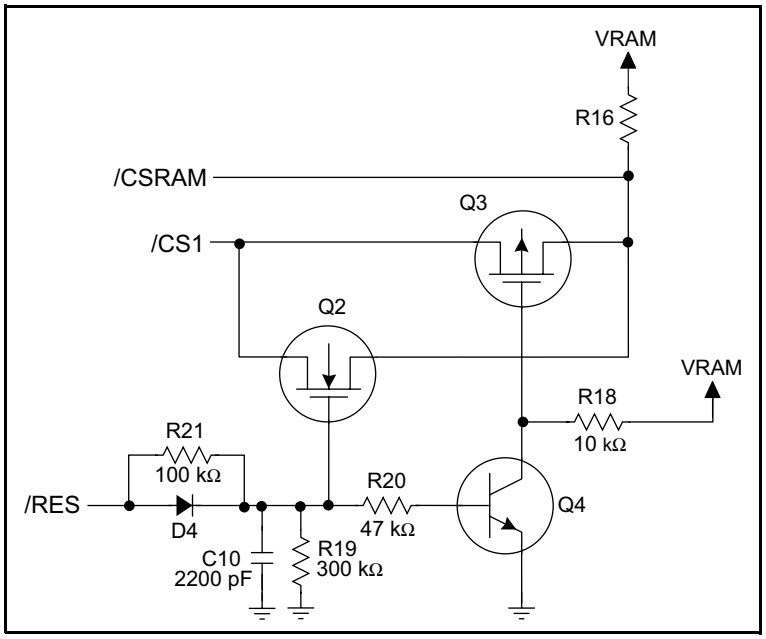


Figure C-6. Chip Select Circuit

The current drain on the battery in a battery-backed circuit must be kept at a minimum. When the CPU card is not powered, the battery keeps the SRAM memory contents and the real-time clock (RTC) going. The SRAM has a powerdown mode that greatly reduces power consumption. This powerdown mode is activated by raising the chip select (CS) signal line. Normally the SRAM requires +5 V to operate. However, only 2 V is required for data retention in powerdown mode. Thus, when power is removed from the circuit, the battery voltage needs to be provided to both the SRAM power pin and to the CS signal line. The CS control circuit accomplishes this task for the CS signal line.

In a powered-up condition, the CS control circuit must allow the processor's chip select signal /CS1 to control the SRAM's CS signal /CSRAM. So, with power applied, /CSRAM must be the same signal as /CS1, and with power removed, /CSRAM must be held high (but only needs to be battery voltage high). Q2 and Q3 are MOSFET transistors with opposing polarity. They are both turned on when power is applied to the circuit. They allow the CS signal to pass from the processor to the SRAM so that the processor can periodically access the SRAM. When power is removed from the circuit, the transistors will turn off and isolate /CSRAM from the processor. The isolated /CSRAM line has a 100 kΩ pullup resistor to VRAM (R16). This pullup resistor keeps /CSRAM at the VRAM voltage level (which under no power condition is the backup battery's regulated voltage at a little more than 2 V).

Transistors Q2 and Q3 are of opposite polarity so that a rail-to-rail voltage can be passed. When the /CS1 voltage is low, Q2 will conduct. When the /CS1 voltage is high, Q3 will

conduct. It takes time for the transistors to turn on, creating a propagation delay. This delay is typically very small, about 10 ns to 15 ns.

The signal that turns the transistors on is a high on the processor's reset line, /RES. When the CPU card is not in reset, the reset line will be high, turning on n-channel Q2 and Q4. Q4 is a simple inverter needed to turn on Q3, a p-channel MOSFET. When a reset occurs, the /RES line will go low. This will cause C10 to discharge through R19 and R21. This small delay (about 160 µs) ensures that there is adequate time for the processor to write any last byte pending to the SRAM before the processor puts itself into a reset state. When coming out of reset, CS will be enabled very quickly because D4 conducts to charge capacitor C10.

APPENDIX D. PROGRAMMING CABLE

Appendix D provides additional theoretical information for the Rabbit 2000™ microprocessor when using the **DIAG** and **PROG** connectors on the programming cable with the CPU card in the Smart Star system. The **PROG** connector is used only when the programming cable is attached to the proramming connector (header J2) on the CPU card while a new application is being developed. Otherwise, the **DIAG** connector on the programming cable allows the programming cable to be used as an RS-232 to CMOS level converter for serial communication, which is appropriate for monitoring or debugging the Smart Star system while it is running.

The programming port, which is shown in Figure D-1, can serve as a convenient communications port for field setup or other occasional communication need (for example, as a diagnostic port). There are several ways that the port can be automatically integrated into software. If the port is simply to perform a setup function, that is, write setup information to flash memory, then the controller can be reset through the programming port and a cold boot performed to start execution of a special program dedicated to this functionality.

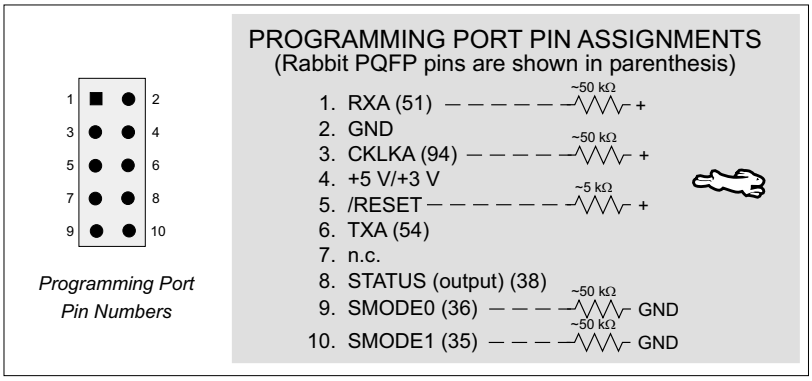


Figure D-1. Programming Port Pin Assignments

When the **PROG** connector is used, the /RESET line can be asserted by manipulating DTR and the STATUS line can be read as DSR on the serial port. The target can be restarted by pulsing reset and then, after a short delay, sending a special character string at 2400 bps. To simply restart the BIOS, the string 80h, 24h, 80h can be sent. When the BIOS is started, it can tell whether the programming cable is connected because the SMODE1 and SMODE0 pins are sensed as being high. This will cause the Rabbit 2000 to enter the bootstrap mode. The Dynamic C programming mode then can have an escape message that will enable the diagnostic serial port function.

Alternatively, the **DIAG** connector can be used to connect the programming port. The /RESET line and the SMODE1 and SMODE0 pins are not connected to this connector. The programming port is then enabled as a diagnostic port by polling the port periodically to see if communication needs to begin or to enable the port and wait for interrupts. The pull-up resistors on RXA and CLKA prevent spurious data reception that might take place if the pins floated.

If the clocked serial mode is used, the serial port can be driven by having two toggling lines that can be driven and one line that can be sensed. This allows a conversation with a device that does not have an asynchronous serial port but that has two output signal lines and one input signal line.

The line TXA (also called PC6) is zero after reset if the cold-boot mode is not enabled. A possible way to detect the presence of a cable on the programming port is for the cable to connect TXA to one of the SMODE pins and then test for the connection by raising PC6 and reading the SMODE pin after the cold-boot mode has been disabled.

APPENDIX E.
SMART STAR SLOT ADDRESS LAYOUT

Appendix E provides information about the register addresses for the various I/O card slots on the backplane. The information in this appendix will be of interest to more advanced users.

The slots on the Smart Star backplane are accessed as external registers via the Rabbit 2000's assembly **IOE** prefix or via standard Rabbit BIOS functions. More convenient functions specific to the Smart Star control system have been written to provide more flexibility; for example, there is now a provision for the automatic update of shadow registers for each slot and for each register.

The Smart Star design routes four address bits to each slot, providing 16 register addresses for each slot. These bits are passed through as bits 0–3 of the register address. The slot number itself is assigned to bits 6–8 of the address. In addition, the backplane design requires that bits 13 and 14 be high and that bit 9 be low. The simplest way to enforce this is to use a base address of 0x6000. Table E-1 provides the address layout for accessing the Smart Star slots, where S*n* is the binary representation of the slot number (0–6), R*n* is the binary representation of the register numbers (0–15), and *X* means the value does not matter.

Table E-1. Smart Star External Register Address Bitmap

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	1	0	*X*	*X*	0	S2	S1	S0	*X*	*X*	R3	R2	R1	R0

This bit mapping of the external register address provides the register addresses for each slot as listed in Table E-2.

Table E-2. Slot External Register Addresses

Slot Number	Address Range
0	0x6000–0x600F
1	0x6040–0x604F
2	0x6080–0x608F
3	0x60C0–0x60CF
4	0x6100–0x610F
5	0x6140–0x614F
6	0x6180–0x618F

INDEX

T

SCHEMATICS

090-0093 CPU Card (SR9100) Schematic

090-0094 Backplane (SR9000) Schematic

090-0103 FWT27 Schematic

090-0085 Programming Cable Schematic

NOTES: UNLESS OTHERWISE SPECIFIED;

1. ALL RESISTOR VALUES ARE IN OHMS, 1/10W, 5%
2. ALL CAPACITORS ARE 50VDC OR HIGHER.
3. THE ORIGINATION SOURCE OF A VOLTAGE IS REPRESENTED BY ($_{VCC}^{\blacktriangle}$), AND ALL REFERENCES TO THAT VOLTAGE ARE REPRESENTED BY ($_{VCC}$).

△4 OUTLINED CIRCUIT NOT STUFFED ON SR9100 MODEL.

5. COMPONENT VALUES SHOWN WITH AN ASTERISK (*) FOLLOWING THE VALUE, ARE NOT STUFFED ON SR9100 MODEL.

REVISION HISTORY			REVISION APPROVAL			
REV	ECO	DESCRIPTION	PROJECT ENGINEER	APPROVAL DATE	DOCUMENT CONTROL	APPROVAL DATE
A	----	NOT RELEASE @ A – TRACKS A/W @ REV–A	RAF	NA	NA	NA
B	E11217	INITIAL RELEASE – TRACKS A/W @ REV–B, ADDED R68				

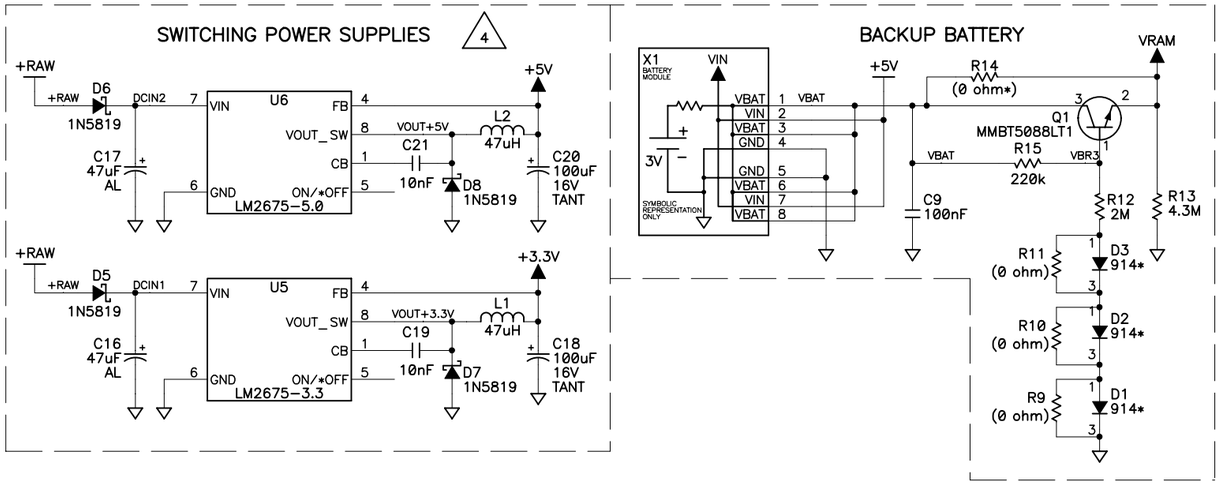
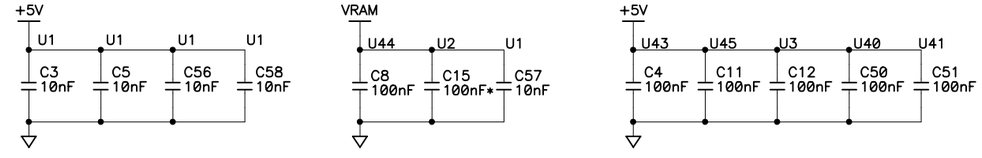
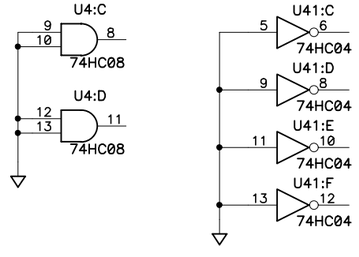


TABLE A

REF DES	DEVICE	DEVICE VOLTAGE INFORMATION					DEVICE: FILTER CAP REF DES(s)
		GND	+5V	+3.3V	VRAM	NO CONNECTS	
U1	RABBIT 2000	2,27,39, 52,77,89	3,28,53,78,92		42		C3, 5 56, 58 PIN–42 – C57
U2	HA7210	4			1		C15
U3	ETC811L	1	4				C12
U4	74HC08	7	14				
U5	LM2675–3.3					2,3	
U6	LM2675–5.0					2,3	
U40	SP483E	5	8				C50
U41	74HC04	7	14				C51
U42	74HC125	7	14				
U43	232A	15	16				C4
U44	SRAM 512K X 8	16			32		C8
	SRAM 32K X 8	14			28		
U45	FLASH	24	8				C11
U46	FLASH	24	8				

Decoupling Capacitors





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DRAWN BY: (INITIAL RELEASE) REP	21JUN99
REVISED BY: KAH	26SEP00
APPROVALS: INITIAL RELEASE	
PROJECT ENGINEER:	
ENGINEERING MANAGER:	
SIGNATURES	DATE

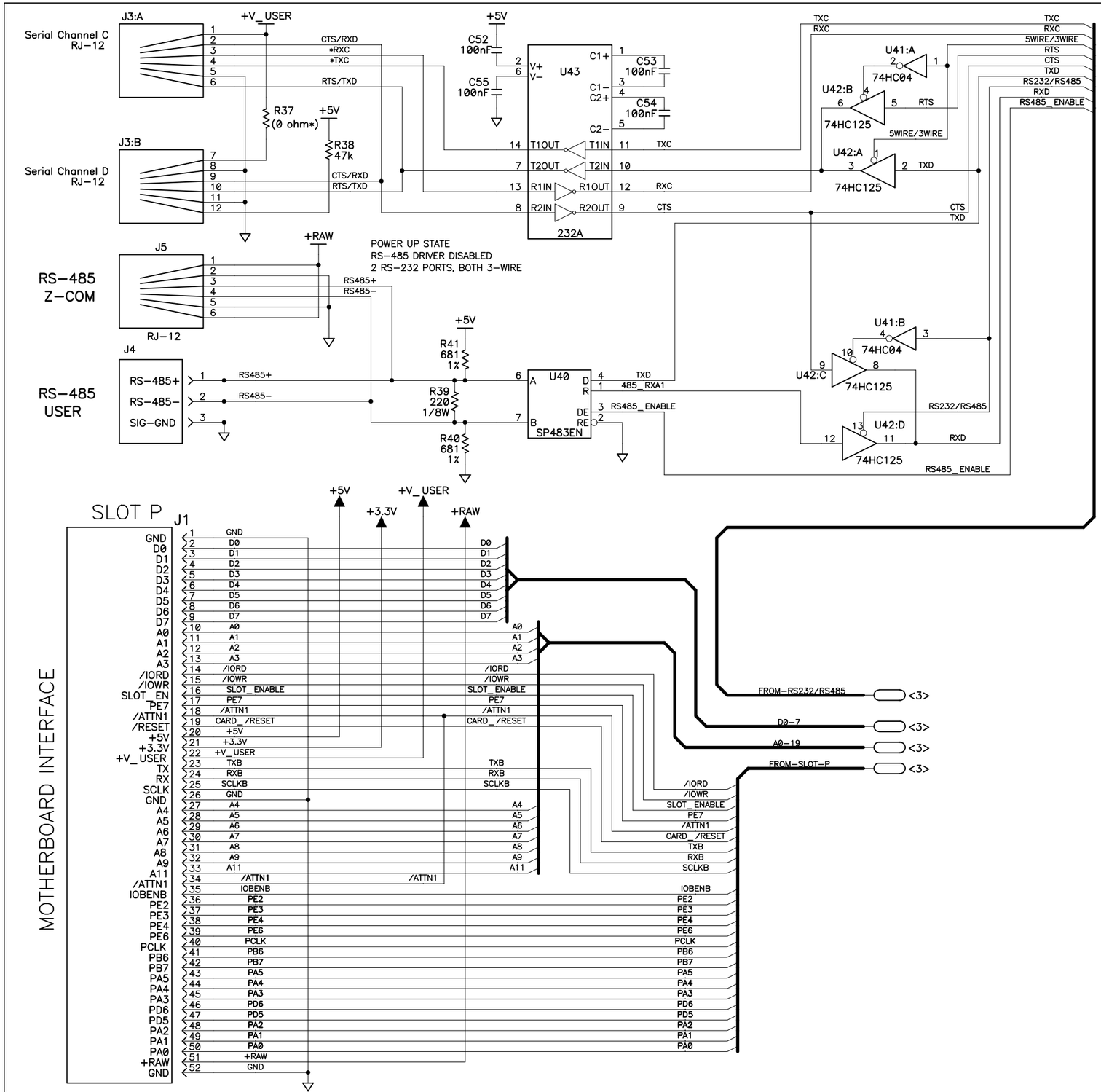
TITLE

SCHEMATIC DIAGRAM SR9100 SERIES PROCESSOR BOARD

Z-WORLD
2900 SPAFFORD ST.
DAVIS, CA 95616
530 - 757 - 4616

SIZE **B** | DWG NO. 090–0093

SCALE NONE | RELEASE DATE | SHEET 1 OF 3



26SEP00

SIZE	DWG NO.		
B	090-0093		
SCALE NONE	REV LTR B	SHEET 2 OF 3	

ONLY ONE DEVICE INSTALLED

U44: OPTIONAL 512K, 256K, 128K, OR 32K SRAM

D0-7

A0-19

TO-SLOT-P

TO-RS232/RS485

U1

RABBIT 2000

U44_ALT_PINOUT

SRAM 32K X 8

SRAM SELECT*

(0 ohm) Resistor Jumper

JP1

128 kB

512 kB

VRAM

SRAM_SEL

U44

SRAM

U46

U45

FLASH

FLASH TYPE

512K X 8	256K X 8	128K X 8
PIN ID	A17	A17	NC
PIN ID	A18	NC/•RST	NC

SRAM TYPE

512K X 8	128K X 8
PIN ID	A17	CS2
PIN ID	A18	NC

Reset Generator

U3

ETC811L

U4:B

74HC08

Alternate RTC timebase

U2

HA7210

32.768kHz

9.216MHz

FLASH 2 SELECT

JP2

1-2 128K/256K FLASH

2-3 512K FLASH

FLASH 1 SELECT

JP3

1-2 128K/256K FLASH

2-3 512K FLASH

CS Control

Q5 FDV302P

Q3 FDV302P

Q2 2N7002

Q6 MMBT3904

Q4 MMBT3904

914

J2

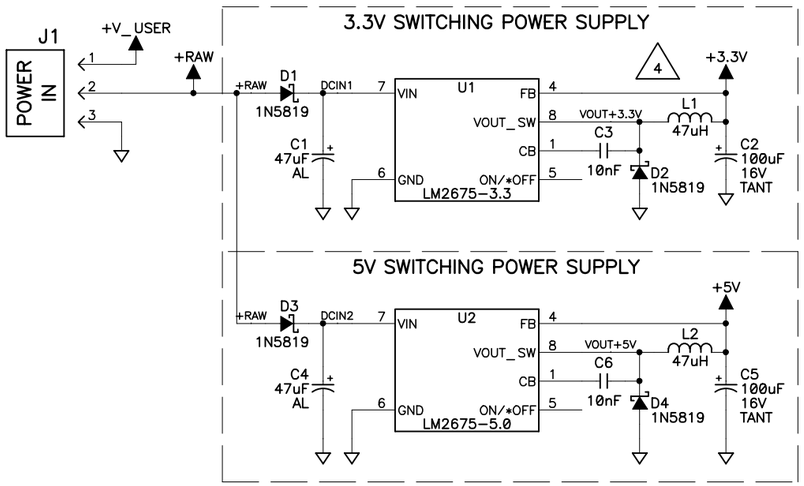
RABBIT PROG PORT

1	RXA
2	GND
3	CLKA
4	VCC
5	/RESET
6	TXA
7	
8	RXA
9	SMODE0
10	SMODE1

26SEP00

SIZE	DWG NO.	
B	090-0093	
SCALE NONE	REV LTR B	SHEET 3 OF 3

REVISION HISTORY			REVISION APPROVAL			
REV	ECO	DESCRIPTION	PROJECT ENGINEER	APPROVAL DATE	DOCUMENT CONTROL	APPROVAL DATE
A	E11217	INITIAL RELEASE				



Decoupling Capacitors

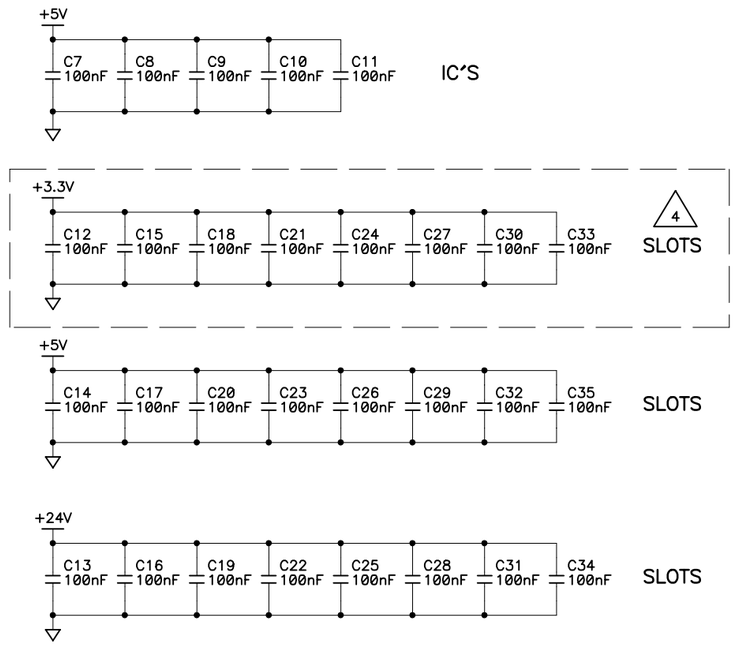


TABLE A

REF DES	DEVICE	DEVICE VOLTAGE INFORMATION					DEVICE: FILTER CAP REF DES(s)
		GND	+5V	+3.3V	VRAM	NO CONNECTS	
U1	LM2675-3.3					2,3	
U2	LM2675-5.0					2,3	
U3	74HCT245	10	20				
U4	74HCT245	10	20				
U5	74VHC138	8	16				
U6	74HCT245	10	20				
U7	74HCT245	10	20				

NOTES: UNLESS OTHERWISE SPECIFIED;
1. ALL RESISTOR VALUES ARE IN OHMS, 1/10W, 5%
2. ALL CAPACITORS ARE 50VDC OR HIGHER.
3. THE ORIGINATION SOURCE OF A VOLTAGE IS REPRESENTED BY ($_{VCC}^{\blacktriangle}$), AND ALL REFERENCES TO THAT VOLTAGE ARE REPRESENTED BY ($_{VCC}^{\blacktriangledown}$).

4 OUTLINED CIRCUIT NOT INSTALLED ON SR9000 MODEL.

APPEND THE FOLLOWING DOCUMENTS WHEN CHANGING THIS DOCUMENT:	

DRAWING CONTENT:	
DRAWN BY: (INITIAL RELEASE) REP	21JUN99
REVISED BY: KAH	26SEP00
APPROVALS: INITIAL RELEASE	
PROJECT ENGINEER:	
ENGINEERING MANAGER:	
SIGNATURES	DATE

TITLE
SCHEMATIC DIAGRAM SR9000 SERIES MOTHERBOARD

Z-WORLD
2900 SPAFFORD ST.
DAVIS, CA 95616
530 - 757 - 4616

SIZE B | DWG NO. 090-0094

SCALE NONE | RELEASE DATE | SHEET 1 OF 3

PROCESSOR SLOT

MOTHERBOARD INTERFACE

J2

GND	1	GND	
D0	2	D0	D0
D1	3	D1	D1
D2	4	D2	D2
D3	5	D3	D3
D4	6	D4	D4
D5	7	D5	D5
D6	8	D6	D6
D7	9	D7	D7
A0	10	A0	A0
A1	11	A1	A1
A2	12	A2	A2
A3	13	A3	A3
/IORD	14	/IORD	
/IOWR	15	/IOWR	
SLOT_EN	16	SLOT_ENABLE	
PE7	17	PE7	
/ATTN1	18	/ATTN1	
/RESET	19	CARD_/RESET	
+5V	20	+5V	
+3.3V	21	+3.3V	
+V_USER	22	+V_USER	
TX	23	TXB	
RX	24	RXB	
SCLK	25	SCLKB	
GND	26	GND	
A4	27	A4	A4
A5	28	A5	A5
A6	29	A6	A6
A7	30	A7	A7
A8	31	A8	A8
A9	32	A9	A9
A11	33	A11	A11
/ATTN1	34	/ATTN1	
IOBENB	35	IOBENB	
PE2	36	PE2	
PE3	37	PE3	
PE4	38	PE4	
PE6	39	PE6	
PCLK	40	PCLK	
PB6	41	PB6	
PB7	42	PB7	
PA5	43	PA5	
PA4	44	PA4	
PA3	45	PA3	
PD6	46	PD6	
PD5	47	PD5	
PA2	48	PA2	
PA1	49	PA1	
PA0	50	PA0	
+RAW	51	+RAW	
GND	52	GND	

+5V, +3.3V, +V_USER, +RAW

U3 74HCT245A

D7	2	A0	B0	18	BUF_D7
D6	3	A1	B1	17	BUF_D6
D5	4	A2	B2	16	BUF_D5
D4	5	A3	B3	15	BUF_D4
D3	6	A4	B4	14	BUF_D3
D2	7	A5	B5	13	BUF_D2
D1	8	A6	B6	12	BUF_D1
D0	9	A7	B7	11	BUF_D0
IOBENB	19	OE			
/IORD	1	T/*R			

BUF_D7 … BUF_D0 — 47k pull-ups R1–R8 to +5V

U5 74VHC138

A6	1	A0	O0	15	CS_SLOT0
A7	2	A1	O1	14	CS_SLOT1
A8	3	A2	O2	13	CS_SLOT2
			O3	12	CS_SLOT3
			O4	11	CS_SLOT4
			O5	10	CS_SLOT5
			O6	9	CS_SLOT6
			O7	7	CS_SLOT7
+5V	6	E3			
SLOT_ENABLE	4	E1			
A9	5	E2			

R9 47k +5V SLOT_ENABLE

U4 74HCT245A

A7	2	A0	B0	18	BUF_A7
A6	3	A1	B1	17	BUF_A6
A5	4	A2	B2	16	BUF_A5
A4	5	A3	B3	15	BUF_A4
A3	6	A4	B4	14	BUF_A3
A2	7	A5	B5	13	BUF_A2
A1	8	A6	B6	12	BUF_A1
A0	9	A7	B7	11	BUF_A0
	19	OE			
	1	T/*R			

U6 74HCT245A

A11	2	A0	B0	18	BUF_A11
A8	3	A1	B1	17	BUF_A8
	4	A2	B2	16	
	5	A3	B3	15	
SCLKB	6	A4	B4	14	SLT4-7_SCLK
TXB	7	A5	B5	13	SLT4-7_TX
SCLKB	8	A6	B6	12	SLT0-3_SCLK
TXB	9	A7	B7	11	SLT0-3_TX
+5V	19	OE			
	1	T/*R			

SLT4-7_SCLK, SLT4-7_TX, SLT0-3_SCLK, SLT0-3_TX

PE7, /ATTN1, CARD_/RESET, RXB

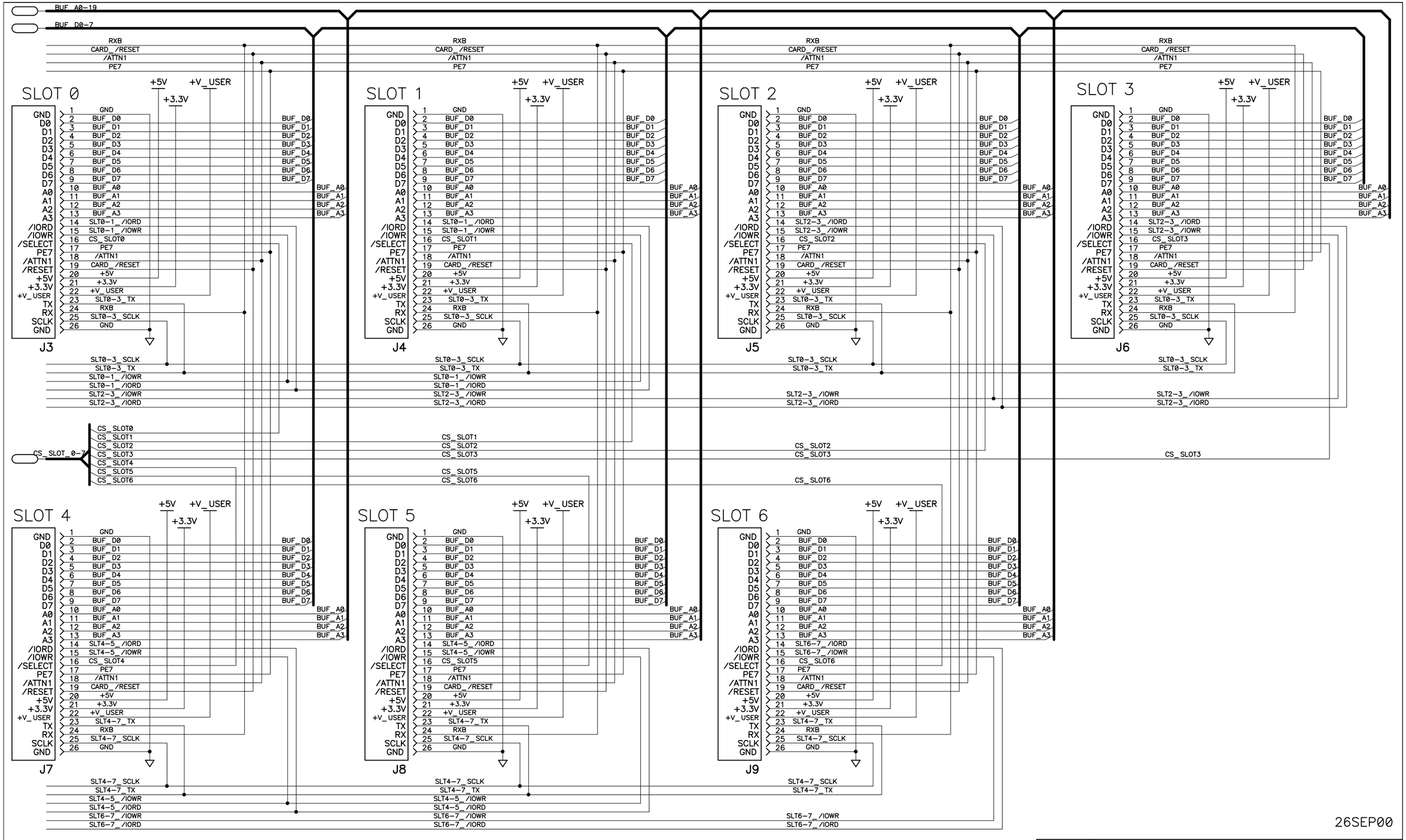
U7 74HCT245A

/IOWR	2	A0	B0	18	SLT6-7_/IOWR
/IORD	3	A1	B1	17	SLT6-7_/IORD
/IOWR	4	A2	B2	16	SLT4-5_/IOWR
/IORD	5	A3	B3	15	SLT4-5_/IORD
/IOWR	6	A4	B4	14	SLT2-3_/IOWR
/IORD	7	A5	B5	13	SLT2-3_/IORD
/IOWR	8	A6	B6	12	SLT0-1_/IOWR
/IORD	9	A7	B7	11	SLT0-1_/IORD
+5V	19	OE			
	1	T/*R			

SLT6-7_/IOWR, SLT6-7_/IORD, SLT4-5_/IOWR, SLT4-5_/IORD, SLT2-3_/IOWR, SLT2-3_/IORD, SLT0-1_/IOWR, SLT0-1_/IORD

26SEP00

SIZE	DWG NO.	
B	090-0094	
SCALE NONE	REV LTR A	SHEET 2 OF 3



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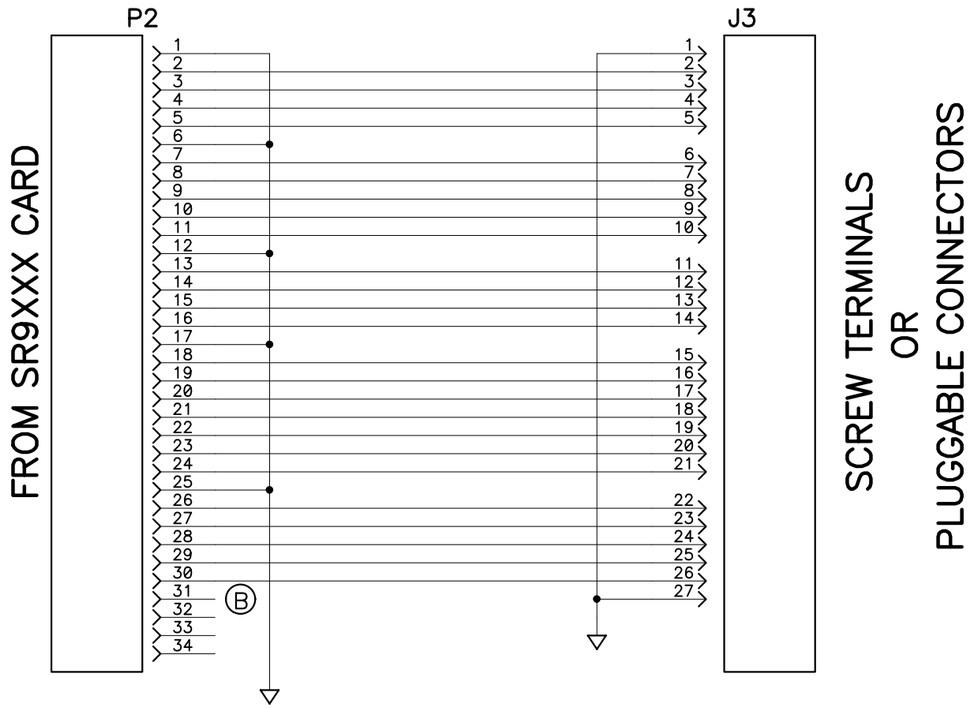
SIZE	DWG NO.	
B	090-0094	
SCALE NONE	REV LTR A	SHEET 3 OF 3

REVISION HISTORY			REVISION APPROVAL			
REV	ECO	DESCRIPTION	PROJECT ENGINEER	APPROVAL DATE	DOCUMENT CONTROL	APPROVAL DATE
A	E11217	INITIAL RELEASE				
B	E11326	DISCONNECT PIN 31 FROM GND	DM	22DEC00		



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DRAWN BY: (INITIAL RELEASE) KEITH HOEK	02DEC99
REVISED BY: ERIC PEAK	22DEC00
APPROVALS: INITIAL RELEASE	
PROJECT ENGINEER:	
ENGINEERING MANAGER:	
SIGNATURES	**DATE**

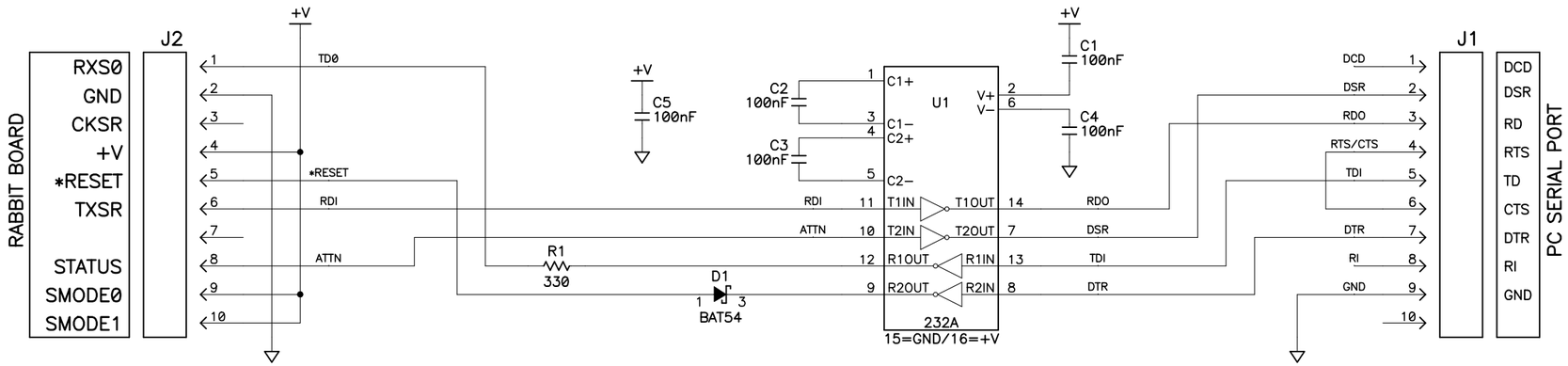
TITLE SCHEMATIC DIAGRAM
SR9XXX SERIES
27 POSITION
FIELD WIRING TERMINAL

Z-WORLD
2900 SPAFFORD ST.
DAVIS, CA 95616
530 - 757 - 4616

SIZE **A** DWG NO. 090–0103

SCALE **NONE** RELEASE DATE SHEET 1 OF 1

REVISION HISTORY			REVISION APPROVAL			
REV	ECO	DESCRIPTION	PROJECT ENGINEER	APPROVAL DATE	DOCUMENT CONTROL	APPROVAL DATE
X1	----	Engineering Prototype Release A/W Rev-A	RH	----	----	----
A	E10680	INITIAL RELEASE OF SCHEMATIC, PCB A/W @ REV-B				



NOTES: UNLESS OTHERWISE SPECIFIED;

1. ALL RESISTOR VALUES ARE IN OHMS, 1/10W, 5%
2. ALL CAPACITORS ARE 50VDC OR HIGHER.
3. THE ORIGINATION SOURCE OF A VOLTAGE IS REPRESENTED BY (V_{CC}), AND ALL REFERENCES TO THAT VOLTAGE ARE REPRESENTED BY (V_{CC}).

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		DRAWN BY: (INITIAL RELEASE) KAH	15MAR99	SCHEMATIC DIAGRAM RABBIT SIB	Z-WORLD 2900 SPAFFORD ST. DAVIS, CA 95616 530 - 757 - 4616
		REVISED BY: KAH	13AUG99		
		APPROVALS: INITIAL RELEASE			
		PROJECT ENGINEER:		SIZE B	DWG NO. 090-0085
		ENGINEERING MANAGER:			
		SIGNATURES	DATE	SCALE NONE	RELEASE DATE / SHEET 1 OF 1