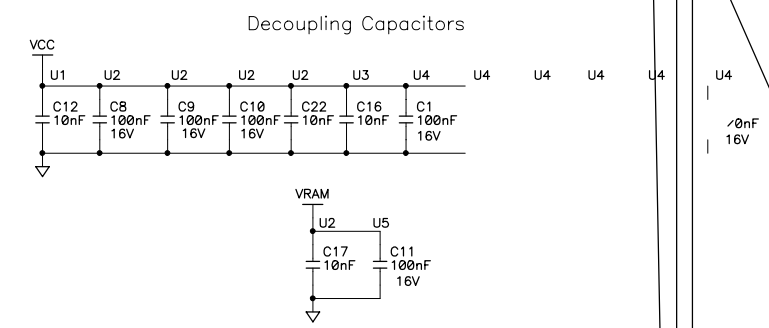


TABLE A

REF DES	DEVICE	DEVICE VOLTAGE INFORMATION				DEVICE: FILTER CAP REF DES(s)
		GND	VCC	VRAM	NO CONNECTS	
U1	ETC811L					C12
U2	RABBIT 2000	2,27,39 52,77,89	3,28,53, 78,92	42		C8, C14, C9
U3	FLASH	24	8			
U4	RTL8019AS	14,28,44 52,83,86	6,17,47 57,70,89			
U5	SRAM 128K X 8	24		8		


STUFFING TABLE

	CIRCUIT	PART	RCM2200
POWER TO VRAM SWITCH	WITH BATTERY BACKUP CIRCUITRY	R33	NOT INSTALLED
	CS CONTROL SWITCH	R27	NOT INSTALLED
FLASH	MAIN	U3	256K FLASH
	FLASH SELECT	JP1	ZERO ohm ACROSS PINS 1-2
	FLASH TYPE	JP2	ZERO ohm ACROSS PINS 1-2
ETHERNET	RJ-45 CONNECTOR WITH BUILT IN MAGNETICS	J3	NOT INSTALLED
		J2	INSTALLED



- NOTES: UNLESS OTHERWISE SPECIFIED;
1. ALL RESISTOR VALUES ARE IN OHMS, 1/16W, 5%
  2. ALL CAPACITORS ARE 50VDC OR HIGHER.
  3. THE ORIGIN SOURCE OF A VOLTAGE IS REPRESENTED BY ( VCC ), AND ALL REFERENCES TO THAT VOLTAGE ARE REPRESENTED BY ( VCC ).
  4. R27, R33, & J3 not normally stuffed.
  5. COMPONENT VALUES SHOWN WITH AN ASTERISK (\*) FOLLOWING THE VALUE, MAY HAVE DIFFERENT VALUES, OR MAY NOT BE STUFFED DEPENDING ON MODEL. SEE STUFFING CHART FOR CLARIFICATION..
  6. JP1 AND JP2 ARE JUMPERED POSITION 1 TO POSITION 2 BY FACTORY DEFAULT.

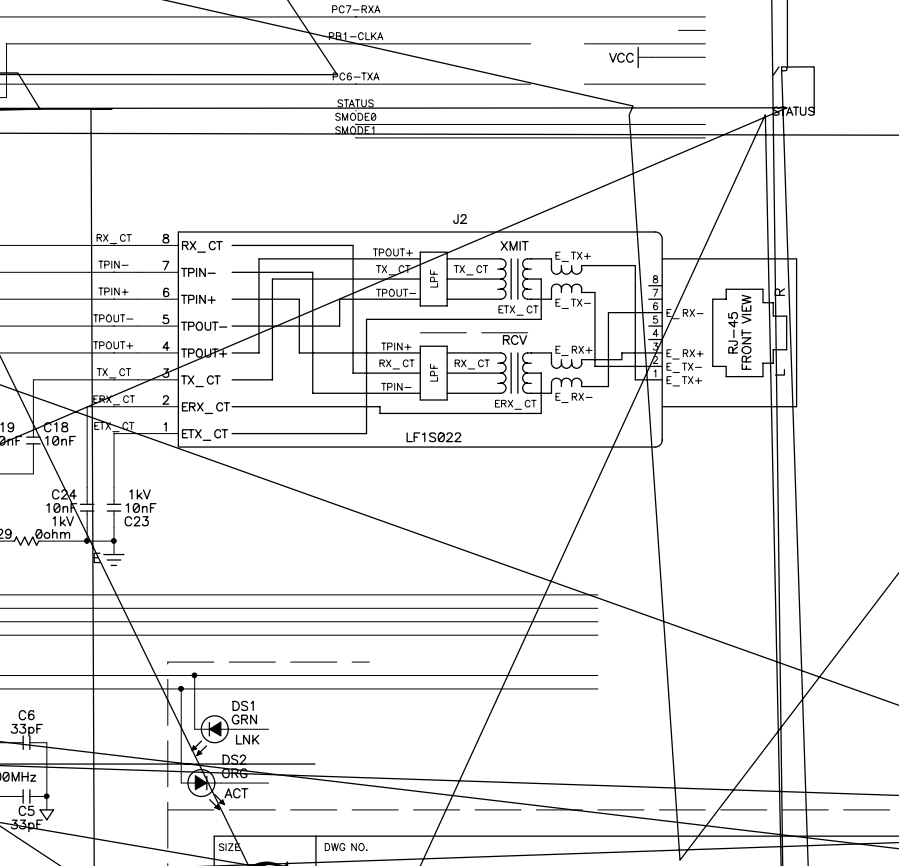
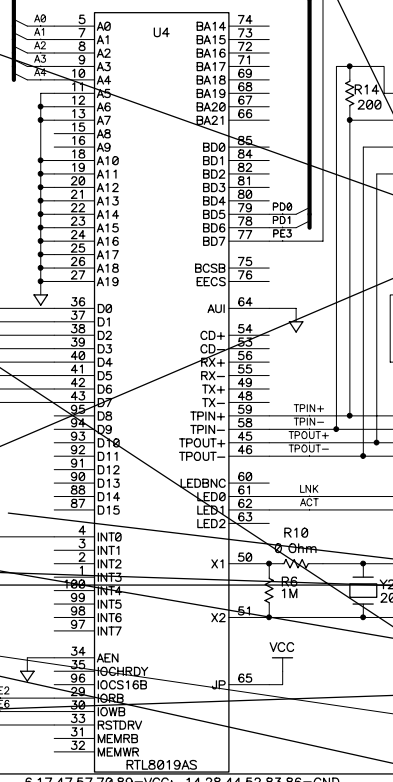
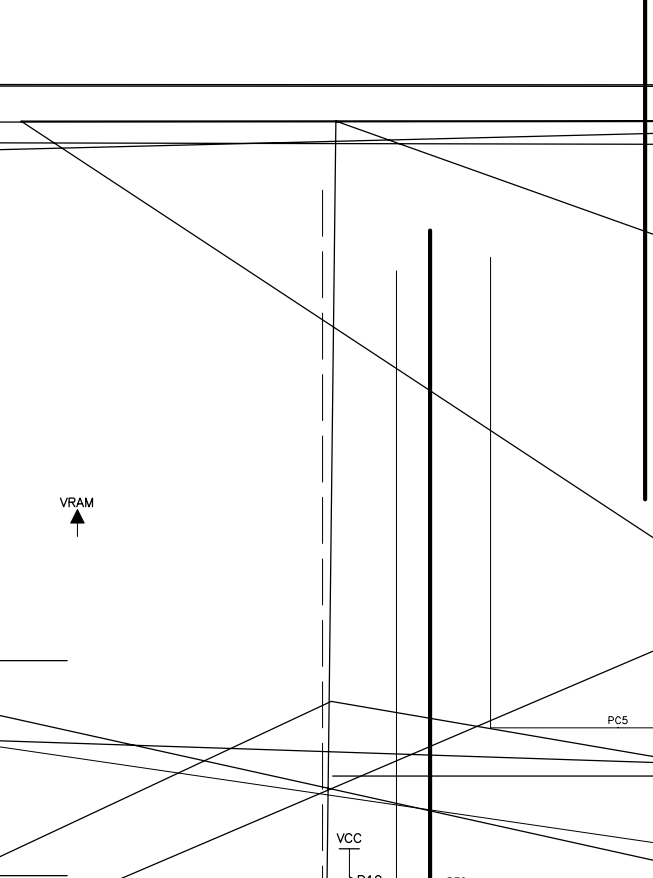
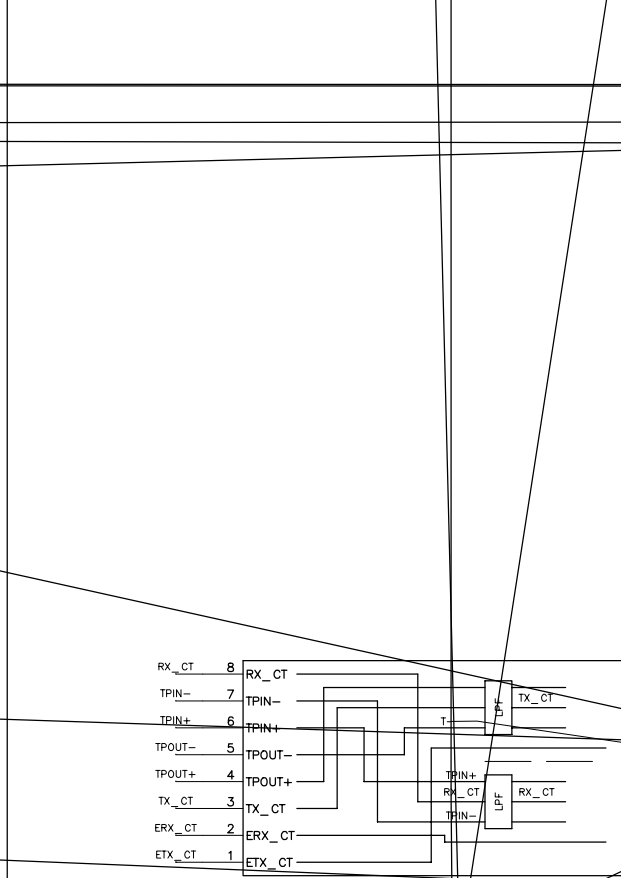
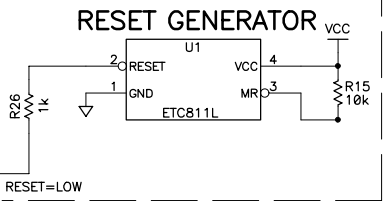
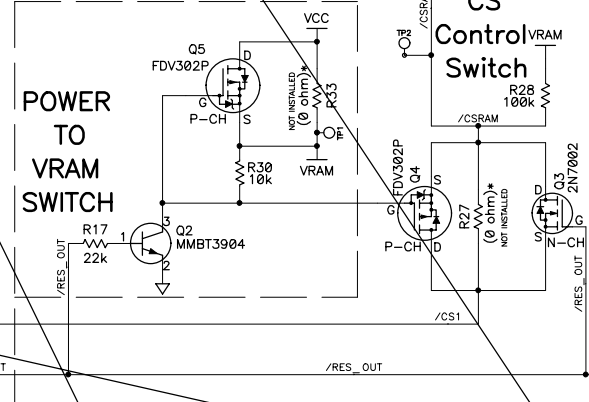
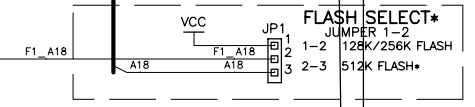
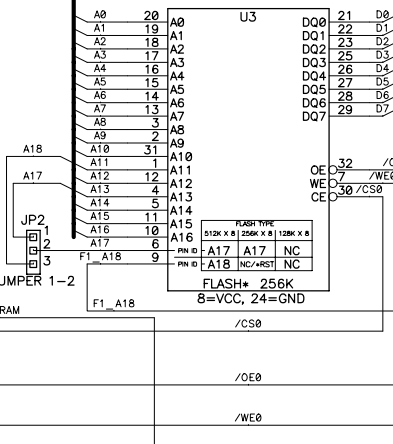
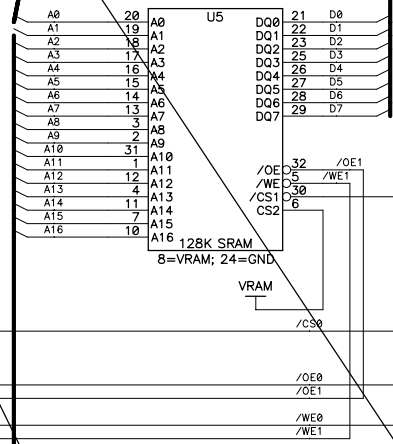
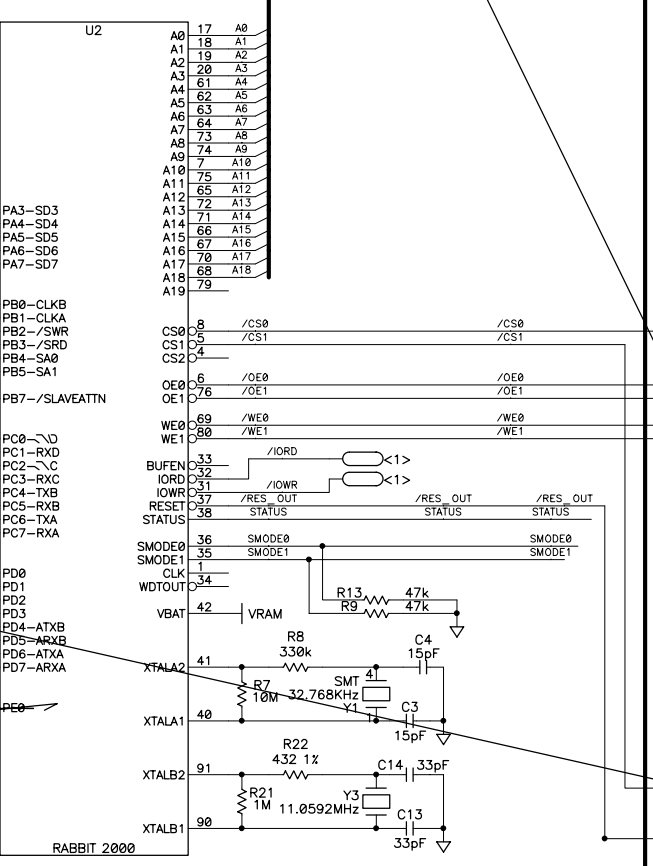
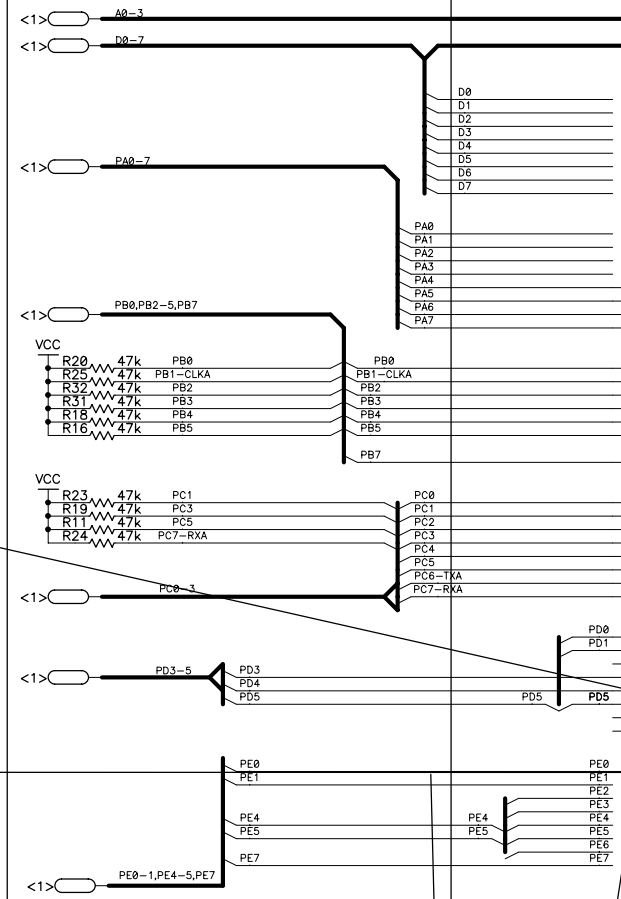
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DRAWN BY: (INITIAL RELEASE) RJH		3/21/01		TITLE SCHEMATIC DIAGRAM MICRO ETHERNET CORE MODULE RCM2200		 2900 SPAFFORD ST. DAVIS, CA 95616 530 - 757-4616	
REVISED BY: RJH		21MAR01					
PROJECT ENGINEER:				SIZE		DWG NO.	
ENGINEERING MANAGER:				090-0120		SCALE	
				RELEASE DATE		SHEET 1 OF 2	

PROCESSOR

SF 1

FL-SH \*



6,17,47,57,70,89=VCC; 14,28,44,52,83,86=GND