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DACs FOR MODERN COMMUNICATIONS SYSTEMS ARE HIGHLY SOPHISTICATED. SELECTING THE RIGHT ONE FOR YOUR APPLICATION REQUIRES YOU TO BE SOPHISTICATED, TOO. A DEVICE THAT WORKS IN YOUR PROTOTYPE MAY OR MAY NOT BE RIGHT FOR THE PRODUCT YOU WANT TO SHIP.

Benchmarking DACs for communications requires a system-oriented approach

DACs are now vital elements in such applications as communications-system base stations, advanced antenna systems, test equipment, satellite uplinks, video projectors, and ultrahigh-resolution imaging systems. As DACs' role grows and versions proliferate, ensuring satisfactory performance in real applications requires designers to carefully review the published specifications, which almost always reflect performance under ideal conditions that differ substantially from the conditions under which the system operates.

To help assess how the actual performance departs from the ideal, designers can focus on important performance parameters—for example, signal characteristics at various frequencies or performance reductions for output signals in particular bands.

Most DACs that target these new applications list a resolution of at least 12 bits and a conversion rate of at least 100M samples/sec. However, the applications are dynamic in that system designers characterize the generated signals in the frequency domain. These signals can be either modulated or unmodulated. Key parameters in such applications are noise, ENOB (effective number of bits), and SFDR (spurious-free dynamic range) at application-specific frequencies. The design approach is known as IF or direct-IF synthesis. In systems that use this approach, the converter's performance determines whether the system meets its overall specifications and even whether the system can function at all.

Each application area requires a different type of signal—for example, narrowband or wideband—at a different frequency. The generated frequency is fundamentally linked to the requirements of the analog-signal chain that follows the DAC and any upconversion to IF or RF, such as NF (noise figure) and IP3 (third-order intercept). DACs that provide improved NF or IP3 can enable designers to reduce system complexity and improve system performance. A DAC that can generate higher frequencies may, for example, enable a reduction in the number of upconversion stages from two to one. Unfortunately, converter performance deteriorates at higher frequencies. This attribute is common to both ADCs and DACs, which exhibit three distinct operating areas in the frequency domain (**Figure 1**).

At low frequencies, performance is limited to dc specifications determined by architectural limitations or inherent noise sources. In the main operating region, performance exhibits a first-order reduction versus frequency. Finally, the frequency reaches a point at which performance degradation accelerates beyond practical use, primarily because device-to-device variations become significant. It is well-known that manufacturing tolerances create variations in analog components' performance and that these variations become more significant at higher frequencies. Obviously, design techniques can minimize these effects but can't completely eradicate them. As you push a device beyond the operating conditions for which it was designed, the circuit techniques that are supposed to ensure the device's performance reach a limit, and more and more portions of the design fail to operate correctly.

One way to improve the performance at a particu-

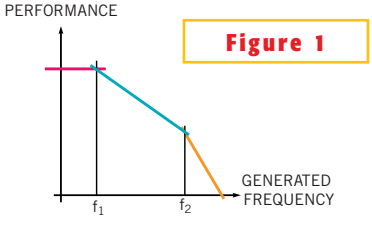


Figure 1

DACs exhibit three frequency-based performance regions. At low frequencies, dc considerations govern performance. In the middle band, which is the area of greatest interest for communications, performance is inversely proportional to the frequency the DAC is synthesizing. Above this middle band, performance degrades so rapidly with frequency and varies so much from sample to sample that the device is really unusable.

lar frequency is to increase the conversion rate. A higher conversion rate increases the effective oversampling ratio (conversion rate/generated frequency). This approach breaks down, however, when it pushes the conversion rate beyond the capability of the converter core.

The suitability of a converter to an application depends on the characteristics of both the converter and the signal you want it to generate. You can categorize signals as narrowband or wideband. Most system designers consider N-CDMA (narrowband-code-division-multiple-access) signals, whose bandwidth is approximately 1.2 MHz, to be wideband, even though the N-CDMA name suggests otherwise. TDMA (time-division-multiple-access) and GSM (Global System for Mobile communications) signals, which have a bandwidth of approximately 200 kHz, are considered narrowband. The reason for the distinction is that different parameters dominate the performance of the two types of systems. Noise dominates in the wideband case, whereas SFDR dominates in the narrowband application. A clue to the importance of noise in wideband systems is the importance of ACPR (adjacent-channel-power ratio) in such systems. ACPR is largely a function of adjacent-channel noise.

The evolution of third-generation W-CDMA (wideband-CDMA) systems provides an excellent example of these points (**Figure 2**). For the most part, first-generation and prototype systems adopted a single-carrier approach and implemented a direct IF at 16 MHz—one quarter of the converter's sampling rate. However, because a higher direct IF relaxes the requirements on the following upconversion stages, designers had to decide whether the benefits of a higher direct IF outweighed the problems associated with operating the DAC at a higher frequency within its main operating region. A DAC operating at 32 MHz could handle W-CDMA, possibly even including the multicarrier systems proposed for the UK third-generation channel-allocation plan (**Figure 3**). The multicarrier approach reduces costs for network operators who hold adjacent spectrum slots, thus making third-generation systems cost effective enough to justify a full network rollout. Ultimately, the higher direct IF will enable adoption of a single upconversion stage.

In TDMA systems, the move to multicarrier, multimode architectures that trade off converter performance for generated frequency now drives the need for higher performance DACs. For example, consider an AMPS (Advanced Mobile Phone System) device that generates a 22.5-MHz band, which covers the full A-band spectrum. Now, reduce the system cost by transmitting the same information over a single radio channel. Typically, such systems use multiple radio channels, with one carrier per channel. This discrete implementation suffers from a number of limitations, not the least of which is high per-channel cost. A high-performance DAC enables the system to combine the multiple carriers and, hence, multiple radio channels, into a less expensive single channel.

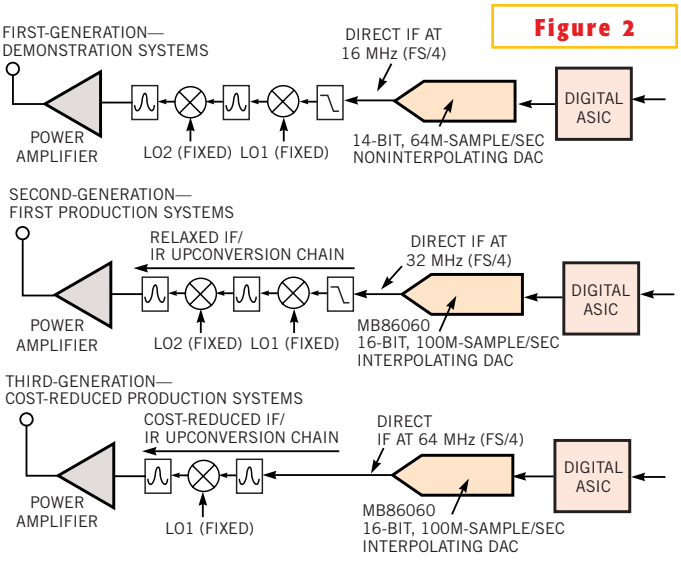
An input data rate of approximately 59M samples/sec could meet the Nyquist criterion if the generating band were 1 to 23.5 MHz. However, system architects might question the wisdom of placing the generated band at this low frequency, because low-order harmonics fall inband. This situation is not ideal for a system in which SFDR is expected to determine the overall performance. It may be preferable to use a higher data rate to achieve a higher generated band. For example, a DAC operating at 100M samples/sec might generate 20.5 to 43 MHz. Although such a system would not completely resolve the issue of inband low-order harmonics, simplification (relaxation) of the subsequent IF/RF upconversion could offer other advantages. The key question is whether the converter, operating at the higher frequency, can provide the required performance over the 22.5-MHz band.

After establishing the different architectures and their performance requirements, designers need to assess seemingly appropriate data converters to decide which provides the best performance. Almost certainly, the converters' data sheets don't provide sufficient minimum guaranteed specifications to allow a choice without a detailed evaluation. Initially, you can compare single-tone SFDR at similar frequencies for different DAC data rates. Although you shouldn't try to infer multitone performance from single-tone SFDR, single-tone performance can help you to judge the integrity of a DAC core at the intended data rate.

One problem is reduced SFDR for output signals in a particular band—say, 20 to 26 MHz—when you double the DAC rate, from, say, 60 to 120 MHz. Degraded performance at higher DAC rates with identical generated signals indicates a fundamental limitation in the converter's core. Such performance does not offer much hope of the DAC's generating higher frequencies, such as those closer to 40 MHz. Increasing the DAC rate for a given generated-signal frequency should improve performance by increasing the effective oversampling ratio and allowing the DAC output to take smaller steps between samples. However, whether increased oversampling yields an improvement depends on whether the converter design was optimized for small- or large-signal performance.

In a DAC that is optimized for large signal swings, in extreme cases, a user can "stuff" the output by forcing a return to

Figure 2

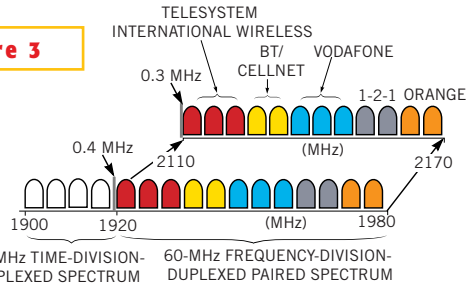


First-generation digital-cellular systems (top) used 16-MHz carriers. In newer architectures, the carrier frequency is 32 MHz because newer data converters can handle the higher frequency and because the higher carrier frequency enables design simplification downstream from the converter.

zero between samples. This approach causes a 6-dB loss of signal power, however. You should not underestimate the importance of this loss. System designers usually demand the highest ACPR or SFDR; immediately reducing these measures by 6 dB is rarely acceptable.

Selecting the best component for an application pays dividends. You must consider several factors besides the obvious system requirements. In communications systems, for example, you should ask what performance subsequent generations of the system might require. You can best accommodate evolving standards by selecting key components, such as data converters, that offer the highest performance. Added margin in the early stages of a design pays dividends through easier design reuse and avoids expensive re-evaluation. This approach gets systems to market faster.

Figure 3



The third-generation digital-cellular spectrum-allocation plan in the United Kingdom allocates adjacent bands of frequencies to the various phone companies. This arrangement allows the companies to use multicarrier systems that greatly improve the system economics. However, the multicarrier approach places stringent requirements on the data converters that the systems use.

Ideally, designers want DACs that deliver market-leading analog performance and also are optimized for integration into different systems. For example, DACs with integrated interpolation filters provide an ideal interface to either commercial DUCs (digital upconverters) or custom digital ASICs and provide the benefit of driving a 400M-sample/sec DAC core. True ECL data inputs are another useful ultrahigh-speed DAC feature because DACs with such inputs can replace BiCMOS and bipolar devices.

Designers are likely to derive advantages from selecting a high-performance converter core that has been enhanced through the integration of such features as interpolating filters, a versatile clock multiplier/generator, programmable digital dither, noise shaping, and segment shuffling. The high-performance clock circuit simplifies integration into the target system. Programmable dither improves small-signal linearity, particularly for the unmodulated signals that are used in test applications. Noise shaping lowers the noise floor in the baseband wanted-frequency band. Segment shuffling improves linearity of the converter's transfer function and redistributes spurious energy as noise. Together, these features yield a device that reduces the external-component count and offers flexibility to meet future system requirements.

One of the most significant issues for a data converter is the required external clock source. Although data converters will always require high-quality clocks, the clock frequency can affect the system-design complexity because demand for a high-frequency clock (for example, one that operates at four times the data rate of the interpolating DAC) can place otherwise unnecessary requirements on other system components. You can avoid such problems by selecting a DAC that incorporates a high-quality, integrated, DLL (delay-locked-loop)-based clock multiplier.

The evaluation phase is the point in a project at which you hope to discover the true usability of the devices that you have selected for your system design. You aren't always so lucky, however. Sometimes you think that a component has demonstrated the required performance, but you're still unsure of how well a design that uses it will transfer from the evaluation board to the prototype and ultimately to full-scale production. In data converters, a clue to possible future problems is significant clock-to-data-timing sensitivity. Unless handled properly in the converter, this noise mechanism can drastically affect the DAC's performance. Inevitably, when you use commercial test equipment to optimize the timing, you can achieve good performance. But, in the system, where the prototype circuit can no longer depend on external equipment to resolve timing issues, the circuit-design tolerances cause clock-to-data-timing sensitivity to manifest itself. By the time you recognize the problem, it is often too late.

Power consumption is also important. All applications have a power budget. Some power budgets are more flexible than others, and some designs can accept higher power components in return for improved performance. Just as you must carefully scrutinize performance, you must carefully review power consumption. Ultrahigh-speed DACs that claim power consumption of less than a few hundred milliwatts almost certainly don't deliver the lowest noise. Systems that use such components often fail to deliver the required ACPR or SFDR.

Finally, you must be careful that your system delivers the specified performance under realistic conditions. For example, you should be cautious of 14-bit converters that claim 3-LSB nonlinearity and quote SFDR at a low generated frequency, such as 5 MHz. Similarly, vendors must state the bandwidth of any measurement. Quoting the SFDR in a 5-MHz band when generating a 5-MHz tone, and thus avoiding any inband harmonic spurs, is a questionable practice. A lot of testing and evaluation described in this article, especially multicarrier TDMA tests, may use simple, unmodulated multitone test signals. When you create these test vectors, theory dictates that you must reduce the signal power of each carrier to prevent overload. The signal level corresponds to a particular peak-to-rms ratio. In reality, the target system generates modulated signals and, through controlled phase relationships among the carriers, enables increases in the signal power beyond the theoretical value. This approach not only promises to achieve higher SFDR but can change the portion of its transfer function that the converter uses, which, in extreme cases, can return very different results. In conclusion, no substitute exists for a detailed evaluation that ensures a data converter will deliver the required performance and that does not have to be repeated or reviewed.□

AUTHOR'S BIOGRAPHY

Paul Maddox is a technical marketing manager for the Mixed Signal Division of Fujitsu Microelectronics Europe. He holds a bachelor's degree in electrical and electronic engineering from The Hatfield Polytechnic (London). He is also a chartered engineer and a member of the Institution of Electrical Engineers. In his spare time, he enjoys running, swimming, and skiing.