Photo courtesy Linear Technology

Blindingly *fast ADCs*

TO GET MEANINGFUL INFORMATION, NOT JUST "DATA," YOU NEED TO KNOW HOW YOUR CONVERTER IS LOOKING AT YOUR SIGNAL.

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Stubborn as Zax (**Reference 1**), our world insists on being analog, and our best means of processing information about our world insist, for the foreseeable future anyway, on being digital. But our world and our means do not stand still. It, or rather all that information about it, moves faster and faster, enabled by new ADC designs that help bridge the gap between our analog reality and our digitized perceptions. What constitutes new, however, are not necessarily wholly novel architectures, but may be new implementations of old, well-known structures brought back to life or new twists brought to bear on evolving applications.

HOMING IN

Successive-approximation converters (commonly known as SAR converters after the successive-approximation register at their core) enjoy strong acceptance in telecommunications, spectrum-analysis, and imaging systems—all applications that stress dynamic performance. They also find sockets in high-speed data-acquisition and -control applications that are often sensitive to the converter's static specifications. Though all converters carry a nameplate corresponding to their resolutions, they do not necessarily offer commensurate performance for all specified parameters (see **sidebar** "So what *is* an N-bit converter?").

SAR converters use a DAC to test and compare bit combinations in sequence from MSB to LSB (**Figure 1**). At the start of a conversion, the controller clears the SAR bits and captures the input signal with an S/H amplifier. If the incoming signal is greater than half scale, the controller sets the SAR's MSB, forcing the DAC to half-scale. The converter repeats the comparison with the next-most-significant bit, setting or not setting it and the subsequent bits as determined by the comparator. The SAR feeds back the converging bit pattern to the comparator through the DAC at each iteration.

A benefit of this structure is that it uses one comparator and samples the input

ACRONYMS

DNL: differential nonlinearity
INL: integral nonlinearity
PECL: positive (or pseudo) emitter coupled logic
S/H amplifier: sample-and-hold amplifier
SINAD: signal-to-noise-and-distortion ratio
T/H amplifier: track-and-hold amplifier
THD: total harmonic distortion

once per conversion, eliminating matching errors found in pipelined structures (**Reference 2**). Capacitive-DAC topologies make excellent use of the capacitor-matching and -scaling capabilities and low-charge-injection-switch characteristics of modern semiconductor processes. As a result, SAR ADCs can support resolutions as fine as 16 bits with good nonlinearity numbers and conversion rates as fast as several megasamples per second, though not necessarily at the same time. The dependence on capacitance ratios can also lead to good behavior over temperature. The capacitive DAC structure also simplifies integrating the S/H-amplifier function.

SAR-converter designs differ, however, in whether they integrate an input-buffer amplifier. Some require you to directly drive the sampling caps, which necessitates that your application circuit provide impulse currents at the start of each conversion cycle. Others provide an on-chip input-buffer amplifier with fixed characteristics. Depending on your signal source, you may not prefer the on-chip input buffer. If your signal source has a low dynamic output impedance and is located near the converter, you may choose to forgo an input buffer. If your source signal has sufficient bandwidth, your design may require filtering ahead of the converter leading to an external amplifier anyway.

The LTC1411 is a good example of the features available on CMOS SAR converters (**Table 1**). The input structure includes differential inputs whose com-

AT A GLANCE

- Don't confuse a converter's resolution (number of many wiggling bits) with its performance. In the best cases, you'll lose less than a bit of resolution to ac error terms, but, in many cases, the loss approaches 2 bits.
- Despite the concentration on ac parameters, poor static behavior can adversely affect high-speed ADC applications.
- A preponderance of specsmanship on the part of ADC vendors results in data sheets deserving careful reading and comparisons. Be aware of claims that apply at frequencies well below your bandwidth of interest.
- Most high-speed ADCs provide integrate S/H or T/H amplifier front ends and voltage references for scaling, which minimize the external "glue" you need to design an ADC into your application.

SO WHAT *IS* AN N-BIT CONVERTER?

If you come from an instrumentation background, you probably expect that an ADC will exhibit linearity errors on the order of ½ LSB over its range. You can trust that, at this level of performance, the converter is not corrupted by its own internal errors; it's as good as perfect. However, as your bandwidth of interest increases, that level linearity becomes difficult to attain and would eventually become less the focus of your task were it not for the fact that static and dynamic errors are related.

The SNR of an ideal N-bit converter is 6.02N+1.76 dB owing to the rms value of quantization noise. (An intuitively pleasing approximation of 6 dB per bit is a good number to keep in mind.) If you postulate nonzero DNL, the SNR decays. In the most benign case, where narrow bits and wide bits are evenly distributed over the transfer function, the rms noise increases by the 3/2 power of the DNL (**Reference A**). At ½-LSB DNL with alternating long and short codes, the SNR drops to 6.02N−0.65 dB, about 2 dB worse than the ideal case. Converters with substantial INL don't exhibit evenly distributed code-width errors, which further adds to the quantization noise. As clock rates increase, acquisition jitter in the S/H or T/H amplifier represent another noise source.

SINAD is the ratio, expressed in decibels, of the rms value of the input signal and the sum of all the other spectral components, usually including the first five harmonics but not including dc. You can calculate the ENOB (effective number of bits) directly from SINAD: ENOB=(SINAD−1.76 dB)/6.02. The noise component is a primary reason that high-speed converters rarely offer ENOB figures corresponding to their resolutions. As you sweep through the converter's bandwidth, the SINAD curve decays, and the ENOB decays with it. Because converter manufacturers usually measure SINAD only to the Nyquist frequency, carefully read the data sheets for converters recommended for undersampled applications.

Spurious-free dynamic range is the ratio, also in decibels, of the input signal's rms value to the peak spurious signal. These numbers often correlate closely with the THD performance in circuits free of interference sources.

If your application requires a converter with good static numbers, check how the manufacturer specifies the integral nonlinearity. Many manufacturers' data sheets report "best-straight-line" INL, which is a measure of the converter's second-order and higher transfer-function errors. Unfortunately, the best straight line assumes that you are willing to sacrifice offset and span accuracy to minimize the worst-case error throughout the span and that you are willing and able to characterize the converter's transfer function to do so. When manufacturers specify endpoint nonlinearity, they agree to treat the transfer function's zero- and full-scale values as cardinal points, allowing you to use a simple two-point zero- and full-scale calibration check. If you use them in this way, the numbers given for a converter specified for best straight line can be optimistic by as much as a factor of two. In cases where the converter's transfer function exhibits a perfectly symmetrical S-shaped nonlinearity curve, the two measures converge on the same value.

REFERENCE

A. Demler, Michael, *High-Speed Analog-to-Digital Conversion*, Academic Press, 1991, pg 92.

mon-mode range extends to the supply rails. A 2.5V bandgap reference, a scaling network, and a reference amplifier allow the converter to read single-ended ground-referenced inputs and provide means for setting the span of the conversion process in 3-dB increments from 0 to −9 dB referenced to 3.6V. In addition to the parallel data interface, the 1411 features busy and out-of-range flags and five control inputs—two that set the span, two that initiate the snooze modes (nap and sleep), and one that initiates a conversion cycle. An internal clock reduces the external component count but disallows synchronizing multiple channels.

The LT1411 offers dynamic specifications in line with its nameplate resolution. THD is −88 dB with a 500-kHz fundamental. Intermodulation distortion, tested with 97.7- and 104.2-kHz input signals, is −86 dB. The SINAD at 80 dB is 6 dB off a theoretically perfect 14-bit converter.

The 1411 also guarantees no missing codes (DNL less than 1 LSB over the input range), and the INL is a modest ±2 LSBs. The LT1411 dissipates a maximum of 325 mW when operational, and typically 10 mW and 5 μW in nap and sleep modes, respectively. It is available in a 36-pin SSOP with versions suitable for the commercial and industrial temperature ranges.

The AD7664 SAR converter from Analog Devices offers 16-bit resolution at conversion rates as fast as 570k samples/sec with both serial and parallel outputs. The company specifies the converter's dynamic performance with 10- and 100-kHz inputs. The part turns in −100-dB THD and 100-dB spurious-free dynamic range with 10-kHz signals, both falling 10 dB at 100 kHz. As a result, the SNR figure of 90 dB at 10 kHz dominates the SINAD calculation. The 3-dB bandwidth extends to 18 MHz.

In addition to 2.5 LSB INL and no missing codes, the span error of 0.08% full-scale range is better than what you could get from all but the most tightly matched resistor pairs. The converter offers three modes of operation with different throughput rates and power dissipation levels to match. At 500k samples/sec, the part dissipates a maximum of 115 mW, but when you use it in its low-power "Impulse" mode, dissipation falls with the sampling rate to a typical 21 μW at 100 samples/sec

Texas Instruments offers the ADS8322, a 500k-sample/sec, 16-bit converter for less than half the price of the AD7664. Its ac performance does not match that of the 7664 with 86-dB SINAD and −92-dB THD, both at 10 kHz. The static characteristics are essentially that of a 14-bit converter in the standard grade. But for a project on a tight budget that doesn't need 16-bit performance, the 8322 is an attractive alternative to many competing parts. The ADS8322 takes an external clock signal allowing you to synchronize multiple channels. Its maximum power dissipation is 125 mW.

TI also makes the ADS7862, a dual 500k-sample/sec, 12-bit converter that features simultaneous sampling from two dual-multiplexed differential inputs (**Figure 2**). An address pin selects between the two inputs for each channel. The conversion start and clocking signals are common to the two converters. Two read accesses per conversion cycle report the A and B channel data sequentially through the single 12-bit port.

Geared toward motor- and position-control applications, the input range extends to 300 mV beyond the supply rails. The static numbers suit control applications with 1- and 2-LSB DNL and INL maximum and a 1-LSB INL match between the two channels. The 7862 holds its offset to 3 LSB and span error to less than 1%. The two channels have gain-match errors of 2 LSB maximum. The manufacturer characterizes the converter's dynamic capability with only typical numbers, which are themselves quite attractive: 1-dB SINAD and −78-dB spurious-free dynamic range. The lack of minimum and maximum values, however, raises obvious challenges for applications that depend on the converter's dynamics.

QUICK AS A FLASH

After decades of converter development, the fastest conversion method yet devised is still the flash converter (**Figure 3**). This architecture incorporates a string

TABLE 1–REPRESENTATIVE SUCCESSIVE-APPROXIMATION ADCs

Manufacturer	Model	Resolution (bits)	NMC* (bits)	Speed (k samples/sec)	NMC* speed product (kbps)	Maximum power dissipation (mW)	Power efficiency (kbps/mW)	Full-power bandwidth (MHz)	Package	Price (1000)
Linear Technology	LTCLinear Technology C	L								

of 2^N reference voltages, one for every output code, and simultaneously measures the input against each of them through an equal number of comparators. A logic decoder converts the comparator outputs, often collectively likened to a thermometer, to any of several binary codings. The obvious limiting factor for the flash architecture is that its area grows exponentially with the number of bits. Even with the reduction of critical dimensions in semiconductor processes, flash converters are generally impractical at resolutions greater than 8 bits.

One weakness of flash converters centers on the comparators' dynamics around their thresholds. A comparator's settling time grows exponentially as the

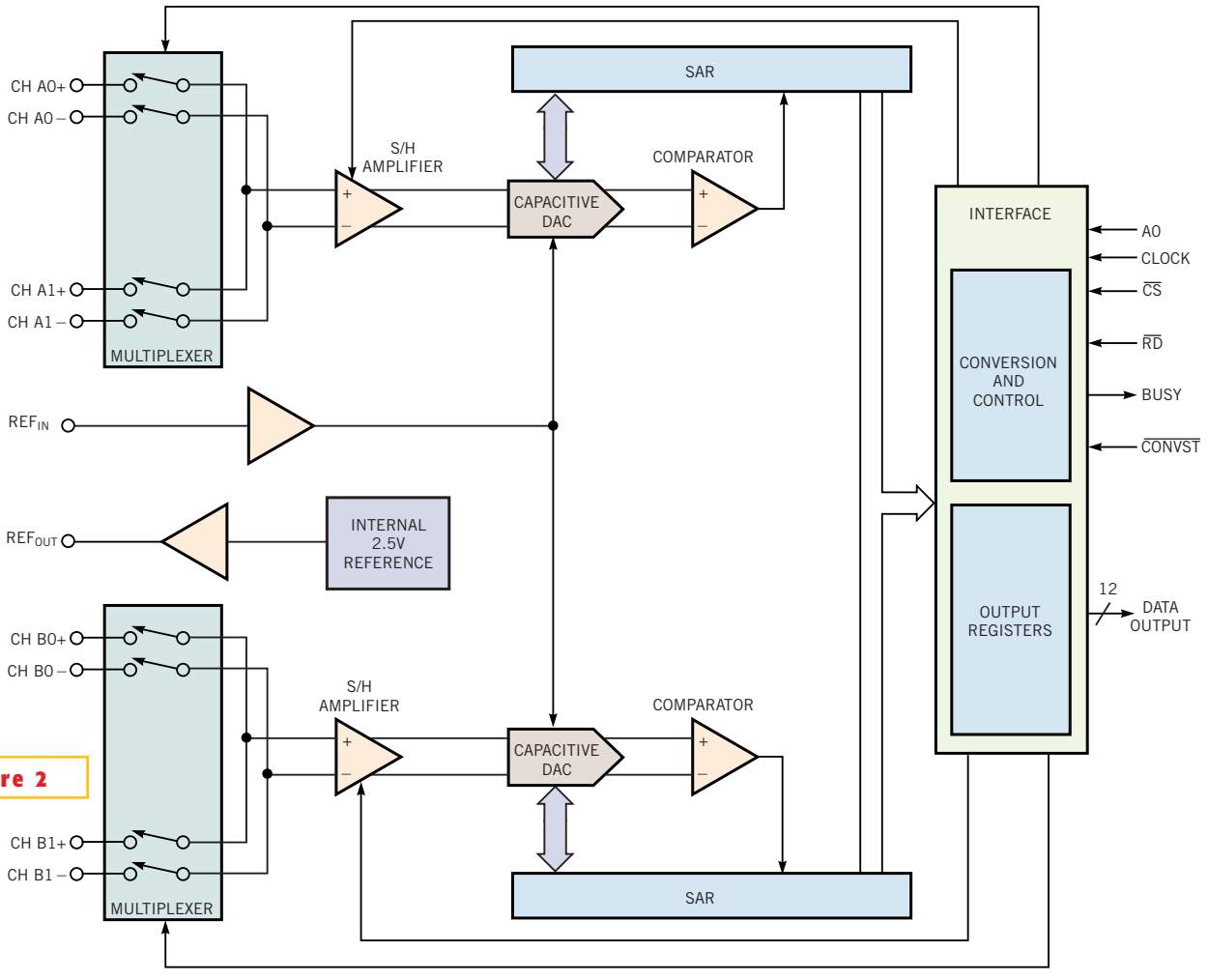

Figure 2

The ADS7862 from Texas Instruments features two synchronized 500k-sample/sec, 12-bit SAR-converter channels.

TABLE 2–REPRESENTATIVE PIPELINED ADCs

Manufacturer	Model	Resolution (bits)	NMC* (bits)	Speed (M samples/sec)	NMC* speed product (Mbps)	Maximum power dissipation (mW)	Power efficiency (Mbps/mW)	Typical –3-dB bandwidth (MHz)	Package	Price (1000)
Analog Devices	AD9433	12	12	125	1500	1250	1.2	750	PQ4-52**	$80
Texas Instruments	ADS809	12	11	80	880	945	0.9	1000	TQFP-48	$29.95
Maxim	MAX1448	10	10	80	800	160 EST	5.0	400	TQFP-32	$8.35
Analog Devices	AD6644	14	13	65	845	1500	0.6	250	LQFP-52	$39
Analog Devices	AD9226	12	12	65	780	500	1.6	750	SSOP-28	$18.55
Maxim	MAX1446	10	10	60	600	135 EST	4.4	400	TQFP-32	$7.35
STMicroelectronics	TSA1201	12	12	50	600	158	3.8	1000	TQFP-48	$17
STMicroelectronics	TSA1002	10	10	50	500	158	3.2	100	TQFP-48	$5.95
Maxim	MAX1444	10	10	40	400	90 EST	4.4	400	TQFP-32	$5.85

*NMC = no missing codes; **PQ4 = "power quad 4," according to Analog Devices.

input differential grows small (**Reference 3**). Continuous input signals will eventually require the structure to discriminate between adjacent codes with an instantaneous amplitude that is only a small fraction of an LSB from the transition point between them. In such cases, the settling time for one comparator may extend beyond the conversion time. The unsettled comparator leads to metastable states in the decoding logic that often result in large single-conversion errors, particularly when the signal is near a major carry. These occurrences of metastability and their artifacts are known colloquially as "thermometer bubbles," after their representation at the comparator outputs, or "sparkle codes," after the visual effect they have when flash converters capture video information.

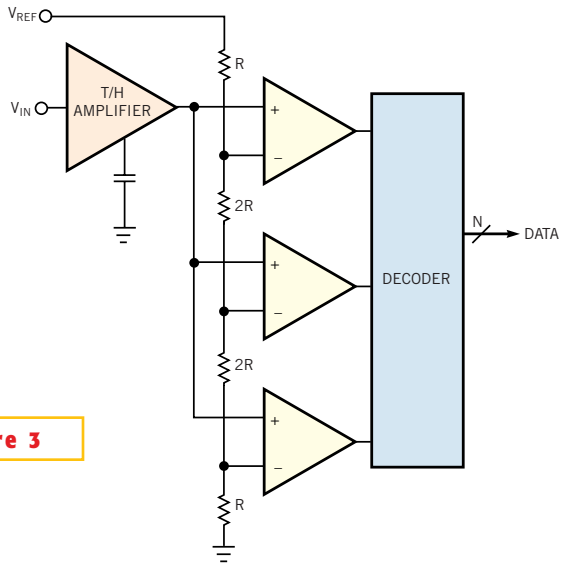

Figure 3

Quick as a blink, the flash converter requires 2^N comparators, which limits practical realizations to around 8 bits.

Maxim has pressed its 27-GHz GST-2 bipolar process into service for a trio of 8-bit flash converters: the MAX106, 104, and 108, which offer digitizing rates of 600M, 1G, and 1.5G samples/sec, respectively. The Max10x converter designs go well beyond the high-speed flash core. The integrated T/H amplifier's differential inputs include on-chip 50Ω termination resistors, as do the differential clock inputs. A bandgap reference sets the ADC's scaling factor, and the part's pinout allows you to either scale the reference or replace it with an external source.

The converter's decoder is designed to limit the occurrence of metastable states to one in 10^{15} clock cycles with no error exceeding an LSB. An output demultiplexer feeds the 8-bit differential outputs to two output ports that you can use in any of three modes. A nondemultiplexed mode feeds the result of every conversion to the primary port, and the same data stream, delayed by one conversion time, to the auxiliary port. You can choose to power down the auxiliary port to save power and use the converter as a straight, one-port device. In the demultiplexed mode, the data-ready flag rises once for every two conversions. The demultiplexer directs the first conversion's results to the auxiliary port and the second's to the primary port. The third mode discards every other conversion and, like the demultiplexed mode, directs the first of the retained conversion results to the auxiliary port and the second to the primary port. The ports' differential outputs are PECL-compatible and powered by their own rails, so you can connect them to either 5 or 3.3V data buses.

The $495 (1000) MAX108, the fastest of the trio, offers $^1/_2$-LSB maximum DNL and best-straight-line INL. The manufacturer gives dynamics specifications at 250 MHz, 750 MHz (the Nyquist frequency), and 1.5 GHz. Worst-case SINAD at the Nyquist frequency with differential inputs is 44.5 dB, limited by noise. The part yields 50-dB spurious-free dynamic range under the same conditions.

PUT THAT IN YOUR PIPE

Pipeline converters lie between SAR converters, which top out at 16 bits and

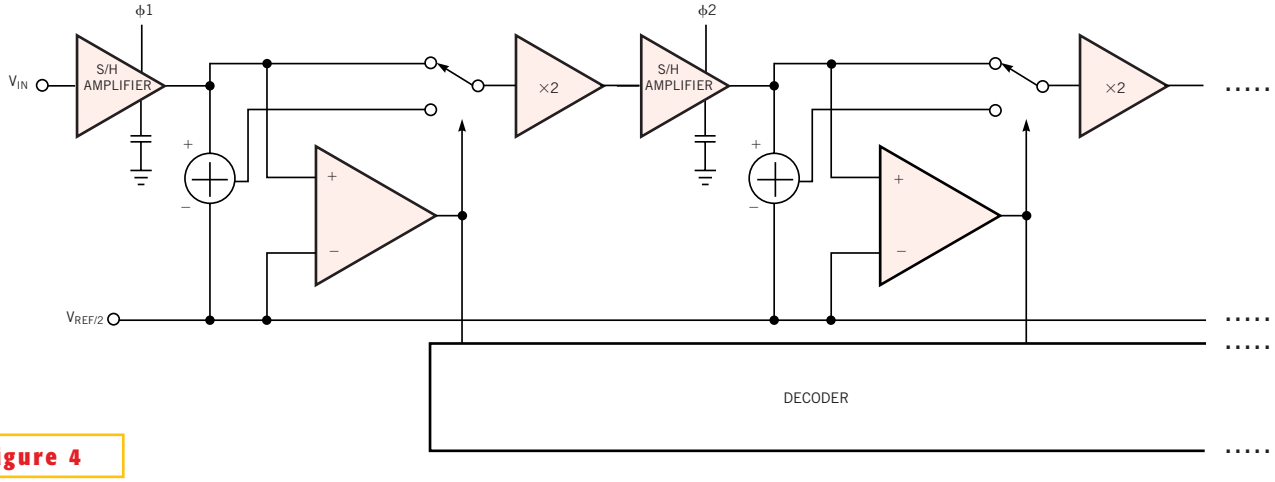

Figure 4

Pipelined converters offer high throughput rates with low circuit complexity. The conversion latency poses difficulty, however, with closed-loop and multiplexed applications.

single-digit megasamples per second, and flash converters, which have speeds to single-digit gigasamples per second but resolutions limited to 8 bits. Examples of pipeline ADCs operate at several tens of megasamples per second and 10- to 14-bit resolutions (**Table 2**).

SAR converters sequentially use one comparator and DAC N times. Flash converters use 2^N comparators in a single comparison time. Between the two, the bit-serial pipeline ADC uses N comparators to complete one conversion per cycle each with an N-cycle latency (**Figure 4**). On the first clock phase, the first S/H amplifier captures the input signal, which a comparator measures with respect to a half-full-scale reference. Inputs smaller than the half-scale reference pass on to the second S/H amplifier through a gain of 2. Inputs larger than the reference route to a differencer, which subtracts the reference from the input before the gain of 2 and the second S/H amplifier. On the second clock phase, the process repeats with an identical stage. The converter replicates this structure with odd-numbered stages clocked on the first phase, and even numbered stages clocked on the second phase. In this fashion, a conversion proceeds through the converter in N clock cycles, but a new conversion completes on every cycle. A variation on the basic bit-serial pipeline architecture replaces each stage's single comparator with an m-bit flash converter and the gain of 2 with a gain of 2^m, reducing the latency to N/m cycles. A further refinement uses overlapping stages to further reduce nonlinearity at the cost of a somewhat longer pipe. Even with latency reduction, pipeline delays can pose stability problems for control loops and synchronization challenges for multiplexed or synchronous parallel data-acquisition systems. However, for single-channel nonfeedback applications, such as undersampled IF digitizers, pipelined converters offer a combination of speed and resolution unavailable from other architectures.

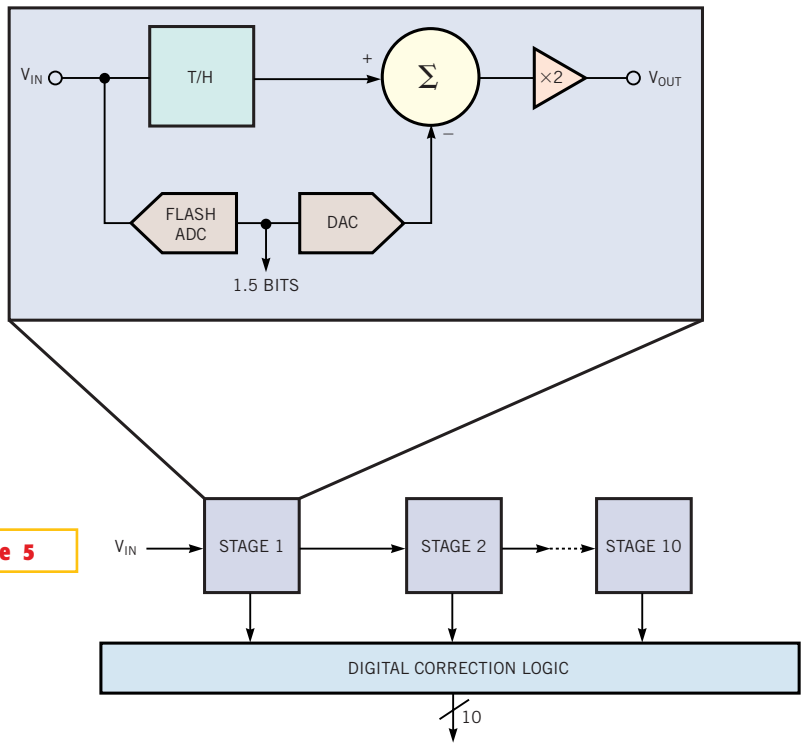

Figure 5

A small flash ADC, overlapping stages, and digital correction logic relieve pipeline-matching errors and improve linearity.

Pipelined structures bring several challenges to converter designers. The sampling process can add step errors due to the charge injected when the MOS switches open at the end of the sampling interval. The injected charge is a function of the MOS device's V_{GS}, so fixed-level switching can add a nonlinearity term. Although compensated switch topologies minimize this error source, they do not eliminate it. The sampling process also adds kT/C noise at each stage. Following stages amplify the noise along with the residual signal. Stage-to-stage differences lead to linearity disjoints, and multibit stages require gain cells with proportionally greater bandwidth. The converter must balance the advantages of multibit stages with the process capability and throughput requirements. Although digital techniques can compensate for static errors, bandwidth and noise limitations do not yield to such treatments and often distinguish between converter product lines.

STMicroelectronics offers a 12-bit, 50M-sample/sec pipelined ADC for portable applications. The TSA1201 dissipates 158 mW maximum from 2.5V supplies at full speed and typically only 40 mW at 5M samples/sec. The input bandwidth extends to 1 GHz for undersampled applications, however, as you should expect of all high-speed convert-

FOR MORE INFORMATION...

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ers, the 61-dB minimum SINAD measured at 15 MHz falls off at high frequencies, 3 dB down at 90 MHz.

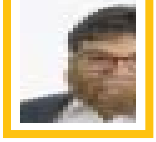
The 1201 features good static specifications: 0.6 and 1.7 LSB DNL and INL, respectively. Noise limits the ac numbers to the 10-to 11-bit range; 61-dB SINAD, despite −68-dB THD, results in a 10-bit effective number of bits, all measured at 15 MHz.

Analog Devices' AD9226 12-bit ADC features an eight-stage, 1.5-bit pipeline that you can clock as fast as 65M samples/sec. It takes 500 mW to drive the 9226, resulting in 67.4-dB SINAD, −76-dB THD and spurious-free dynamic range, and 10.9 effective number of bits, all measured at 15 MHz. The SNR holds up fairly well at high input frequencies, falling typically at 3.4 dB at 15 to 200 MHz.

Like the AD9226, the MAX1448 10-bit converter from Maxim exemplifies the pipelined structures built with flash-converter stages (**Figure 5**). The 80M-sample/sec 1448 offers 55.3-dB SINAD and 61-dB SFDR at 20 MHz. Its differential-input T/H-amplifier front end has a 400-MHz, −3-dB bandwidth.

The ADS809 from Texas Instruments also competes in the 12-bit arena at 80M samples/sec. Its T/H amplifier accepts either differential or single-ended signals. Internal reference scaling allows you to choose among 1, 1.5, and 2V p-p full-scale inputs. The manufacturer offers few worst-case specifications for the ADS809. Among these, 1.7 and 6 LSBs for DNL and INL, respectively, suggest mid-band dynamic results in the 10- to 11-bit neighborhood, as does the worst-case 65-dB SFDR and typical 63-dB SINAD with 10-MHz inputs.□

You can reach Technical Editor Joshua Israelsohn at 1-617-558-4427, fax 1-617-558-4470, e-mail jisraelsohn@cahners.com.



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